AND8118/D

EPT21/23/25 ECLinPS Plus™ Translator TTL output SPICE Modeling Kit

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APPLICATION NOTE

Objective

The objective of this kit is to provide customers with enough circuit schematic and SPICE parameter information to allow them to perform system level interconnect modeling for the current devices of the ECLinPS Plus logic line, ON Semiconductor's high performance ECL family. **The kit is not intended to provide information necessary to perform circuit level modeling on ECLinPS Plus Translator devices.**

Schematic Information

The kit contains representative input and output schematics, netlists, and waveform used for the ECLinPS Plus Translator devices. This application note may be modified as new device input or output buffers are added. The subcircuit models such as the input or output buffer, package, input ESD, and output ESD may be interconnected as subcircuits to simulate specific a device input an output buffers structure as shown in Figure 1 below. The block diagram in Figure 2 illustrates a typical driver and receiver interconnect configuration which can be modeled using the information in this kit.

There are four terminals on all transistor models: Emitter, Base, Collector, and Substrate (biased to V_{EE}). It should be noted that the input buffer circuit would drive differentially by replacing IN with the inverted $\overline{IN}$ signal.

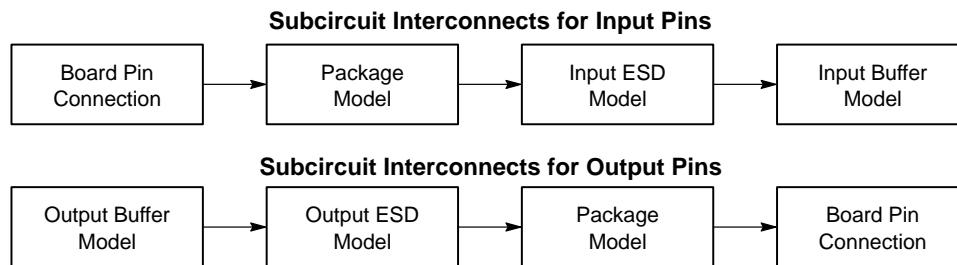Table 1 describes the nomenclature used in the schematics and netlists.

Subcircuit Interconnects for Input Pins

Subcircuit Interconnects for Output Pins
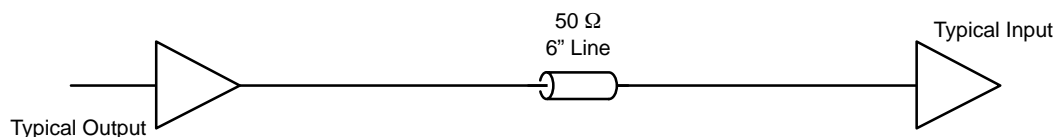

Figure 1. Input and Output Pins Interconnects

Figure 2. Typical Application for I/O SPICE Modeling Kit

Table 1. Schematics and Netlist Nomenclature

Parameter	Function Description
V_{CC}	3.3 V / 0.0 V*
VCS	Internal Reference Voltage (V_{EE} + 1.1 V $\pm$ 50 mV)
V_{EE}	0.0 V / −3.3 V* LVECL
GND	0 V
IN	TRUE (Positive Phase) INPUT TO CKT
INb or $\overline{IN}$	INVERTED (Negative Phase) INPUT To CKT
INTA	Internal Input Node A to Drive TTL Output
INTB	Internal Input Node B to Drive TTL Output
Q	TTL Output of CKT (Positive Phase)

*EPT25

Input Buffer

The Typical ECL Input Buffer schematic (see Figure 3. Typical INBUF) and netlist represents the Low Voltage NECL configuration of the ECL structure currently in use on the MC100EPT25 device in this family. To simulate a Low Voltage PECL mode of operation used on the MC100EPT21 and MC100EPT23, all levels except VCS, are adjusted (shifted) +3.3 V with respect to V_{CC}. The VCS is adjusted with respect to V_{EE} (as approx. VEE + 1.1 V $\pm$ 50 mV)

This schematic requires the addition of ESD models (Figures 5 and 7) and package models (see Appendix A and B) for increased accuracy in simulated model behavior. The internal input pull−up and / or pull−down resistor is shown in the ESD network, Figures 5 and 6. It is unnecessary to include an ESD or package model for the V_{BB} pins of the models because V_{BB} is intended as an output node voltage reference. If V_{BB} is modeled as an external node, it is usually bypassed as a constant voltage supply. Adding ESD and Package parameters would provide no additional benefit to the V_{BB} pin.

Output Buffer

The low voltage TTL output buffer schematic with output ESD structure and simplified package model can be seen in Figure 4. Any input or output that is driving or being driven by an off chip signal should include the ESD and package models. When simulating an output, the load (resistor and capacitance), package model, ESD structure, and the output emitter follower of the unused output, should not be eliminated to simplify the system model.

Package

A case model for SOIC8 (Appendix A) and TSSOP8 (Appendix B) package types is included to improve the accuracy of the system model. The package model represents the parasitics from the pin up to, but not including the die pad. The package pin model should be represented on each device input pin connecting to an input model, all device output pins connecting to an output model, V_{CC}, and

VEE. A package model can be used at the V_{EE} pin, but is not necessary since the current in the V_{EE} pin is a constant. An expansion of the SOIC8 Package Model can be found at the end of Appendix A. When high accuracy is not important and to speed up the simulation process, the simplified package model can be used, which is shown in Figure 4.

ESD

The ESD structure used in the ECLinPS Plus Translators with TTL output are found in Figures 5, 6, and 7. For MC100EPT21 and MC100EPT23 devices ESD structure, use Figure 6. Input ESD with pull−up and pull−down EPT21/23. For the MC100EPT25, use Figure 5. Input ESD with Pull−down EPT25. Use Figure 7 for output pin ESD structure.

SPICE Netlists

The netlists are organized as a group of subcircuits. In each subcircuit model netlist, the model name is followed by a list of external node interconnects. Subcircuit models such as the Input or Output Buffer, Package, Input ESD and Output ESD should connect to supplies through hierarchical, passed parameters such as V_{CC}, V_{EE}, etc., for proper simulation and not separately attached to independent power supplies.

SPICE Parameter Information

In addition to the schematics and netlists is a listing of the SPICE parameters for the referenced transistors, TNA and TN1. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the transistor structures, but for the type of modeling that are intended by this application note actual delay times are not necessary since they are not modeled. Variation of the device transistor parameters is not recommended. Some output performance levels are more easily varied by other methods and will be discussed in the next section.

Modeling Information

The VCS or V_{BB} bias drivers for the devices are not detailed since their circuitry would result in a substantial increase of model complexity and simulation time. Instead, these internal reference voltages are driven with ideal constant voltage sources. The output buffer schematic and netlist simulate a typical output waveshape, which can be seen in Figure 8: LVTTL_OUT – Output Waveform (f = 250 MHz).

Simple adjustments may be made to the models allowing some output variance to simulate conditions near mean or typical conditions. This application note is not intended to provide simulation of data book specifications limits or process corners of a device.

Summary

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation.
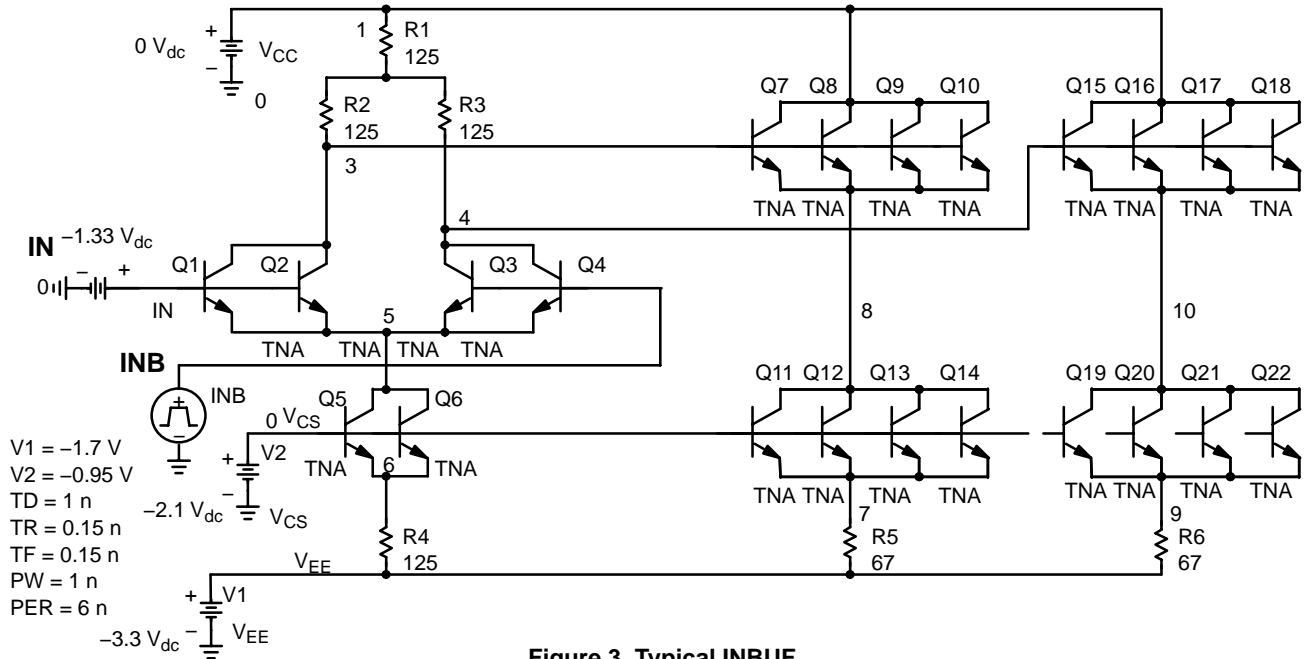
Input Buffer

Figure 3. Typical INBUF

```
.SUBCKT TYPICAL INBUF IN INB VCS VEE
Q_Q1 3 IN 5 TNA
Q_Q2 3 IN 5 TNA
Q_Q3 4 INB 5 TNA
Q_Q4 4 INB 5 TNA
Q_Q5 5 VCS 6 TNA
Q_Q6 5 VCS 6 TNA
Q_Q7 1 3 8 TNA
Q_Q8 1 3 8 TNA
Q_Q9 1 3 8 TNA
Q_Q10 1 3 8 TNA
Q_Q11 8 VCS 7 TNA
Q_Q12 8 VCS 7 TNA
Q_Q13 8 VCS 7 TNA
Q_Q14 8 VCS 7 TNA
Q_Q15 1 4 10 TNA
Q_Q16 1 4 10 TNA
Q_Q17 1 4 10 TNA
Q_Q18 1 4 10 TNA
Q_Q19 10 VCS 9 TNA
Q_Q20 10 VCS 9 TNA
Q_Q21 10 VCS 9 TNA
Q_Q22 10 VCS 9 TNA
R_R1 2 1 125
R_R2 3 2 125
R_R3 4 2 125
R_R4 VEE 6 125
R_R5 VEE 7 67
R_R6 VEE 9 67
V_V1 VEE 0 −3.3Vdc
V_V2 VCS 0 −2.1Vdc
V_IN IN 0 −1.33Vdc
V_VCC 1 0 0Vdc
V_INB INB 0
+PULSE −1.7V −0.95V 1n 0.15n 0.15n 1n 6n
.END TYPICAL INBUF
```

Output Buffer
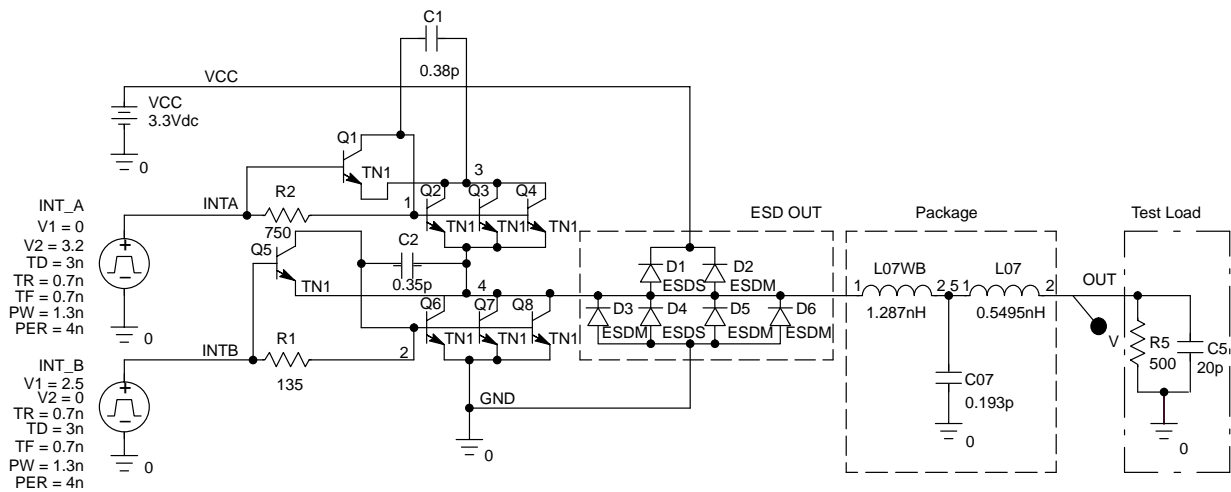
Figure 4. LVTTL_OUT

```
.SUBCKT EPT_LVTTL_OUT_PACKAGE
Q_Q1          1 INTA 3 TN1
V_VCC         3 0 3.3Vdc
Q_Q2          3 1 4 TN1
C_C5          0 OUT  20p
Q_Q8          4 2 0 TN1
Q_Q4          3 1 4 TN1
D_D6          0 4 ESDS
R_R1          2 INTB  135
L_L07WB       4 5  1.287nH
R_R5          0 OUT  500
L_L07         5 OUT  0.5495nH
D_D2          4 3 ESDM
D_D3          0 4 ESDM
C_C1          1 3  0.38p
Q_Q7          4 2 0 TN1
D_D5          0 4 ESDM
R_R2          INTA 1  750
Q_Q5          2 INTB 4 TN1
Q_Q3          3 1 4 TN1
C_C07         0 5  0.193p
D_D4          0 4 ESDS
V_INT_A   INTA 0
+PULSE 0 3.2 3n 0.7n 0.7n 1.3n 4n
D_D1          4 3 ESDM
Q_Q6          4 2 0 TN1
V_INT_B       INTB 0
+PULSE 2.5 0 3n 0.7n 0.7n 1.3n 4n
C_C2          2 4  0.35p
.END EPT_LVTTL_OUT_PACKAGE
```
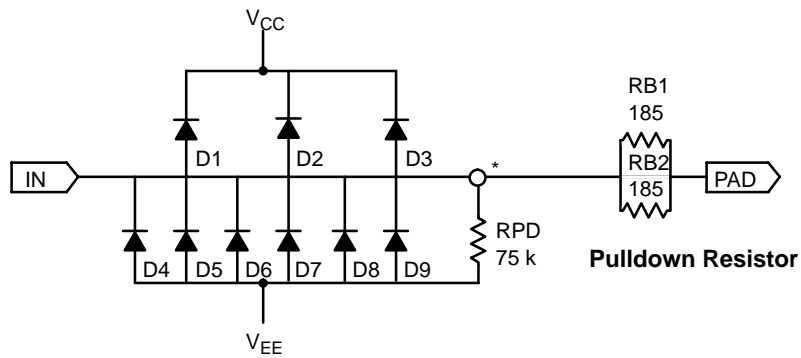
Figure 5. Input ESD with Pull–down EPT25

```
.SUBCKT IN_ESD_PD VCC VEE IN PAD
D1  IN  VCC ESDM
D2  IN  VCC ESDM
D3  IN  VCC ESDM
D4  VEE IN  ESDM
D5  VEE IN  ESDS
D6  VEE IN  ESDM
D7  VEE IN  ESDS
D8  VEE IN  ESDM
D9  VEE IN  ESDS
RPD IN  VEE 75K
RB1 IN  PAD 185
RB2 IN  PAD 185
.ENDS IN_ESD_PD
```
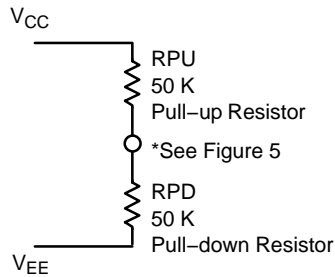

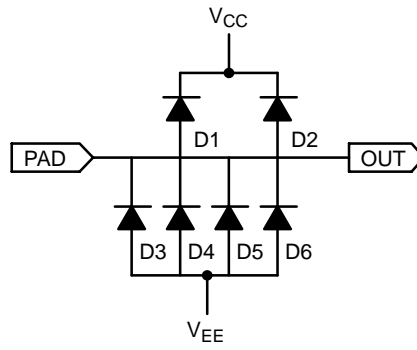**Figure 6. Input ESD with Pull–up and Pull–down EPT21/23**

```
.SUBCKT IN_ESD_PU VCC VEE IN PAD
D1  IN  VCC ESDM
D2  IN  VCC ESDM
D3  IN  VCC ESDM
D4  VEE IN  ESDM
D5  VEE IN  ESDS
D6  VEE IN  ESDM
D7  VEE IN  ESDS
D8  VEE IN  ESDM
D9  VEE IN  ESDS
RPD IN  VEE 50K
RPU IN  VCC 50K
RB1 IN  PAD 185
RB2 IN  PAD 185
.ENDS IN_ESD_PU
```

Figure 7. Output ESD

```
.SUBCKT OUT_ESD VCC VEE OUT
D1 OUT VCC ESDM
D2 OUT VCC ESDM
D3 VEE OUT ESDM
D4 VEE OUT ESDS
D5 VEE OUT ESDM
D6 VEE OUT ESDS
.ENDS OUT_ESD
```

2.41V
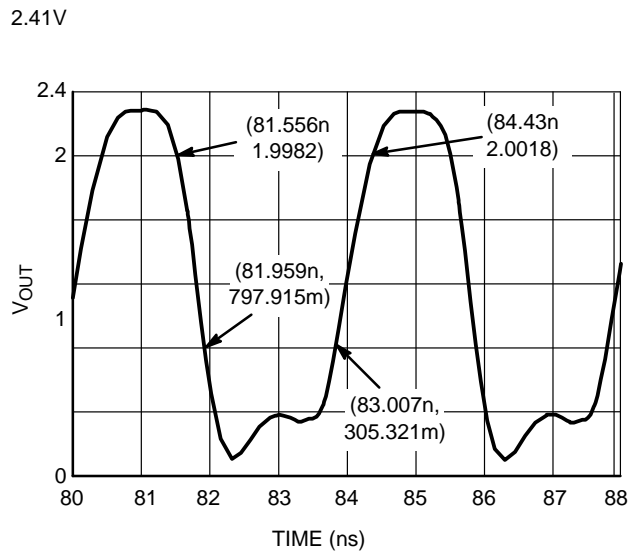
Figure 8. LVTTL_OUT – Output Waveform (f$_{in}$ = 250 MHz)

*********** Transistor and Diodes Nominal SPICE Models* ***********

```
**************************************************************************
.MODEL TNA NPN (IS=6.54e-18 BF=195 NF=1 VAF=93.6 IKF=6.81e-03
+ ISE=3.26e-16 NE=2.5 BR=18.4 VAR=2.76 IKR=6.36e-04 ISC=1.89e-17
+ NC=1.426 RB=544 IRB=3.16e-05 RBM=154 RE=13 RC=61 CJE=1.45e-14
+ VJE=.8867 MJE=.2868 TF=8.00e-12 ITF=5.2e-03 XTF=2.8 VTF=1.4 PTF=41.56 TR=1e-9
+ CJC=5.68e-15 VJC=0.632 MJC=0.301 XCJC=.3 CJS=7.94e-15 VJS=.4193 MJS=0.256
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
.MODEL TN1 NPN (IS=2.18e-17 BF=179 NF=1 VAF=96.5 IKF=2.42e-02
+ ISE=3.83e-16 NE=2.5 BR=20.4 VAR=2.76 IKR=1.98e-03 ISC=2.91e-17
+ NC=1.426 RB=230 IRB=1.12e-04 RBM=48 RE=6 RC=22 CJE=4.98e-14
+ VJE=.8867 MJE=.2868 TF=8.00e-12 ITF=1.6e-02 XTF=2.8 VTF=1.4 PTF=41.56
+ TR=1e-9 CJC=1.55e-14 VJC=0.632 MJC=0.301 XCJC=.3 CJS=1.71e-14 VJS=.4193
+ MJS=0.256 EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
.MODEL ESDM D (IS=1.55E-14 CJO=160fF RS=12 VJ=.58 M=.25 BV=9)
.MODEL ESDS D (IS=1.55E-14 CJO=29fF VJ=.624 M=.571)
**************************************************************************
SPICE MODELS 4.5
```

Appendix A

Package: SO–8

```
* SPICE subcircuit file of coupled
*
* Transmission line model
*
* Conductor number-pin designation
* Conductor Pin
* 1 1
* 2 2
* 3 3
* 4 4
* 5 5
* 6 6
* 7 7
* 8 8
*
* number of lumps: 1
* FASTEST APPLICABLE EDGE RATE:
* COMPRESSION OF SUBCIRCUITS PERFORMED:
* Connect chip side to N**I and board
*
.SUBCKT LINES N01I N01O N02I N02O
+ N05I N05O N06I N06O N07I N07O N08I
L01WB N01I N01M 1.367e-09
L01 N01M N01O 7.794e-10
C01 N01M 0 2.445e-13
L02WB N02I N02M 1.287e-09
L02 N02M N02O 5.473e-10
C02 N02M 0 1.888e-13
L03WB N03I N03M 1.287e-09
L03 N03M N03O 5.473e-10
C03 N03M 0 1.901e-13
L04WB N04I N04M 1.367e-09
L04 N04M N04O 7.723e-10
C04 N04M 0 2.443e-13
L05WB N05I N05M 1.367e-09
L05 N05M N05O 7.710e-10
C05 N05M 0 2.478e-13
L06WB N06I N06M 1.287e-09
L06 N06M N06O 5.489e-10
C06 N06M 0 1.916e-13
L07WB N07I N07M 1.287e-09
L07 N07M N07O 5.495e-10
C07 N07M 0 1.930e-13
L08WB N08I N08M 1.367e-09
L08 N08M N08O 7.786e-10
C08 N08M 0 2.451e-13
K0102 L01 L02 0.1687
K0102WB L01WB L02WB 0.3400
C0102 N01O N02O 3.674e-14
K0103 L01 L03 0.0702
K0103WB L01WB L03WB 0.1847
K0203 L02 L03 0.1822
K0203WB L02WB L03WB 0.3505
C0203 N02O N03O 3.521e-14
K0204 L02 L04 0.0682
K0204WB L02WB L04WB 0.1847
K0304 L03 L04 0.1694
K0304WB L03WB L04WB 0.3400
C0304 N03O N04O 3.675e-14
```

```
K0305WB L03WB L05WB 0.1847
K0405WB L04WB L05WB 0.3455
K0406WB L04WB L06WB 0.1847
K0506 L05 L06 0.1697
K0506WB L05WB L06WB 0.3400
C0506 N05O N06O 3.720e-14
K0507 L05 L07 0.0682
K0507WB L05WB L07WB 0.1847
K0607 L06 L07 0.1824
K0607WB L06WB L07WB 0.3505
C0607 N06O N07O 3.570e-14
K0608 L06 L08 0.0702
K0608WB L06WB L08WB 0.1847
K0708 L07 L08 0.1691
K0708WB L07WB L08WB 0.3400
C0708 N07O N08O 3.632e-14
.ENDS LINES
***************************************************************************
```
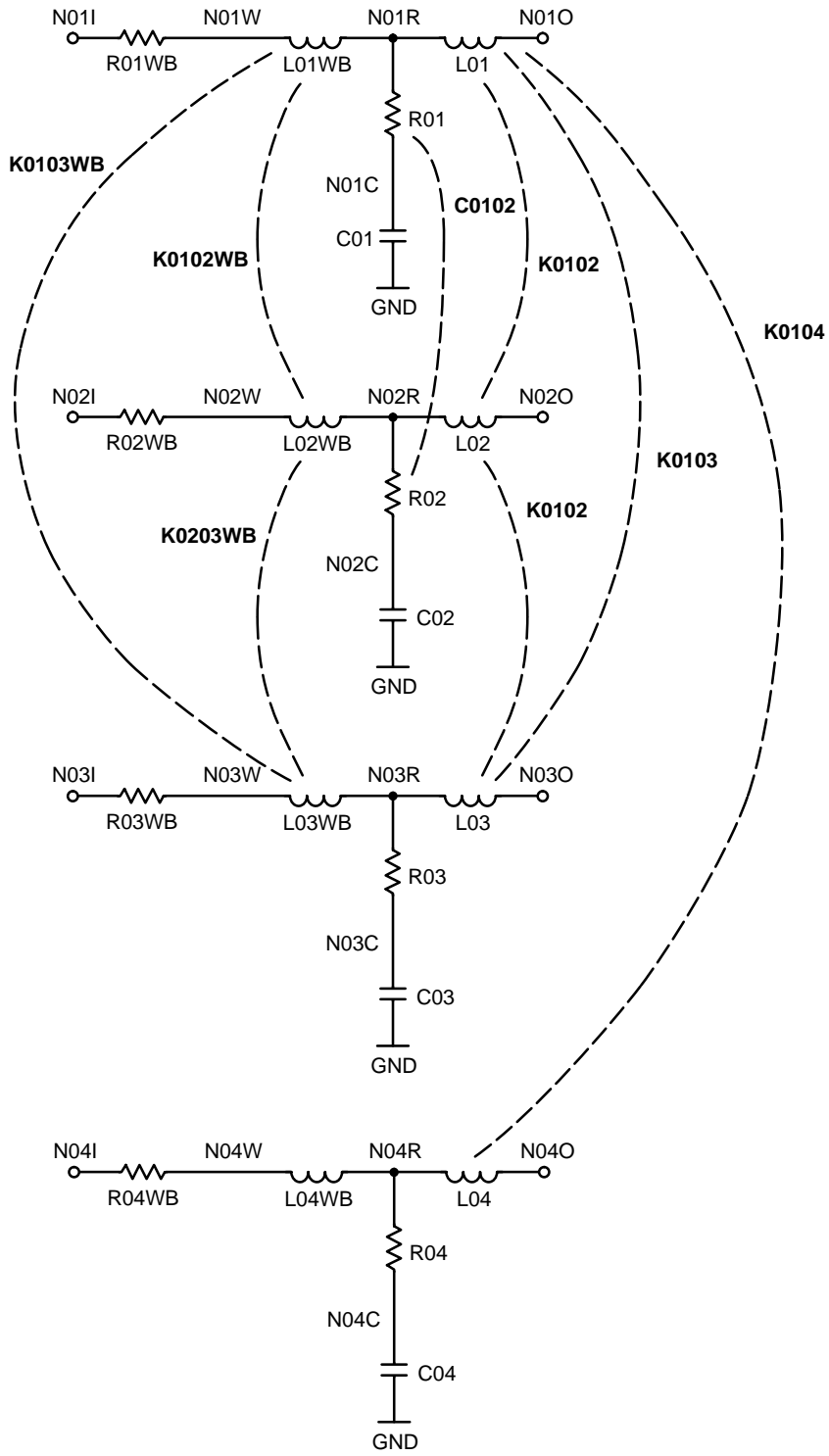
Figure 9.

Appendix B

Package: TSSOP–8

```
* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
* counter-clockwise
* Conductor Pin
* 1 1
* 2 2
* 3 3
* 4 4
* 5 5
* 6 6
* 7 7
* 8 8
*
* number of lumps: 1
* FASTEST APPLICABLE EDGE RATE: 0.048 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
R_SHORT 0 GND 0.0001
*
X_777 N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O GND PACKAGE
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O GND
R01WB N01I N01W 4.727e-02
L01WB N01W N01R 1.158e-09
R01 N01R N01C 9.680e-04
C01 N01C GND 8.978e-14
L01 N01C N01O 7.466e-10
R02WB N02I N02W 3.815e-02
L02WB N02W N02R 9.835e-10
R02 N02R N02C 9.680e-04
C02 N02C GND 7.711e-14
L02 N02C N02O 7.466e-10
R03WB N03I N03W 3.815e-02
L03WB N03W N03R 9.835e-10
R03 N03R N03C 9.680e-04
C03 N03C GND 7.704e-14
L03 N03C N03O 7.465e-10
R04WB N04I N04W 4.727e-02
L04WB N04W N04R 1.158e-09
R04 N04R N04C 9.680e-04
C04 N04C GND 8.983e-14
L04 N04C N04O 7.460e-10
R05WB N05I N05W 4.727e-02
L05WB N05W N05R 1.158e-09
R05 N05R N05C 9.680e-04
C05 N05C GND 8.983e-14
L05 N05C N05O 7.460e-10
R06WB N06I N06W 3.815e-02
L06WB N06W N06R 9.835e-10
R06 N06R N06C 9.680e-04
C06 N06C GND 7.704e-14
L06 N06C N06O 7.465e-10
R07WB N07I N07W 3.815e-02
L07WB N07W N07R 9.835e-10
```

```
R07 N07R N07C 9.680e-04
C07 N07C GND 7.711e-14
L07 N07C N07O 7.466e-10
R08WB N08I N08W 4.727e-02
L08WB N08W N08R 1.158e-09
R08 N08R N08C 9.680e-04
C08 N08C GND 8.978e-14
L08 N08C N08O 7.466e-10
K0102 L01 L02 0.2481
K0102WB L01WB L02WB 0.1729
C0102 N01C N02C 2.283e-14
K0103 L01 L03 0.1067
K0103WB L01WB L03WB 0.0598
K0104 L01 L04 0.0593
K0203 L02 L03 0.2479
K0203WB L02WB L03WB 0.1463
C0203 N02C N03C 2.136e-14
K0204 L02 L04 0.1068
K0204WB L02WB L04WB 0.0598
K0304 L03 L04 0.2481
K0304WB L03WB L04WB 0.1729
C0304 N03C N04C 2.279e-14
K0506 L05 L06 0.2481
K0506WB L05WB L06WB 0.1513
C0506 N05C N06C 2.279e-14
K0507 L05 L07 0.1068
K0507WB L05WB L07WB 0.0615
K0508 L05 L08 0.0593
K0607 L06 L07 0.2479
K0607WB L06WB L07WB 0.1729
C0607 N06C N07C 2.136e-14
K0608 L06 L08 0.1067
K0608WB L06WB L08WB 0.0615
K0708 L07 L08 0.2481
K0708WB L07WB L08WB 0.1513
C0708 N07C N08C 2.283e-14
.ENDS PACKAGE
*****************************************************************************
```

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