AND8081/D

Flip Chip CSP Packages

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APPLICATION NOTE

Introduction to Chip Scale Packaging

This application note provided guidelines for the use of Chip Scale Packages related to mounting devices to a PCB. Included is information on PCB layout for Systems Engineers and manufacturing processes for Manufacturing Process Engineers.

Package Overview

Flip Chip CSP "Package" Overview

Chip Scale Packages offered by ON Semiconductor represent the smallest footprint size since the package is the same size as the die. ON Semiconductor offers several types of CSPs. This application note covers only those with larger solder bumps.

Flip Chip CSP bumped die are created by attaching solder spheres to the I/O pads of the active side of the wafer. The I/O layout may be either in peripheral or array format. A redistribution layer may be used to reroute the device pads to the bump pads.

Solder bumps allow compatibility of the package connections with standard surface mount technology pick and place and reflow processes and standard flip chip mounting systems. The larger solder bumps of the Flip Chip CSP require no underfill for increased reliability performance. Solder bumps are primarily Pb−free however eutectic SnPb solder is available.

Devices designed with smaller bumps generally have a peripheral pad layout and tighter spacing. In this case, underfill is recommended to improve board level solder joint reliability.

Package Construction and Process Description

Flip Chip CSPs are created at the wafer level. Upon completion of standard wafer processing, a polymeric Repassivation layer is applied to the wafer, leaving the bonding pads exposed. In the case where bumps are formed directly over the device bonding pads (Bump on I/O), an under bump metallization (UBM)is applied to the bonding pads to provide an interface between the die pad metallization and the solder bump. The UBM may be a sputtered AlNiVCu thin film or an electroplate Cu. In the case where the solder bumps are offset from the device bonding pads, a plated RDL trace is applied to connect the device bonding pad to the UBM. Solder spheres are placed on each exposed UBM pad and reflowed to create an interconnection system ready for board assembly.

Once the bumps are reflowed, wafers are laser marked, electrically tested, sawn into individual die, and packed in tape and reel, bumps down. A typical Flip Chip CSP is represented in **Figure 1**. Total device thickness varies, depending on customer requirements.

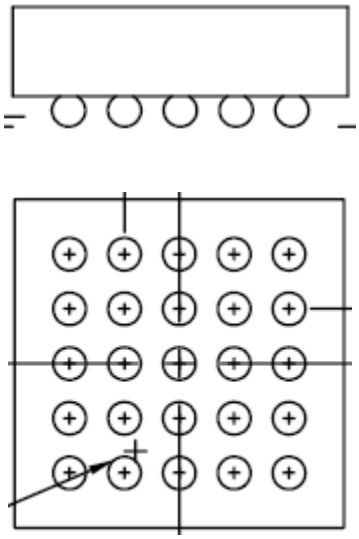


Figure 1. Daisy Chain Flip Chip CSP

Printed Circuit Board Design

Recommended PCB Layout

Two types of land patterns are used for surface mount packages − non−solder mask defined (NSMD) and solder mask defined (SMD), as shown in Figure 2. For SMD configured pads, the solder mask covers the outsider perimeter of the circular contact pads, thus limiting the solder connection to only the top surface of the exposed pads. For NSMD pads, the solder mask opening is larger than the contact pad, leaving a gap between the solder mask and Cu pad. NSMD pads are preferred due to better dimensional control of the copper etch process as compared with the solder mask etch process. The solder bumps adhere

to the NSMD pad wall as the pad surface, providing additional mechanical strength and solder joint fatigue life. SMD pad definition introduces increased levels of stress near the solder mask overlap region which may result in solder joint fatigue cracking in extreme temperature cycling conditions. The smaller NSMD pads also provide more room for escape routing on the PCB since they can be smaller diameter than the SMD pads.

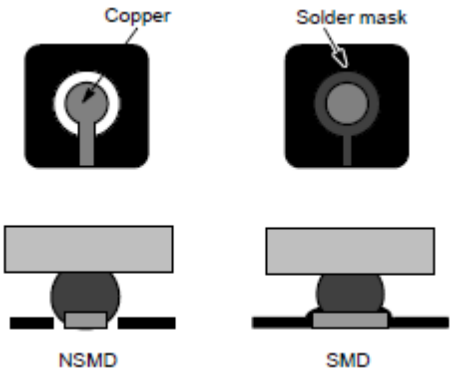


Figure 2. NSMD vs. SMD Pads

A copper layer thickness of less than 1 oz (30 μm) is recommended to maintain a maximum stand−off height for maximum solder joint fatigue life.

Micro−via pads should be NSMD to ensure adequate wetting area of the copper pad.

Corner traces should approach outer pads either laterally or perpendicularly, not diagonally.

A summary of recommended design parameters is found in Table 1.

Table 1. PCB ASSEMBLY RECOMMENDATIONS

Parameter	500 μm Pitch 300 μm Solder Sphere	400 μm Pitch 250 μm Solder Sphere	400 μm Pitch 200 μm Solder Sphere
PCB Pad Size	250 μm + 25 − 0	229 μm + 25 − 0	229 μm + 25 − 0
Pad Shape	Round	Round	Round
Pad Type	NSMD	NSMD	NSMD
Solder Mask Opening	350 μm ± 25	305 ± 25	305 ± 25
Solder Stencil Thickness	125 μm	100 μm	100 μm
Stencil Aperture	250 x 250 μm	200 x 200 μm	200 x 200 μm
Solder Flux Ratio	50/50	50/50	50/50
Solder Paste Type	No Clean Type 4 or Finer	No Clean Type 5	No Clean Type 5
Trace Finish	OSP Cu or NiAu	OSP Cu or NiAu	OSP Cu or NiAu
Trace Width	150 μm max	100 − 125 μm	100 − 125 μm

PCB I/O Contacts Surface Finish Characteristics

Organic Solderability preservative (OSP) Cu or electroless nickel immersion gold pad finish can be used. The Au thickness should not exceed 0.127 μm to minimize formation of brittle AuSn intermetallics which may compromise solder joint integrity. HASL (Hot Air Solder Leveled) finish is not recommended due to inconsistent solder volume deposition on each pad.

Solder Assembly Recommendations

SMT Process Flow

Surface mount assembly operations include printing solder paste onto the PCB.

Solder Paste Characteristics

Type 5 (15 − 25 μm powder) ANSI/J−STD−005 compliant solder paste is suggested. No clean solder paste is recommended. Metal loading is about 88.5 wt%.

Solder Stencil and Printing

Stencils should be laser cut with an electro−polished finish. Stencil thickness and recommended opening sizes are given in Table 1. Solder paste height, uniformity, registration and proper placement should be monitored.

Package Placement

Standard pick and place machines can be used for placing CSPs. Such placement equipment falls into two categories:

a vision system to locate the package silhouette commonly known as a chip shooter, or a fine pitch vision system to locate individual bumps. It is preferable to use vision systems employing solder bump recognition for improved placement accuracy, although throughput is reduced. Little or no force should be exerted on the CSP during placement.

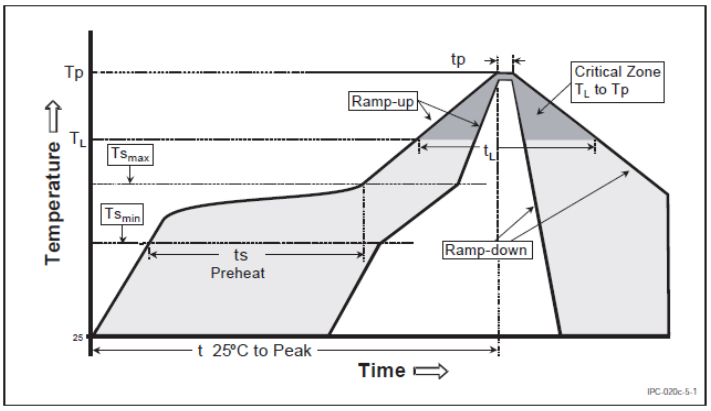
Solder Paste Reflow and Cleaning

When cleaning a No−clean or RMA flux residue, semi−aqueous solvents, saponified water, alcohols and other CFC−free alternatives may be used to sufficiently remove all residue. If cleaning a water soluble flux residue, spray and immersion should be sufficient to remove all ionic contamination and residue.

IR Reflow Profile

Pb−Free CSPs are compatible with the recommended Pb−Free reflow profile found in JEDEC J−STD−020. An optimized profile should be determined using the solder paste manufacturer's recommendations.

Pb−Free CSPs should not be reflowed in conjunction with eutectic SnPb solder paste as this will compromise board level reliability.



Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	20-40 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

Figure 3. Typical Reflow Profile for Pb−Free Solder (J−STD−020C)

Solder Joint Inspection

Inspection of solder joints is commonly performed with an x−ray inspection system. The x−ray system is used to locate open contacts, shorts between pads, solder voids, and extraneous solder. A cross section of a typical flip chip solder joint is shown below in Figure 4.

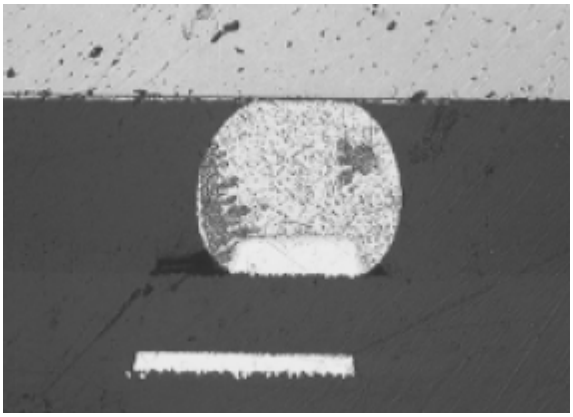


Figure 4. Cross Section of Flip Chip Solder Bump

Underfill

Underfill is not required for Flip Chip devices constructed with solder spheres 200 μm or larger. Solder joint reliability tests have shown parts to pass temperature cycling tests without the need for further encapsulation. These devices can, however, withstand dispense of an underfill as long as the process temperature does not exceed 175°C for up to 5 minutes.

Rework Process

The rework procedure is similar to that used for most BGAs and CSPs. Key steps include:

1. CSP removal uses localized heating which duplicates the original reflow profile used for assembly.
2. The reject CSP can be removed once the temperature exceeds the liquidus temperature of the solder.
3. Additional solder paste should be applied to the cleaned pads prior to component placement.
4. A new part is picked up using a vacuum needle pick−up tip and placed onto the board.
5. The replacement part is reflowed to the board using the same reflow profile as used in assembly. The reflow process should include localized convection heating and pre−heat from the bottom.

ON Semiconductor CSP Reliability Test Data

Board Level CSP Package Reliability

ON Semiconductor performed solder joint fatigue testing on Flip Chip CSP daisy chain structures per IPC−SM−785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments. The test vehicle is a 5 x 5 array of solder bumps, spaced at pitches of 0.5 mm or 0.4 mm. Devices were assembled with Type 5 SAC305 solder paste to 0.032” thick 4−layer high temperature FR4 test boards designed with NiAu NSMD pads. Boards were temperature cycled from −40°C to 125°C (about 2 cycles / hr) and continuously monitored for changes in resistance. The temperature cycling profile is found in Figure 5 below. Table 2 summarizes some daisy chain CSP solder joint reliability tests.

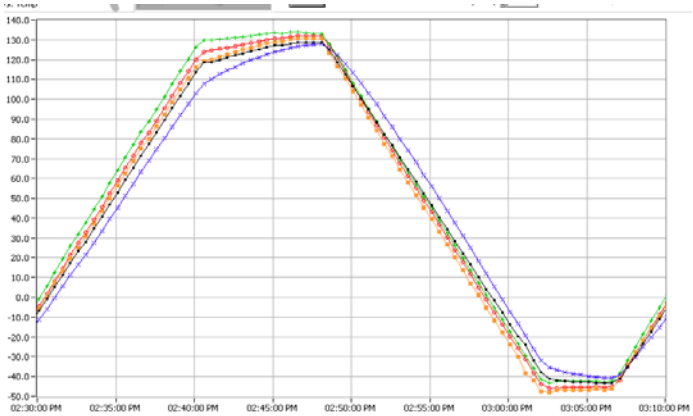


Figure 5. Typical Temperature Cycling Profile for Solder Joint Fatigue Testing

Test results show that first failure for both the 400 μm and 500 μm pitch 5 x 5 daisy chain arrays is greater than 1000 cycles. A Weibull Plot of the solder joint fatigue data for these daisy chain devices is shown below in Figure 6.

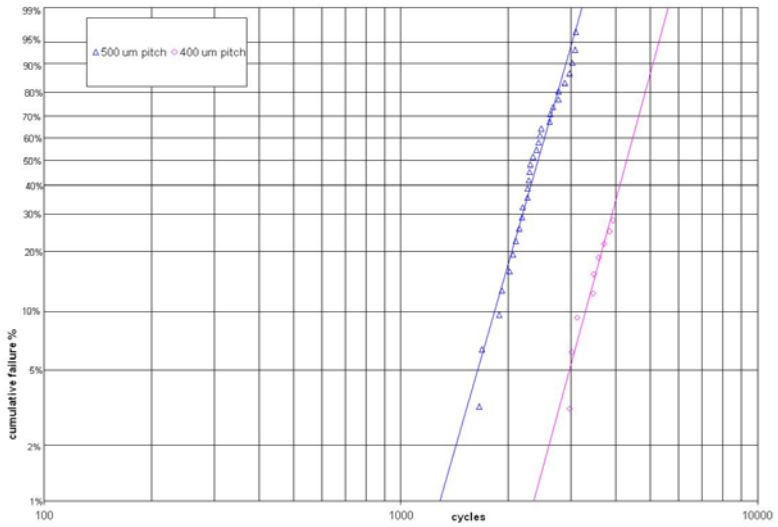


Figure 6. Weibull Plot of 400 μm/500 μm Pitch Daisy Chain Device Cumulative Temp Cycle Failure Rate

Tape and Reel Specifications and Labeling Description

All Flip Chip CSPs are shipped in tape and reel compliant with industrial standard EIA−481 and per ON Semiconductor Tape and Reel Packaging Specification document BRD8011−D. Tape and reel construction is given in Figure 7 below.

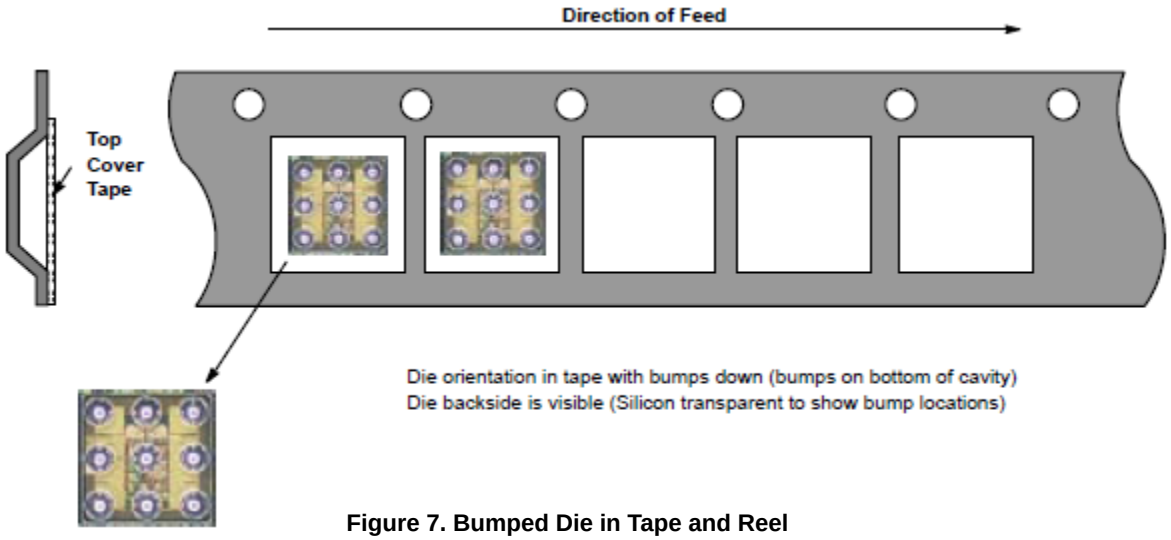


Figure 7. Bumped Die in Tape and Reel

The SMD pick and place machines should pick up the component from the point which is located in the center of two adjacent sprocket holes in the feeding direction. This must be taken into account when designing the location of the component in the Tape and Reel pocket.

Tape Material: Embossed (ie. blister)

Reel Size: Standard reel diameter is 7 inches (178 mm) for all 8 mm tape

Reel material: Plastic

Device Orientation: Pin 1 placed closest to sprocket holes

The cavity is designed to provide sufficient clearance surrounding the component so that:

1. The part does not protrude beyond either surface of the carrier tape.
2. The part can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed.
3. Rotation of the part is limited to 20° maximum.
4. Lateral movement of the part is restricted to 0.05 mm maximum.

Tape with or without parts shall pass around radium R without damage.

Barcode labeling (if required) shall be on the side of the reel opposite the sprocket holes.

PUBLICATION ORDERING INFORMATION

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