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Introduction

The intent of this document is to shed light on the accuracy one can expect to obtain with a given design. All of the error components and their relationship to the overall accuracy of the system are laid out for the user to see and understand. These errors are both random (independent statistically) and

To do this, we must generate the basics behind the design and then identify the error components.

The following block diagram in Figure 1 shows all of the components that contribute error to the output voltage of the converter:

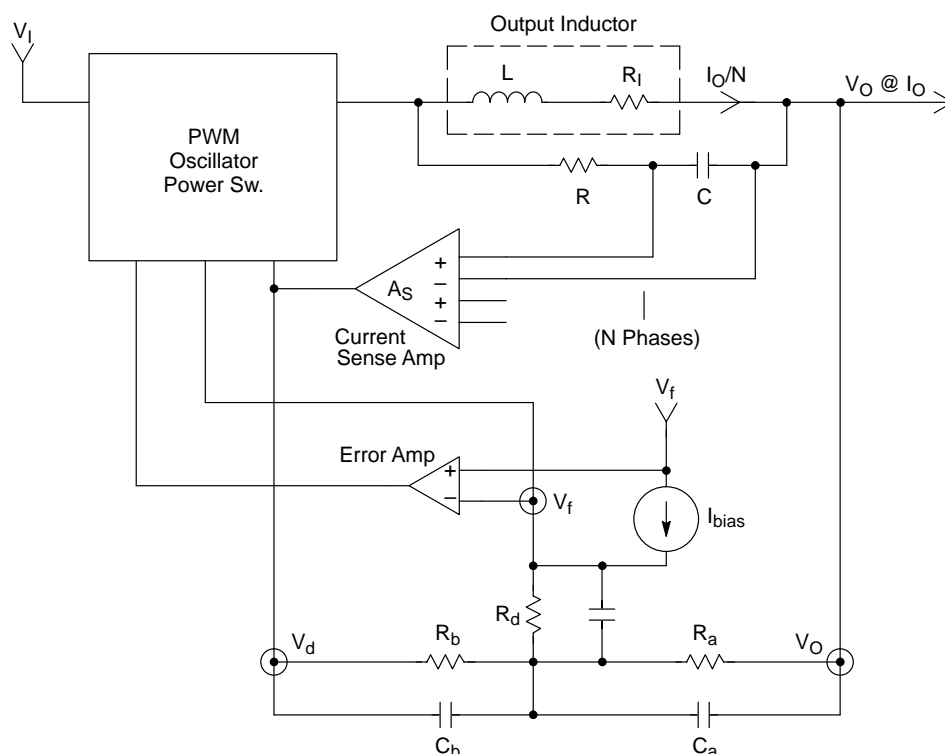


Figure 1. Block Diagram of Enhanced System

The output voltage of the converter is given by the following relationship in terms of the factors in Figure 1. Each factor is also described.

$$V_o = V_f - I_b(R_a + R'_d) - \frac{R_a(1 + sC_bR_b)}{R_b(1 + sC_aR_a)} V_d$$

$$V_d = I_o A_s R_l \frac{(1 + s \frac{L}{R_l})}{(1 + sCR)} + V_{os}$$

$$R'_d = R_d \left(1 + \frac{R_a}{R_b}\right)$$

- I_b – Feedback Bias Current
- V_f – Feedback Voltage DAC/Offset Set Point
- V_i – Input Voltage
- V_o – Output Voltage
- V_d – Current Sense Amp Output Voltage
- V_{os} – Current Sense Amp Output Offset Voltage
- R_l – Inductor Resistance
- A_s – Current Sense Amplifier Gain
- I_o – Output Load Current
- N – Number of Phases

Another error factor to take into account is the output ripple, which is given by the following:

$$V_r = \frac{V_o}{(2f_s L)} \cdot \left(1 - \frac{NV_o}{V_i}\right) \cdot |Z_o(\omega = 2\pi Nf_s)|$$

$|Z_o(\omega = 2\pi Nf_s)|$ – Output impedance of output capacitors at output ripple frequency.

Thus, combining all of the factors together, we get the following expression for the overall output voltage:

$$\therefore V_o = V_f + V_r - I_b(R_a + R'_d) - \frac{R_a}{R_b} V_{os} - I_o A_s R_l \frac{R_a(1 + sC_bR_b)}{R_b(1 + sC_aR_a)} \frac{(1 + s \frac{L}{R_l})}{(1 + sCR)}$$

Let's define the design's output droop impedance (R_{oa}) as follows:

$$R_{oa} = A_s R_l \frac{R_a(1 + sC_bR_b)}{R_b(1 + sC_aR_a)} \frac{(1 + s \frac{L}{R_l})}{(1 + sCR)}$$

$$\therefore V_o = V_f + V_r - I_b(R_a + R'_d) - \frac{R_a}{R_b} V_{os} - I_o R_{oa}$$

$$\text{Let } C_b R_b = CR \text{ and } \frac{L}{R_l} = C_a R_a.$$

$$R_{oa}(\text{static}) = A_s R_l \frac{R_a}{R_b}$$

$$R_{oa}(\text{dynamic}) = A_s \frac{C_b}{C_a} \frac{L}{CR}$$

Notice that R_{oa} is dependent on different factors depending on if the output is static or dynamic. The static value will determine the set point of the output load line based on the average output load current (I_o) and the dynamic value determines how the output load line tracks changing output currents (ΔI_o). More on this impact to the accuracy of the output later. First we must introduce the load line and its associated parameters.

Output Load Line

Figure 2 shows a typical load line and the design parameters that describe it. It is this load line that one designs to and it is specified for the design:

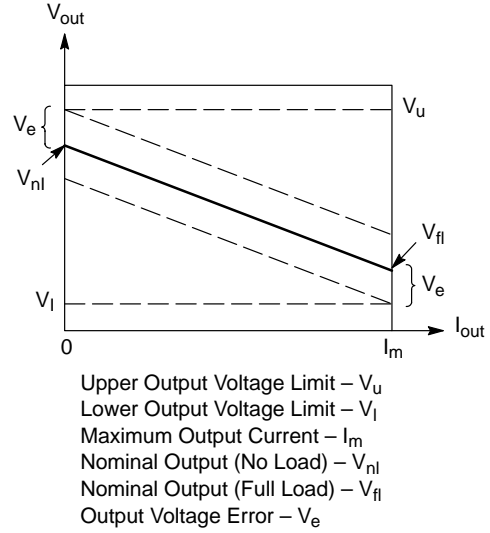


Figure 2. Output Load Line Characteristics

One needs to determine the load line characteristics based on the platform. Then the following terms can be computed:

$$\begin{aligned} V_{out}(\text{loadline}) &= V_{nl} - I_{out} R_o \\ V_e &= V_u - V_{nl} = V_{fl} - V_l \\ V_d &= V_{nl} - V_{fl} \\ R_o &= \frac{V_d}{I_m} \\ \text{Droop voltage} &= V_d \\ \text{Droop resistance} &= R_o \end{aligned}$$

Before proceeding, let's define a new function called the error load line:

$$\begin{aligned} V_{err} &= V_{out}(\text{loadline}) - V_o \\ &= (V_{nl} - V_f - I_b(R_a + R'_d) - \frac{R_a}{R_b} V_{os}) \\ &\quad - I_o(R_o - R_{oa}) + V_r \end{aligned}$$

From this expression, we can see there is a term dependent on output current and one that is not, as well as the ripple term. Let's analyze the constant term in more detail. The components of the initial set point error (constant term) are as follows:

$$\begin{aligned} \varepsilon_{vf} V_f &\quad - \text{Feedback Voltage DAC Set Point Error} \\ \varepsilon_{ib} I_b (R'_d + R_a) &\quad - \text{Feedback Bias Current Error} \\ \varepsilon_{ra} I_b (R'_d + R_a) &\quad - \text{Resistor (a) Error} \\ \varepsilon_{rd} I_b (R'_d + R_a) &\quad - \text{Resistor (d) Error} \\ \frac{R_a}{R_b} V_{os} &\quad - \text{VDRP Offset Error} \end{aligned}$$

Thus, we can define the no load error voltage as follows:

$$V_{nlerr} = \sqrt{(\varepsilon_{vf} V_f)^2 + (\varepsilon_{ib}^2 + \varepsilon_{ra}^2 + \varepsilon_{rd}^2) I_b^2 (R_a + R_d)^2 + \left(\frac{R_a}{R_b} V_{os}\right)^2}$$

For the current dependent component, there are both static and dynamic errors. The static and dynamic droop resistance errors are described below (subscript on each error describes source of error).

NOTE:

Since the current information is summed over all phases, errors associated with components that are used on a per phase basis will be statistically reduced by the number of phases. These components are A_s , L , R_l , R and C . This factor is included in the following expressions, where N is the number of phases.

$$\Delta R_O (\text{static}) = \sqrt{\left(\frac{\epsilon_{as}^2}{N} + \frac{\epsilon_{rl}^2}{N} + \epsilon_{ra}^2 + \epsilon_{rb}^2\right)} \cdot R_{Oa}(\text{static}) + \epsilon_{rlt}(T)R_{Oa}(\text{static})$$

$$\Delta R_O (\text{dynamic}) = \sqrt{\left(\frac{\epsilon_{as}^2}{N} + \epsilon_{cb}^2 + \epsilon_{ca}^2 + \frac{\epsilon_l^2}{N} + \frac{\epsilon_c^2}{N} + \frac{\epsilon_r^2}{N}\right)} \cdot R_{Oa}(\text{dynamic})$$

The $\epsilon_{rlt}(T)$ term describes the temperature dependent function of the droop resistance (this will be analyzed later).

The error anywhere on the load line as a function of current depends on the static level you are at and the dynamic current step that got you there. The current step size is a function of where you started at and ended up. Based on never exceeding the maximum ($I_{cc \text{ max}}$) or minimum ($I_{cc \text{ stop-grant}}$), one can statistically describe the current step size as a function of these two parameters as follows:

$$\Delta I_O = 0.7(I_{cc \text{ max}} - I_{cc \text{ stopgrant}})$$

Thus, the error associated with the dynamic response of the system is basically independent of the static load current and can be given as:

$$V_{erodyn} = \Delta I_O \Delta R_O (\text{dynamic})$$

The static error term depends on the output current and is described as follows:

$$V_{erosta} = I_O \Delta R_O (\text{static})$$

Determining Temperature Dependence Function

To analyze the temperature dependence of the design, we must first introduce a thermistor to compensate for the temperature dependent change of the inductor's resistance R_l . Figure 3 shows the design, which is to make R_a become an NTC based resistor with the same magnitude TC as copper:

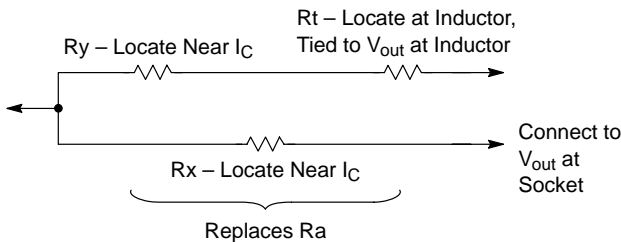


Figure 3. R_a Replacement for Inductor Temperature Compensation

In this design, R_t is an NTC thermistor, which is typically non-linear. The parallel combination of all three resistors is used to produce a value for R_a that is nominally the correct value for the overall design at room temp and to have the same but opposite in sign TC as the copper wire of the inductor. The following expression shows the interaction of the temperature dependent components on the droop resistance:

$$R_{Oa} = (R_l R_a) \frac{(1 + s \frac{L}{R_l})}{(1 + s C_a R_a)} \frac{A_s (1 + s C_b R_b)}{R_b (1 + s C R)}$$

$$\frac{L}{R_l} = C_a R_a \Rightarrow (R_l R_a) = \frac{L}{C_a}$$

$$R_l R_a = R_{l0} (1 + \rho_l \Delta T) R_{a0} (1 - \rho_a \Delta T)$$

$$\approx R_{l0} R_{a0} [1 + (\rho_l - \rho_a) \Delta T]$$

Testing has shown that this method of compensation tracks temperature changes to within $\pm 20\%$ of actual.

Assuming:

1. The inductors ΔT maximum is $\pm 50^\circ\text{C}$ over all ambient and operating conditions.
2. The TC of annealed copper wire is $0.00383\%/^\circ\text{C}$.
3. The temperature compensation is good to $\pm 20\%$ and statistically random.

We can conclude the error factor $\epsilon_{rlt}(T) = \epsilon_{rt} = \pm 4\%$. The correct expression now for $\Delta R_O(\text{static})$ would be, where ϵ_{rao} is the initial error associated with R_a :

$$\Delta R_O (\text{static}) =$$

$$\sqrt{\left(\frac{\epsilon_{as}^2}{N} + \frac{\epsilon_{rl}^2}{N} + \epsilon_{rao}^2 + \epsilon_{rb}^2 + \epsilon_{rt}^2\right)} R_O (\text{static})$$

A side affect of this method of compensation is on the no load set point, since it is a function of $(R'_d + R_a)$.

$$R_{nl} = R'_d + R_a = R'_d + R_{ao} (1 - \rho_a \Delta T)$$

$$= (R'_d + R_{ao}) \left(1 - \frac{R_{ao}}{(R'_d + R_{ao})} \rho_a \Delta T\right)$$

We can generate an error term for R_{nl} based on the change in R_a and the error associated with R'_d (each being statistically random). Based on our assumptions, the term $\rho_a \Delta T = \pm 0.19$ and:

$$\epsilon_{rat} = \frac{R_{ao}}{(R'_d + R_{ao})} \rho_a \Delta T \text{ and } \epsilon_{rd} = \frac{R'_d}{(R'_d + R_{ao})} \epsilon_{rdo}$$

The expression for the no load error now becomes:

$$V_{nlerr} = \sqrt{(\epsilon_{vf} V_f)^2 + (\epsilon_{ib}^2 + \epsilon_{rao}^2 + \epsilon_{rat}^2 + \epsilon_{rd}^2) I_b^2 (R'_d + R_a)^2 + \left(\frac{R_a}{R_b} V_{os}\right)^2}$$

Determining Overall System Error

The overall error function for the output can now be generated from all of the previous terms to yield the following:

$$V_{err} = V_r + \sqrt{V_{eronl}^2 + V_{erodyn}^2 + V_{erosta}^2}$$

All of the related factors involved for performing the calculation of the system error are described throughout this document. A spreadsheet for performing the system design and indicating the error associated with it has been created

for assisting in determining the error of the system. The following design example will demonstrate the results of a particular design.

Design Example

Using the CS5323, a design for the Willamette FMB is produced. The spreadsheet shown in Figure 5 shows the load line requirements, the parameters and errors associated with the controller, and the design values for the components used in conjunction with the controller.

Multiphase VR Design: C95323/C95323		C95323 Parameters:		High Frequency Capacitor:	
Enter VID Voltage:	1.75	Current Sense to Vdip Gain:	3.1	Rh=	0.0015
Enter No Load Voltage:	1.726	Current Sense to Vdip Error:	0.12	Lh=	7.14286E-11
Enter Full Load Voltage:	1.836	Feedback Bias Current:	1.79E-05	High=	3343940.045
Enter Full Load Current:	60	Feedback Bias Current Error:	0.06	Enter ESR:	0.03
Enter Stop Grant Current:	70	Feedback DAC Output Error:	0.008	Enter ESL:	2.00E-08
Enter Output Error Voltage:	0.025	Vdip Output Offset Voltage:	0.02	Minimum # of Capacitors:	28
Droop Resistance:	0.0015			Enter Capacitance:	1.00E-06
Enter Input Voltage:	12			Enter number used:	38
Enter Slew Rate (A/us):	350	External Component Errors:		Bulk Capacitor:	
Maximum Switching Frequency:	291696.6667	Standard Resistor Tolerance:	0.01	Controller Upper f1 Limit:	1.20E+05
Enter Switching Frequency:	240000	Standard Capacitor Tolerance:	0.1	High Freq. Cap. Lower 3dB:	5.31E+05
Rosc=	55933.33333			Enter ESR:	0.005
		Inductor Related Factors:		Enter ESL:	5.00E-08
CR<=	0.000346017	Inductor Initial Resistance Error:	0.05	Enter Capacitance:	5.60E-04
Enter R:	24300	Inductance Error:	0.1	Rbulk Total:	1.96E-03
C<=	1.42354E-08	Inductor Total Temp Change:	100	Lbulk Total:	6.61E-10
Enter C:	2.20E-08	Inductor Temp Tracking Error:	0.2	Minimum # of Capacitors:	8
		Ra Temp Tracking Error:	0.0383		
0.0008 < Rl <	4.21E-03	Initial Ra Error:	0.02	Controller Comp Capacitors:	
Enter Rl (at room temp):	0.0024	Ra Temp Change Error:	0.1915	Enter Cm:	4.00E-08
Enter L:	5.50E-07	Rd Error:	0	C1:	2.02E-08
		Ro Static Error (ohm):	0.00013	C2:	1.96E-06
Rnl=	1.34E+03	Ro Dynamic Error (ohm):	0.00027	Output Current Limit:	
Rb=	6.30E+03			Enter Current Limit:	90
Enter Ra:	1270	Output Voltage Errors:		lim Voltage:	1.728
Actual No Load Voltage:	1.7273E+00	Output Independent Error:	15.31	Enter Rm:	1500
Enter Rb:	6340	Output Dynamic Error:	9.3173	Rn:	1364.583333
Actual Full Load Voltage:	1.6378E+00	Output Ripple (peak):	4.80		
Ca=	1.804E-07				
Cb=	8.43E-08				

Figure 4. Design Example Spreadsheet

Figure 5 shows the circuit and Figure 6 shows the output error values as well as the design target and actual errors graphically.

AND8071/D

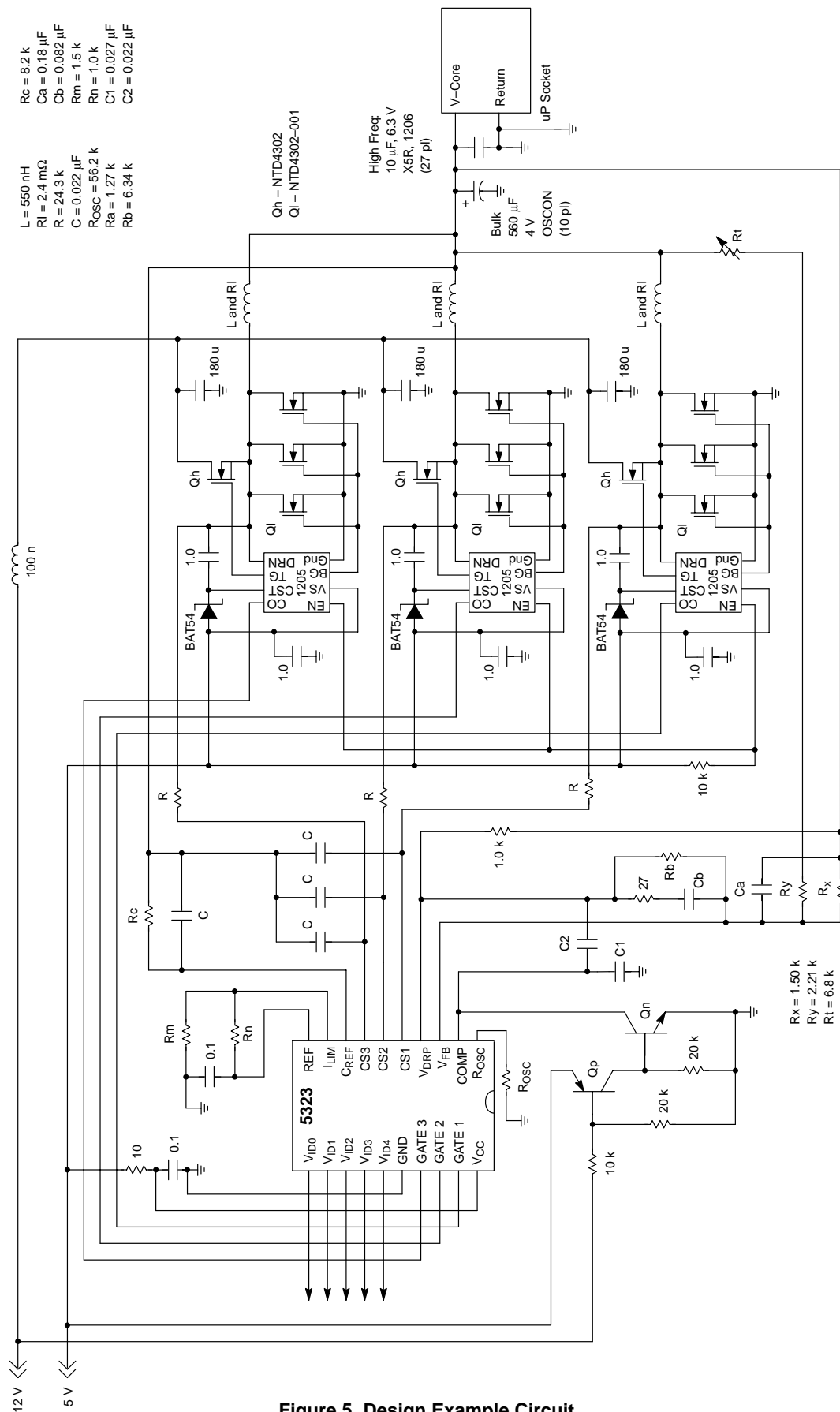
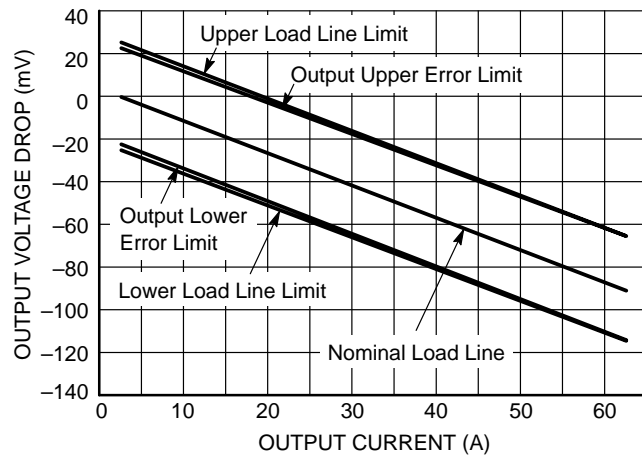


Figure 5. Design Example Circuit



CURRENT	STATIC ERROR	ERROR
0	0	22.72
5	0.65	23.73
10	1.31	22.77
15	1.96	22.83
20	2.62	22.91
25	3.27	23.02
30	3.92	23.15
35	4.58	23.30
40	5.23	23.47
45	5.88	23.66
50	6.54	23.88
55	7.19	24.11
60	7.85	24.36

Figure 6. Design Example Output Error

It can be seen that the system design meets or exceeds the error requirements for the design.


Design Assistance

A free design assistance spreadsheet is available on our website at:

<http://www.onsemi.com/pub/Collateral/CS53X3DESIGN.XLS>

Notes

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