A Comparison of Key Parametrics of CMOS and Bipolar Integrated Circuits In Line Driver Applications

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APPLICATION NOTE

INTRODUCTION

CMOS has the reputation, among system designers, as a low power technology; whereas, Bipolar ECL is considered a power hog. However, many low power CMOS devices consume many watts, and many ECL devices consume much less than one watt. This paper addresses devices in CMOS and ECL technology that can be used for similar purposes and compares the differences in speed, power, and other relevant specifications.

CMOS started its life as a low power alternative to high density ICs for the watch and calculator industry. Operating at 5 V and less than 1 MHz, CMOS was near zero power. Indeed, the structure was created using a P–channel device as a load resistor and an active N channel. With this structure, power was consumed only during transition and with clock rates at just a few hundred kilohertz, power was nearly zero. In contrast, the ECL used a bipolar differential circuit whereby speed was achieved by keeping its transistors out of saturation. By the early 1970s, CMOS speeds were about 10 MHz, while ECL could operate at nearly 1 GHz.

Notwithstanding a few unique applications, CMOS is the only viable technology for building high–density devices. Microprocessors, memories, ASICs, and ASSPs are nearly all CMOS. However, there is still room for optimal performance using “mix and match” technologies. For example, in I/O structures, density is not the critical factor and ultra–small geometry is not necessarily the key to improved performance.

According to Insight Onsite, 5.0 V logic represented as much as 75% of all logic sold in 1999. Since all very small geometry devices must run at less than 5.0 V, it appears that the real world is far behind the leading–edge technology. Many CMOS output drivers can drive from 24 – 64 mA. The need for such high drive lies with the very low impedance of bus lines and the quest for speed.

Achieving speed depends on several factors. A signal propagates across a board at the speed of light. If the board is fabricated from a standard material like glass–epoxy, the speed is 5 – 6 ns/m. It takes approximately 2 ns to propagate a signal across a board a distance of 0.33 m. A very fast CMOS IC might switch in 2 ns; therefore, a total of 4 ns are lost waiting for the signal to get to the device and switch it on. If a designer was trying to use this trace as part of a backplane operating at 100 MHz, nearly half a time slot will be used to deliver the signal to its target IC and switch it on. In actuality, running a backplane–bus at 100 MHz is quite difficult. It is easier, but more costly, to widen the bus.

A CMOS IC input at the end of a 0.33 m transmission line constitutes a nominal 5 – 10 pf capacitor termination. Transmission line theory shows a signal will travel back and forth down the line, creating overshoot and undershoot. Since a CMOS input signal must be monotonic, a termination resistance must be placed on the trace to prevent ringing. With standard printed circuit techniques, Blood [1] shows the characteristic impedance of a line is between 40 – 120 Ω. A single resistor of 100 Ω can be placed in parallel to the input of the receiving IC; thus, terminating the line in its assumed characteristic impedance. If the supply voltage is 5.0 V and the saturation voltage of an output device is assumed to be 0.5 V, the current in the driving devices is 45 mA. This implies greater than 100 mW of power dissipation per trace, assuming a 50% duty cycle. A 64–bit bus would draw a whopping 6 watts, just to terminate the lines.

Forstner and Huchzemeier report that a backplane looks like a transmission line with many capacitive loads across it. The characteristic impedance of the line may drop by a factor of 5 or more (e.g., from 100 Ω to 20 Ω). Matching a 20 Ω, 64–bit bus requires peak current of greater than 200 mA per line or a nearly 13 A peak. Operating from a 5.0 V supply with a 50% duty cycle, the average power is 30 W. It becomes obvious from this discussion that CMOS is not necessarily a low–power technology, and in fact, neither standard CMOS nor BiCMOS is very efficient for driving high speed, rail–to–rail busses.

Shrinking the device geometry has little effect on the overall die size in many driver devices. Device size is determined by pad pitch, ESD structures, and the very large devices needed for high drive. Typical input loading is 10 pf or more, irrespective of any internal geometry, owing to the ESD structure of the device, and the board and connector construction. Several bus solutions have recently become available, all operating from lower voltage and with smaller swing than standard TTL/CMOS, to reduce the power from 30 W.

There are two relatively new CMOS I/O structures contending for bus driver applications. The first is Gunning Transistor Logic (GTL). This output was created several years ago to limit the power in an output stage. GTL uses a comparator input that requires a small voltage swing. A standard CMOS input, operating at 3.3 V, has an input voltage requirement of +2.0 V for a high and 0.8 V for a low. The input is replaced with a high–speed comparator, requiring only a few hundred millivolts of swing. The output driver is an open drain tied to a voltage less than Vcc. The output swing is reduced along with output power. Typical values for the output terminating voltage range between 1.2 and 1.5 V. The reference voltage of the comparator is typically one–third the supply voltage (or 1.0 V). Figure 1 shows the circuit. The low supply voltage is 1.5 V and Vref is 1.0 V +/–250 mV of threshold. The terminating resistor can be as low as 20 Ω and still achieve reasonable power dissipation.

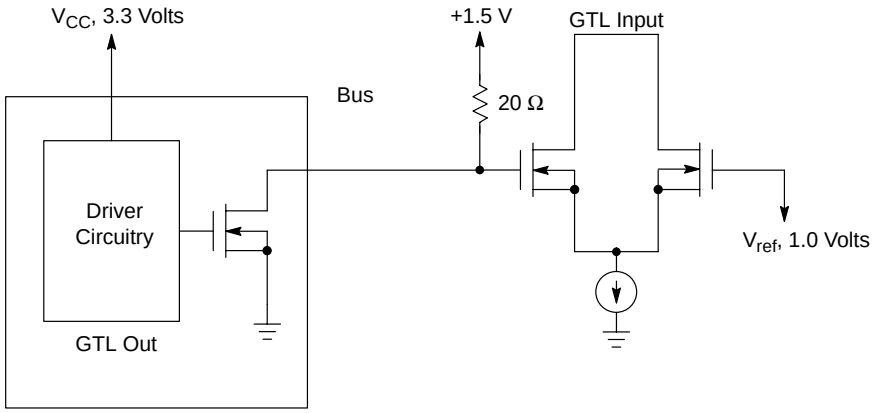

Figure 1. Circuit Diagram

In this configuration, the output current is approximately 50 mA, but the power supplied to the resistor is now only 37 mW, assuming 50% duty cycle. Thus, a 64–bit bus only consumes 2.4 W. GTL provides a rather easy way to reduce power consumption, while at the same time, matching transmission line impedance. The downside risk is noise immunity. With only +/–250 mV swing, the system has a much lower noise margin than TTL or CMOS. In order to overcome the noise immunity issues, a differential bus may be used.

In a differential or “balanced” bus, any noise picked up on one wire will usually be picked up on the second one, and the common mode rejection at the input will cancel much of the noise. ECL has been available as an option to the designer and high noise/high–speed environments have used this technology extensively. A newer technique developed in the 1990s uses CMOS devices in a differential mode. EIA–644 calls for a Low Voltage Differential Signal (LVDS). This specification, neither CMOS nor ECL, is a reference document similar to RS–422, for voltage levels.

When implemented in CMOS, LVDS outputs look like open–drain differential devices driven by a current source (Figure 2). The input looks like GTL input with both inputs being fed. The EIA–644 specification calls for 400 mV of differential swing at the output and the input capable of switching with 100 mV of swing. The terminating resistor R is usually supplied externally by the system designer so a value can be selected that matches the transmission line used. In practice, the LVDS driver is limited to ~4 mA from its current source, which limits the power dissipation in the output stage to about 13 mW. As seen previously for a backplane, 100 Ω is not a reasonable figure. A newer specification, called Bus–LVDS (BLVDS), has been developed to try to accommodate the very low impedance encountered on a backplane. With differential I/Os, BLVDS looks very similar to ECL.

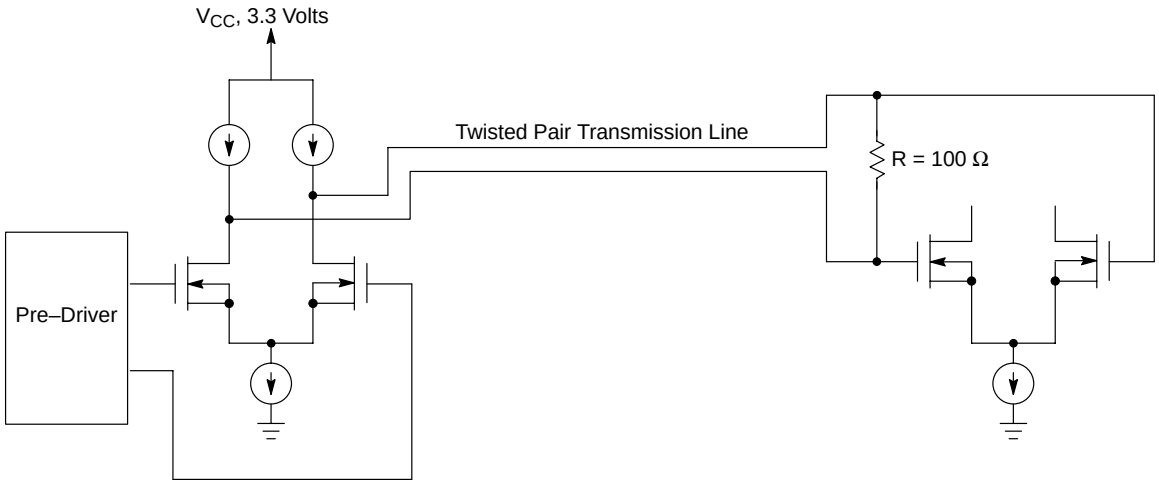

Figure 2. CMOS LVDS

ECL, by its very structure, is differential and the swing is generally +/–800 mV, about twice that of LVDS. Larger swing improves noise immunity, and unlike CMOS LVDS, voltage swing is not achieved at the expense of device power. ECL circuits are low impedance voltage sources driven from emitter followers. It is relatively easy to limit the swing of ECL outputs, either internally or externally, and match the EIA–644 specification. ECL inputs are differential as well and will switch with a 50 mV differential, although the specification is generally much higher. An ECL differential input pair is far better matched than CMOS devices. This translates to more consistent switching and results in lower pin–to–pin skew and lower part–to–part skew, as well. ECL has made tremendous strides in process technology. Submicron geometry predominates, with much lower voltage and internal capacitance. The f_τ available now is 10 – 20 GHz or more. In bus driver applications, ECL can be ten times faster than CMOS (GTL or LVDS).

Figure 3 illustrates a differential ECL driver with emitter follower outputs and comparator inputs. As with CMOS, processing innovations allow power requirements to drop dramatically for ECL. Unlike CMOS, the speed of the device doesn't decrease with lower voltage, as long as the device is specified to operate at that voltage. New ECL devices have 2.5 volt specifications and are faster than older higher voltage parts because of improved device geometry. Also, unlike CMOS, power requirements are fairly independent of toggle rate. Newer devices operating at even lower voltage will be available soon. This translates directly to lower power since the current is nearly independent of the operating voltage.

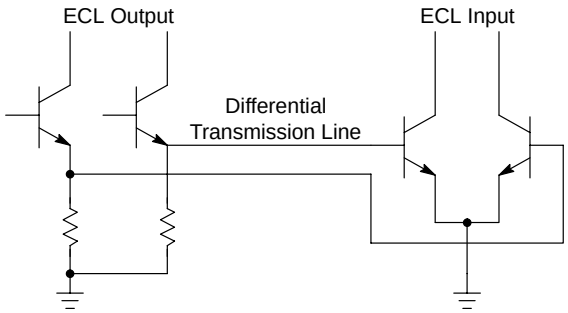

Figure 3. ECL Driver with Emitter Follower Outputs and Comparator Inputs

Comparing ECL to CMOS LVDS and Standard CMOS Devices

Table 1 shows the performance of several devices. The methodology uses a single receiver/transmitter pair. It is assumed the devices are terminated with power consumption stated per pair. All values come from original manufacturers' data sheets. The supply voltage is the value recommended by the manufacturer. It is assumed the VCX device is driving an 80 Ω resistor.

Table 1. Device Comparison

Characteristic	Units	Vendor "A"	ECLinPS Plus™	VCX
Transmitter	–	LV017A	100EP16	VCX04
Receiver	–	LV018A	100EP16	VCX04
Technology	–	CMOS/LVDS	ECL	CMOS
Standards	–	EIA–644	ECL	CMOS
Operating Voltage	–	3.3	3.3	3.3
Max Operating Frequency	MHz	300	3000	200
Max Propagation Delay*	ps	4000	280	5.6
Max Differential Skew*	ps	1100	40	N/App
Max Part to Part Skew*	ps	2000	140	4400
Power Cons at Max Frequency (typical)*	mW	133	158	100

*Per transmitter/receiver pair

Conclusion

There were no GTL line drivers available to compare, so VCX was used as the closest CMOS technology. GTL, if made into a line driver, would be expected to have power requirements somewhat greater than LVDS since the technology is similar. GTL is essentially single–ended LVDS with a fixed reference voltage. The power requirements are nearly the same for ECL and LVDS, even though ECL runs at ten times the speed.

For line driver applications, LVDS is useful below 300 MHz. Beyond 300 MHz, the designer has the choice of ECL or multiple LVDS drivers. There are some LVDS clock drivers available at the present and results are similar. Pin–to–pin skew is much worse for LVDS when compared to ECL and the power requirements are quite similar. Although attempts have been made to create a differential bus using BLVDS devices, BLVDS devices are useful to about 300 MHz. They have skew and propagation delay much higher than ECL without the noise immunity.

For backplane applications, BLVDS needs to match impedance as low as 20 Ω. This will be the subject of a forthcoming article.

It would seem that GTL is much better suited than ECL or standard CMOS to backplane requirements at less than 300 MHz, since it requires only a single line per I/O. For optimal backplane speed, ECL is still the only technology that will permit speed greater than 300 MHz reliably, and surprisingly, at power levels not very different from CMOS running at much lower speed.

References:

1. MECL System Design Handbook, William Blood, ON Semiconductor Publication HB205/D, Rev.1A, May, 1988.
2. "Fast GTL Backplane with the GTL 1655," P. Forstner and J. Huchzermeier, T. I. Application Note, 1999.

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