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AND8037/D

Stability in High Speed Linear LDO Regulators

Prepared by: Tod Schiff
ON Semiconductor

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APPLICATION NOTE

Abstract

In today's world of high speed, high power processors, there is a great demand put on the design of the power supply for these devices. There is the need for regulation down to low voltages with large currents that must have response times in the microseconds for changing loads. The lower voltage levels also demand that the "noise" on the output be extremely small. Transient response and gain peaking will determine the magnitude of these factors. Closed loop response of the regulator design thus becomes more of a critical issue.

The future shows these voltages going down, currents going up, and transient responses approaching 100 nsec, only placing more restrictions on the designer's goal of using real world devices to achieve these requirements.

The devices of the past have been compensated internally to handle a wide range of output capacitor types and remain functional (stable). The response time of these regulators has been sufficient to handle most or all of the applications they are used in. There is usually a minimum ESR for the output capacitor specified with no limitations on the maximum. If an external power device (usually a BJT or MOSFET) is to be used, no practical limitation was placed on the design parameters for this device.

LDO controllers designed for fast transient response tend to have gain–bandwidth products that are large and place more demands on the overall design on the system to yield fast, stable, low overshoot responses. The controller's output gate drive impedance, feedback input impedance, and gain–bandwidths all play a factor in determining the selection of external components to be used. The output capacitor's ESR and capacitance as well as the output power device's input capacitance and forward conductance gain will determine the regulators response when working in conjunction with the controller's parameters.

By analyzing the overall response of the feedback loop, there are some basic guidelines that will make the overall response of the regulator less sensitive to the parasitics of the devices being used. There are also certain things one needs to look out for in the selection of components to give the best overall response.

Mathematical modeling, circuit simulation, and breadboard testing all work together to give a clear insight to this design approach. Although not perfect, the basic design guidelines will show the parameters of most interest in the selection of all devices used for the best response to meet a given set of power supply requirements.

1. Introduction

Figure 1 shows the basic components that make up a linear low–dropout (LDO) regulator. There is an error amp that measures the difference between a reference voltage supply and a feedback voltage from the output of the regulator. This error signal is amplified and then used to control the input of an output driver.

The feedback divider is used to attenuate the amount of the output voltage that is fed back to the error amplifier's input, thus allowing the output voltage to be set greater than the reference voltage.

The driver's output acts as a current source and is used for producing the output voltage of the regulator by passing this current through the output impedance. The output impedance is primarily made up of a load resistance in parallel with an output capacitor.

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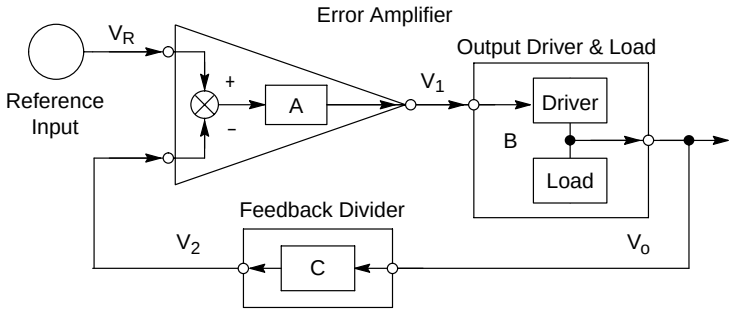
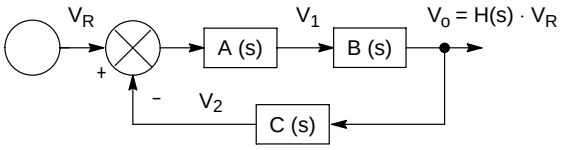


Figure 1. Basic LDO Regulator Block Diagram

The error amplifier, output driver/load, and feedback divider each has its own transfer function (A, B, and C). The stability and response of the regulator will depend on all of these.

2. LDO Closed Loop Function

The overall closed loop response of an LDO regulator determines how stable and how fast its response will be. A simplified closed loop block diagram for an LDO is shown in Figure 2. The closed loop response function for the system is also shown in terms of each of the block's transfer functions.



$$H(s) = \frac{V_O}{V_R} = \frac{1}{C(s)} \times \frac{1}{1 + \frac{1}{\{A(s) \cdot B(s) \cdot C(s)\}}} = A_V \times \frac{N(s)}{D(s)}$$

$$A_V = \frac{1}{C(s)} = 1 + \frac{R1}{R2} \text{ (DC)}$$

$$\text{or } = 1 \text{ (AC)}$$

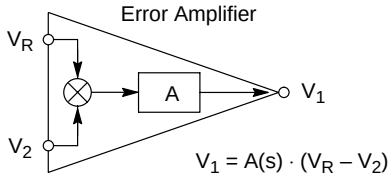
Figure 2. LDO Closed Loop Block Diagram

Here is shown the general form of the overall closed loop transfer function H(s) for the LDO regulator. Section 4 deals with the design of the feedback divider such that we obtain the desired function C(s) as shown here.

3. Error Amplifier

The error amplifier usually has a very large open loop gain at dc and then starts to roll off after a set frequency. The gain at dc is greater than 60 dB to keep the error in the output voltage of the regulator less than 0.1%. There is a dominant low frequency roll off point (pole) for controlling and limiting the gain at higher frequencies. The error amp also has a secondary high frequency pole that usually stems from the design of the part.

Figure 3 shows a basic error amplifier and its transfer function. Over the frequency range of interest for stability and transient analysis, the transfer function for the error amplifier A(s) can be approximated as shown.



$$A(s) = \frac{A_0}{\left(\frac{s}{\omega_0} + 1\right) \cdot \left(\frac{s}{\omega_1} + 1\right)} \approx \frac{\omega_a}{s} \cdot \frac{1}{\left(\frac{s}{\omega_1} + 1\right)}$$

A_0 – error amp open loop gain
ω_0 – dominant error amp pole
ω_1 – secondary error amp pole (set $\omega_1 = \omega_a$ if not specified)
ω_a – error amp gain bandwidth
$A_0 \cdot f_0$ – gain bandwidth

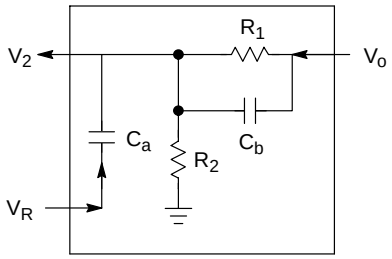
Figure 3. Feedback Divider and Transfer Function

Notice we introduce here a term commonly known as the "gain–bandwidth" of the amplifier. The device manufacturer usually specifies the gain bandwidth directly or graphically. Unfortunately, the second pole is generally not specified. It is conservative (for the purpose of analysis) to set this pole equal to the gain–bandwidth of the error amp.

4. The Feedback Divider

The feedback divider is used for setting the output voltage of the LDO regulator when the output is required to be larger than the reference input voltage. At high frequencies though, it would be preferred not to attenuate the output signal that is delivered to the error amp input.

Figure 4 shows the components that make up the divider as well as its transfer function.



$$V_2 = \frac{1}{A_V} \cdot \frac{(1 + sC_bR_1) \cdot V_o + (sC_aR_T) \cdot V_R \cdot A_V}{[1 + s(C_a + C_b)R_T]}$$

$$A_V = 1 + \frac{R_1}{R_2} \qquad R_T = R_a \parallel R_b$$

Figure 4. Feedback Divider and Transfer Function

By looking at the expression for V_2 one can see it depends on both the output voltage V_O and reference input V_R. By setting the components in the divider properly, one can achieve the desired result for C(s). The following design guidelines yield the proper results:

$$A_V = \frac{V_o}{V_R}(DC) \qquad R_1 \le \frac{A_V}{10\omega_a C_a}$$

$$R_2 = \frac{R_1}{(A_V - 1)} \qquad C_b \ge \frac{100}{\omega_a R_2}$$

V_o − output voltage (known)
V_R − reference voltage (known)
A_V − DC gain (solve for)
ω_a − gain bandwidth (from error amp analysis)
C_a − error amp input capacitance (use 10 pf if not specified)
R_1 − first divider resistor (solve for)
R_2 − second divider resistor (solve for)
C_b − divider compensation capacitor (solve for)

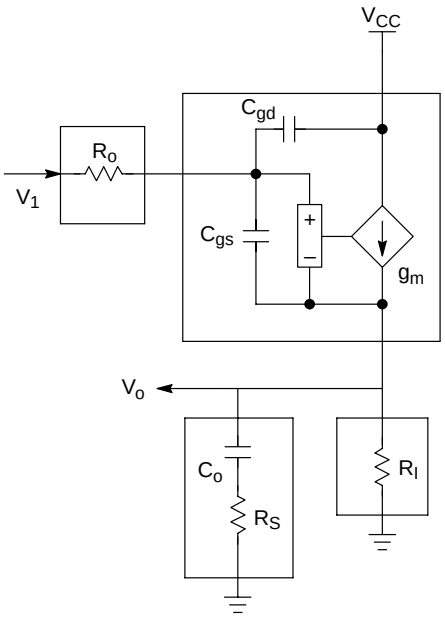
$$V_2 = C(s) \cdot V_o \qquad C(s) = \frac{1}{A_V}\,(DC) = 1\,(AC)$$

If the feedback divider is built into the device (i.e. a fixed output voltage version), then the divider is typically already optimized for these design guidelines.

5. Output Driver and Load

The final component block of the LDO regulator is the output driver and load combination. Together they form the final transfer function block in the system. This section of the LDO regulator is the most complex section dealt with so far. It also happens to be the one that has the most influence on the overall system behavior. It is the one the designer has the most control over, which can be both good and bad. It is good from the standpoint that the designer has the flexibility to make the system perform optimally with the proper selection of components. But it can be bad for the same reason if the approach to selecting these components is not well understood.

The components that make up this section of the circuit and its associated transfer function are shown in Figure 5.



$$B(s) = \frac{\left(\frac{s}{\omega_c} + 1\right)}{\left\{s^2 \frac{1}{\omega_c \cdot \omega_F} \cdot \left(\beta + \frac{1}{g_m \cdot R_s}\right) + s\left[\frac{1}{\omega_c} \cdot \left(1 + \frac{1}{g_m \cdot R_s}\right) + \frac{\beta}{\omega_F}\right] + 1\right\}}$$

$$\omega_c = \frac{1}{R_s \cdot C_o} \qquad \omega_F = \frac{1}{C_i \cdot R_o}$$

$$C_i = C_{gs} + C_{gd} \qquad \beta = \frac{C_{gd}}{(C_{gs} + C_{gd})}$$

$$V_o = B(s) \cdot V_1$$

Figure 5. Output Driver/Load and Transfer Function

Here it can be seen that the transfer function B(s) contains two poles and one zero. There are also two frequency components. One is made up from the error amplifier's output impedance interacting with the driver's input capacitance. The other is the component associated

with the output capacitor's equivalent series resistance (ESR) and capacitance.

To best determine the impact of these components on the overall response of the system, we next need to determine the overall closed loop transfer function and look at it in detail.

6. Closed Loop Response Analysis

In section 2 we determined an expression for the overall closed loop transfer function H(s). We now need to combine the results for A(s), B(s), and C(s) into this formula to produce the following for H(s):

$$H(s) = A_V \cdot \frac{N(s)}{D(s)} = \frac{N(s)}{D(s)} \ (A_V = 1, \ AC)$$

$$N(s) = \left(\frac{s}{\omega_c} + 1\right)$$

$$D(s) = \left\{ \begin{array}{l} \frac{s^4}{\omega_1 \cdot \omega_a \cdot \omega_c \cdot \omega_f} \cdot \left(\beta + \frac{1}{g_m \cdot R_S}\right) + \frac{s^3}{\omega_1 \cdot \omega_a} \cdot \left[\frac{1}{\omega_c}\left(1 + \frac{1}{g_m \cdot R_S}\right) + \frac{\beta}{\omega_f}\right] + \frac{s^3}{\omega_a \cdot \omega_c \cdot \omega_f} \cdot \left(\beta + \frac{1}{g_m \cdot R_S}\right) \\ + \frac{s^2}{\omega_1 \cdot \omega_a} + \frac{s^2}{\omega_a} \cdot \left[\frac{1}{\omega_c} \cdot \left(1 + \frac{1}{g_m \cdot R_S}\right) + \frac{\beta}{\omega_f}\right] + s \cdot \left(\frac{1}{\omega_a} + \frac{1}{\omega_c}\right) + 1 \end{array} \right\}$$

It can be seen that the system contains one zero and four poles overall. It is also obvious that this expression is far to complex to work from directly and some limitations need to be placed on the factors involved to yield the type of response desired.

A closer analysis of the pole locations places them generally as two real (one high frequency and one low) and the other two being complex or real (depending on the design). By determining the conditions for having the poles remaining in the left–hand plane (required for stability) and being critically damped or more (required for optimum response), the following set of design guidelines are obtained.

$$\omega_p = \left(\frac{1}{\omega_1} + \frac{1}{\omega_f}\right)^{-1}$$

$$\frac{1}{20 \cdot \left(1 + \frac{\omega_a}{(3 \cdot \omega_p)}\right)} \cdot \frac{1}{g_m} \le R_S \le \frac{(3 \cdot \omega_p)}{\omega_a} \cdot \frac{1}{g_m}$$

$$C_o \cdot R_S = \frac{1}{\omega_c} \ge 5 \cdot \left(\frac{1}{\omega_a} + \frac{1}{\omega_p}\right)$$

$$T = \frac{1}{\omega_p} + \frac{1}{g_m \cdot R_S \cdot \omega_a}$$

ω_p − secondary pole for open loop (solve for)
ω_1 − error amp second pole (known or assumed)
ω_f − driver pole frequency
(if driver built in, let $\omega_p = \omega_1$)
ω_a − gain bandwidth (from error amp analysis)
g_m − maximum driver transconductance gain
(if driver built in, then $1/g_m$ is the output impedance of the regulator)
R_S − ESR resistance of output capacitor (solve for)
C_o − output capacitor (solve for)
T − overall loop response time (solve for)

These guidelines give the designer a straightforward method of solving for the output driver and output capacitor in terms of the controller being used. It also allows one to determine what controller may be needed if a given time response is required for the network. In general, it ties together all of the parameters involved in the design.

If a regulator is being used where the output driver device is built in, then one needs to follow the described procedure given above in the selection of the parameters.

These guidelines have been used to design LDO regulators that have been simulated and prototyped. A design example and closed loop response has been done where the various components have been changed to show the validity of these design guidelines (refer to section 8 and [1]).

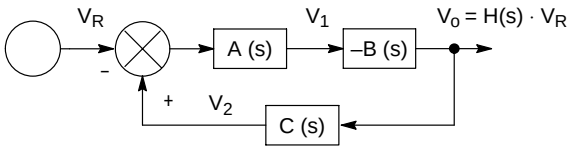
7. Alternate LDO Topologies

Up to now, the closed loop response design has been geared for an N–channel MOSFET output driver topology. If the output driver were an NPN transistor, the only change would be to make the following substitutions.

$$C_{gs} = C_{be} \qquad C_{gd} = C_{bc}$$

So instead of gate–to–source and gate–to–drain capacitances, we have base–to–emitter and base–to–collector (the base–to–emitter resistance can be ignored).

If the LDO regulator is designed for driving a P–channel MOSFET (or PNP transistor), the closed loop changes are only sign changes with the overall analysis remaining the same. Figure 6, on the following page, shows this style of topology and the resulting overall transfer function H(s) (which is the same as the previous).



$$H(s) = \frac{V_O}{V_R} = \frac{1}{C(s)} \times \frac{1}{1 + \frac{1}{[A(s) \cdot B(s) \cdot C(s)]}} = A_V \times \frac{N(s)}{D(s)}$$

Figure 6. Closed Loop Block Diagram and Transfer Function for Alternate Topology

The same basic design guidelines still apply for this form of LDO regulator.

8. Design Example

The following is a design example to show the response of an LDO based on changing various parameters. It is shown that the design guidelines presented yield a stable response and can also be used for optimizing the transient behavior.

The MC33567 dual LDO controller and MTD3055 N–channel MOSFET will be used for the design example.

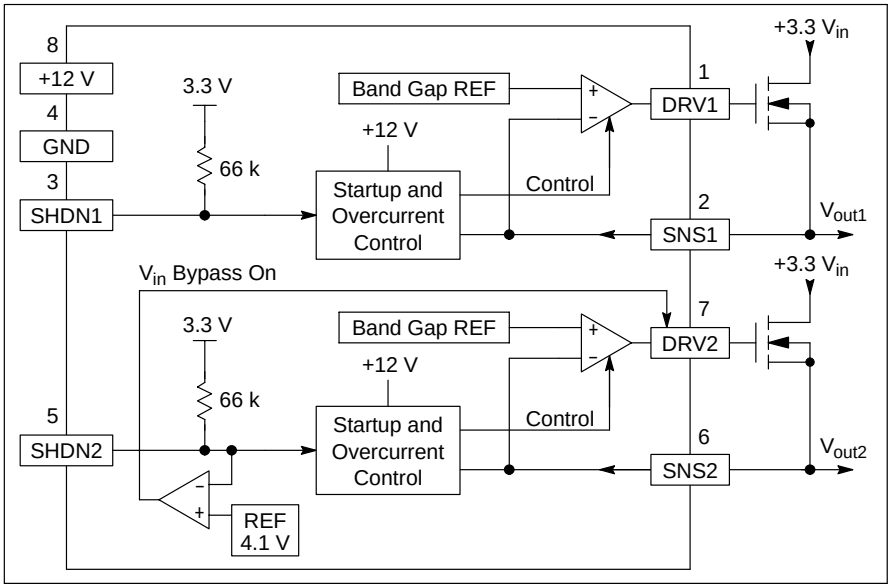
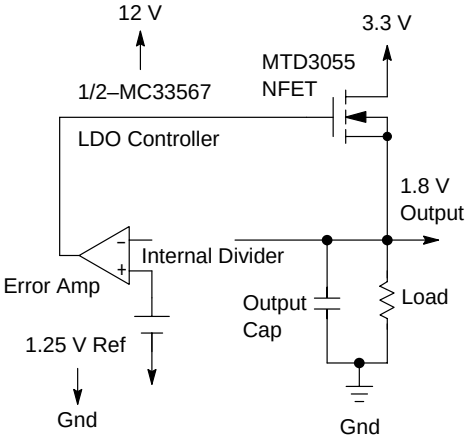


Figure 7. MC33567 Dual LDO Controller

The following figure shows the LDO regulator design and the parameters for the MC33567 controller and MTD3055 NFET.



Circuit Parameters:
MC33567 – 5 MHz Gain Bandwidth
50 Ω Output Impedance
Optimized Internal Divider
MTD3055 – 7 Ω Transconductance Gain
2200 pf Input Capacitance
Load – 0.9 A (2 Ω)

Figure 8. LDO Regulator Example Using MC33567 and MTD3055

Figure 9 shows what happens to the closed loop response when the ESR of the output capacitance is changed. The computed upper and lower limits on the ESR for this design example are also shown.

Note that making the ESR larger or smaller tends to make the response more unstable. Notice that making the ESR larger speeds up the closed loop response but will also increase the magnitude of the initial transient response due to fast changes in output current (see Figure 13).

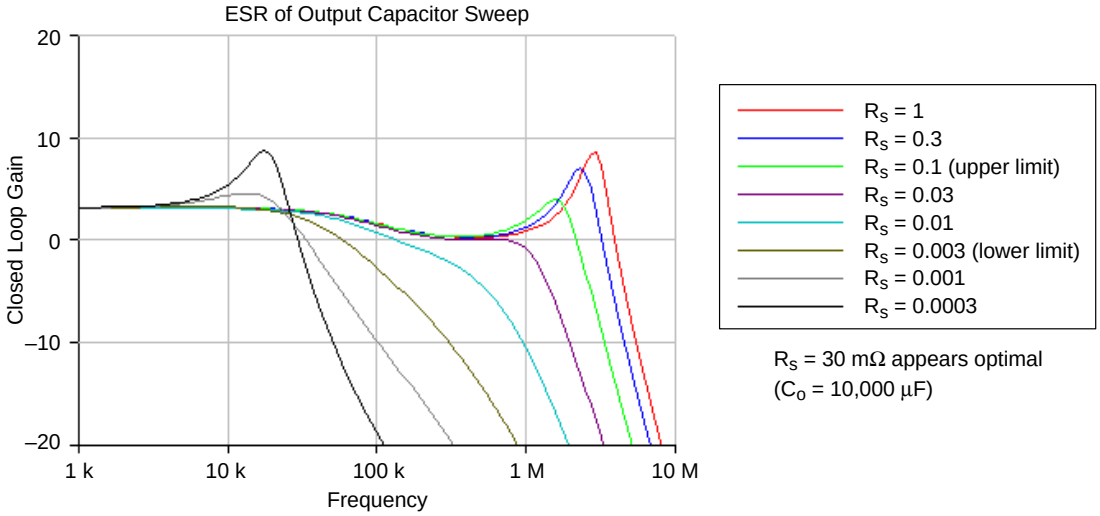


Figure 9. Closed Loop Response for Varying ESR of Output Capacitor

Figure 10 shows what happens to the closed loop response when the value of the output capacitance is changed. The limit on the value for this design example is also shown.

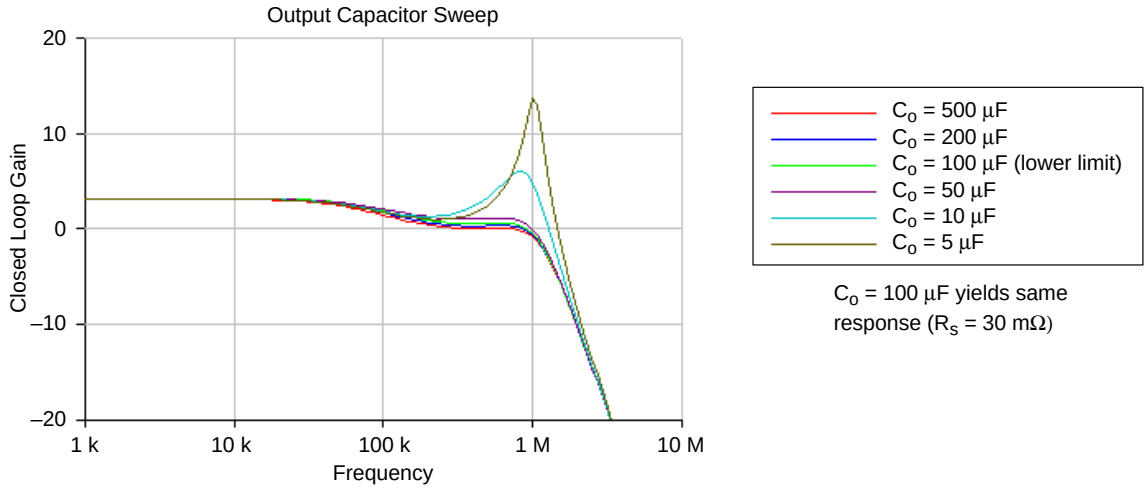


Figure 10. Closed Loop Response for Varying Value of Output Capacitor

Figure 11 shows what happens to the closed loop response when the output driver (NFET) is changed. The system is optimized for the MTD3055. By changing to a higher gain FET, we create more instability. If there needs to be interchangeability on driver devices, always design around the higher gain one so the other devices will be stable.

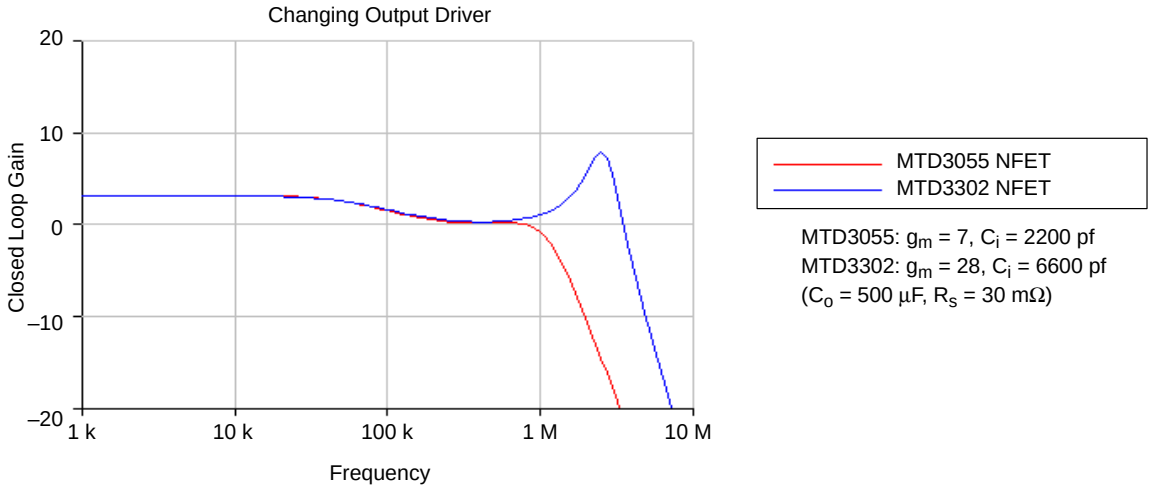


Figure 11. Closed Loop Response for Changing Output Driver

Figure 12 shows what happens to the closed loop response when the gain bandwidth of the error amp is changed. The system was optimized for the MC33567 5 MHz gain bandwidth. By changing to a higher value, we create more instability.

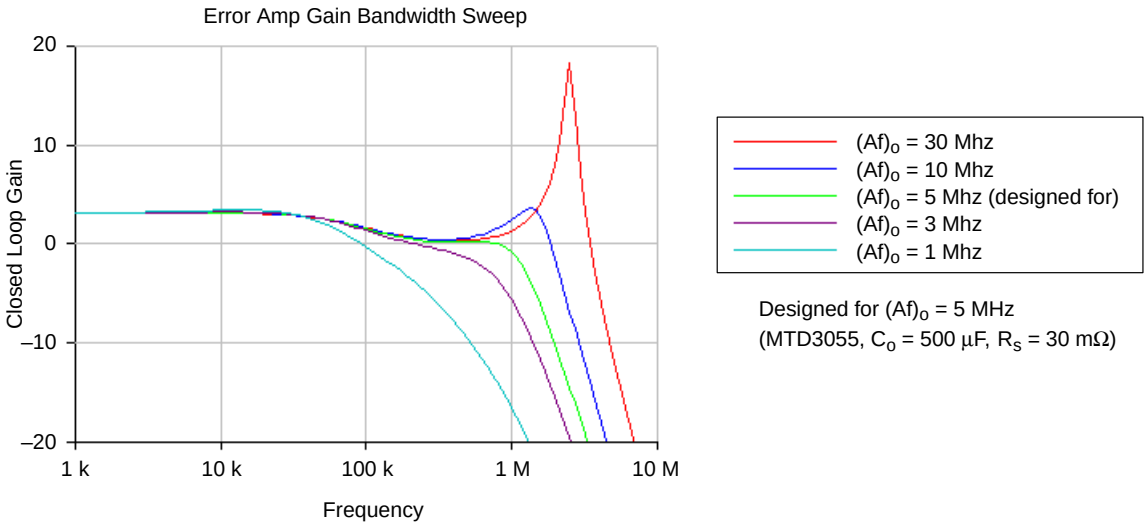


Figure 12. Closed Loop Response for Changing Error Amplifier Gain Bandwidth

Finally, we want to take a look at the transient response for the LDO regulator where the design guidelines have been used. Figure 13 is what an optimized transient response looks like in theory and Figure 14 shows various transient responses for the design example.

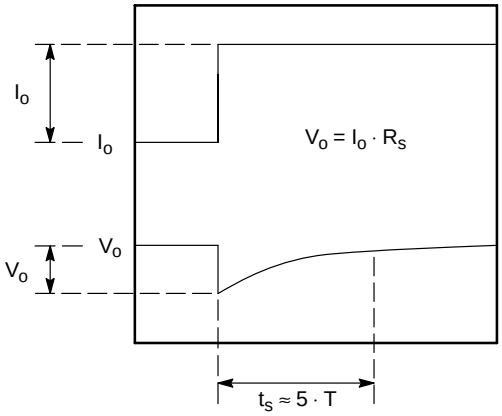


Figure 13. Typical Transient Response for Optimized System

Here, the value T is from section 6. If the transient response is a requirement, one can use the equations in Figure 13 to solve for R_S and T, then use the design guidelines in reverse to select the appropriate LDO controller/regulator design.

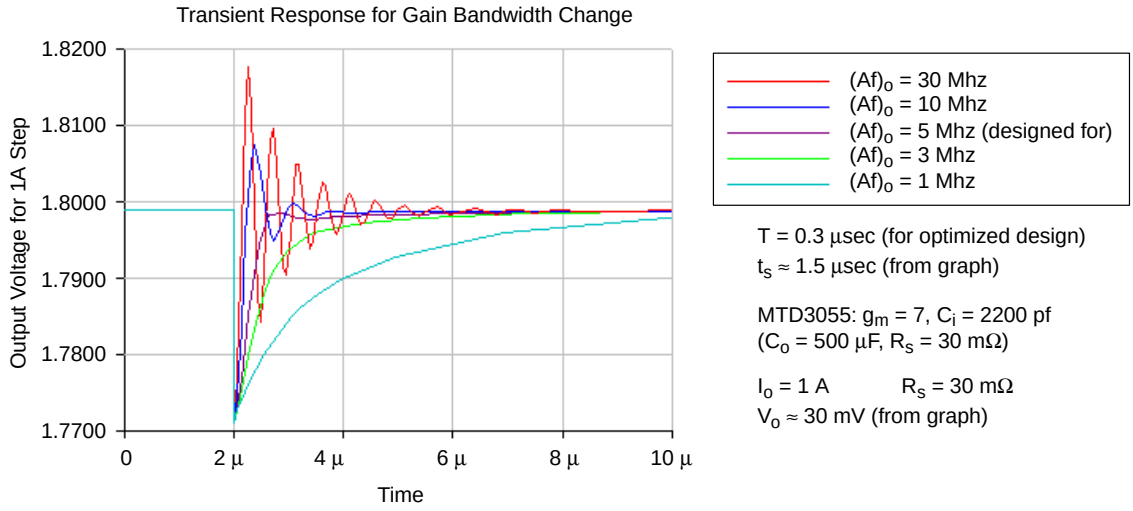


Figure 14. Transient Response for Changing Error Amplifier Gain Bandwidth

It can be seen that the transient response for the optimized design responds the fastest with little or no overshoot after the initial step. If the initial step is too large, a smaller ESR is needed for the output capacitor. But one needs to go through the design guidelines with this new value to make sure stability is preserved.

9. Conclusions

The basics involved for designing a linear LDO regulator based on stability and response has been presented to the designer in a form that allows the selection of components for the design. These guidelines are straightforward and do not require an analysis of the open loop response, phase margin, or pole/zero location.

Once a design has been produced using these guidelines, one should run the circuit through a simulation and then prototype it. There are other factors involved, such as second order parasitics and circuit board layout interference that can cause the network to behave differently than expected. The guidelines given are generally conservative enough to make the overall design least susceptible to these issues.

Also, since the guidelines given are very conservative, one may obtain a satisfactory result with component values that lie just outside of the guidelines (although deviating far from them will generally cause instability).

References

1. Schiff, Tod (2000), “Stability in High Speed Linear LDO Regulators’’, Tech Online Symposium for Electronics Engineers.

Notes

Notes

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001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.