Design Guideline for 3-Channel Interleaved CCM PFC Using the FAN9673 5 kW CCM PFC Controller

AN4165/D

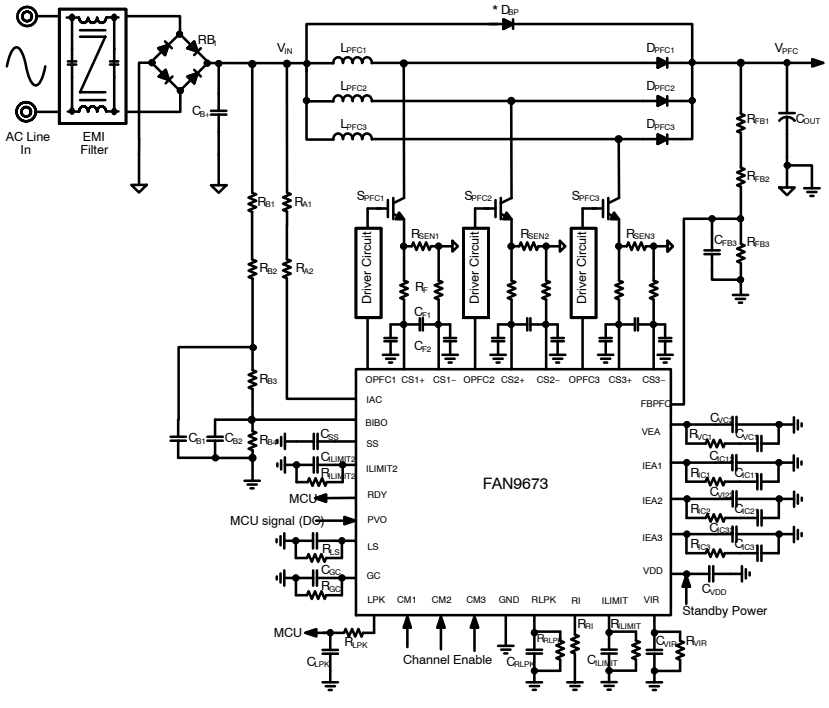
INTRODUCTION

The interleaved boost Power Factor Correction (PFC) converter has become the topology of choice for high−power applications due to the improved efficiency that can be achieved through load current sharing. By sharing the load current in more than one balanced phase, the RMS current stress, current ripple, and boost inductor size per phase can be significantly reduced. Therefore, the heavy load efficiency can be significantly improved, which allows for the selection of cost effective power MOSFET and boost diode as well as improved longevity of the power supply.

The FAN9673 advanced PFC controller is an optimal solution for implementing high−power PFC (above several kilowatts). The FAN9673 is a Continuous Conduction Mode (CCM) PFC controller for a three−channel interleaved boost−type pre−regulator.

Incorporating circuits for the implementation of leading−edge modulation, average current mode, boost−type power factor correction, the FAN9673 enables the design of a power supply that fully complies with the IEC61000−3−2 specification. The FAN9673 also features an innovative channel management function, which allows the power level of the slave channels to be loaded/unloaded smoothly according to the voltage on CM pin, thereby improving the PFC converter's load transient response.

This application note presents practical design considerations for a 3−channel interleaved CCM boost PFC employing the FAN9673. It includes the procedure for designing the boost inductor and output filter, selecting components, and implementing average current mode control. The design procedure is then verified through an experimental 5 kW prototype converter. Figure 1 shows the typical application circuit of the PFC converter.



* About D_{BP} please reference System Design Precautions

Figure 1. Typical Application Circuit of FAN9673

DESIGN PROCEDURE

In this section, a design procedure is presented using the schematic of Figure 1 as the reference. A 5 kW rated output power, three−channel CCM interleaved PFC with European input range (high−line single range) is selected as a design example. The design specifications are as follows:

Table 1. DESIGN SPECIFICATIONS

Line Voltage Range	180 ~ 264 V_{AC}
Line Frequency	50 Hz
Nominal PFC Output Voltage	V_{PFC} = 393 V
Minimum PFC Output Voltage	V_{PFC2} = 350 V
Output Power	P_O = 5 kW
Number of Channel	3
PFC Output Voltage Ripple	5%
Switching Frequency	f_{SW} = 40 kHz
PFC Efficiency	η > 0.95
Brownout Line Voltage	160 V_{AC}
Brown−in Line Voltage	170 V_{AC}
Channel Management Method	External Signal from MCU

[STEP −1] Estimate Input Rated Power and Output Current

The overall system is comprised of three parallel boost PFC stages, as shown in Figure 2, so the input power of the PFC stage is given as:

$$P_{IN} = \frac{P_{OUT-TOT}}{\eta} \quad \text{(eq. 1)}$$

where η is combined efficiency of the PFC stages.

The output current of PFC stage is given by:

$$I_{OUT-TOT} = \frac{P_{OUT-TOT}}{V_{PFC}} \quad \text{(eq. 2)}$$

The output current of each boost stage is given by:

$$I_{OUT} = \frac{P_{OUT-TOT}}{V_{PFC} \times \text{Channel Number}} \quad \text{(eq. 3)}$$

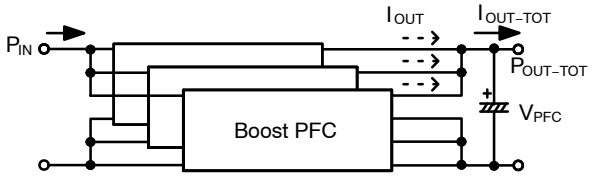


Figure 2. PFC Stage Configuration

Design Example

$$P_{IN} = \frac{P_{OUT-TOT}}{\eta} = \frac{5000}{0.95} = 5263\ \text{W} \quad \text{(eq. 4)}$$

$$P_{OUT} = \frac{P_{OUT-TOT}}{\text{Channel number}} = \frac{5000}{3} = 1667\ \text{W} \quad \text{(eq. 5)}$$

$$I_{OUT-TOT} = \frac{P_{OUT-TOT}}{V_{PFC}} = \frac{5000}{393} = 12.27\ \text{A} \quad \text{(eq. 6)}$$

$$I_{OUT} = \frac{I_{OUT-TOT}}{3} = \frac{12.72}{3} = 4.24\ \text{A} \quad \text{(eq. 7)}$$

[STEP −2] Frequency Setting

The internal oscillator frequency of the FAN9673 is determined by the external resistor RRI on the RI pin. The switching frequency is determined by the timing resistor RRI, calculated as:

$$f_{SW} \cong \frac{8 \times 10^8}{R_{RI}} \quad \text{(eq. 8)}$$

The guaranteed switching frequency ranges are 18 kHz ~40 kHz and 55 kHz ~75 kHz.

Design Example

R_{RI} of 20 kΩ is selected to obtain 40 kHz switching frequency.

$$R_{RI} = \frac{8 \times 10^8}{f_{SW}} = \frac{8 \times 10^8}{40 \times 10^3} = 20\text{k}\Omega \quad \text{(eq. 9)}$$

[STEP −3] V_{IN} Range & R_{IAC} Setting

The FAN9673 senses the peak value of line voltage using the IAC pin, as shown in Figure 3. The peak value of the line voltage is obtained by a peak detect circuit using a sample−and−hold method. Meanwhile, the instantaneous line voltage information is obtained by sensing the current that flows into the IAC pin through R_{IAC}.

R_{IAC} should be selected according to the input voltage range. For universal AC input (85 V ~ 264 V), V_{VIR} should be set < 1.5 V and R_{IAC} should chosen as 6 MΩ. If the input is high−voltage single−range AC input (180 V ~ 264 V), V_{VIR} should be set > 3.5 V (maximum is 5 V) and R_{IAC} should be chosen as 12 MΩ. V_{VIR} should be determined based on the AC input range. The setting of V_{VIR} influences gain of the gain modulator, RDY−pin hysteresis, and the brown−in/out hysteresis.

$$V_{AC} = 85\ \text{V} \sim 265\ \text{V} \Rightarrow R_{IAC} = 6\ \text{M}\Omega,\ V_{VIR} < 1.5\ \text{V}$$
$$V_{AC} = 180\ \text{V} \sim 265\ \text{V} \Rightarrow R_{IAC} = 12\ \text{M}\Omega,\ V_{VIR} > 3.5\ \text{V} \quad \text{(eq. 10)}$$

The V_{VIR} can be set according to the equation below:

$$V_{VIR} = I_{VIR} \times R_{VIR} \quad \text{(eq. 11)}$$

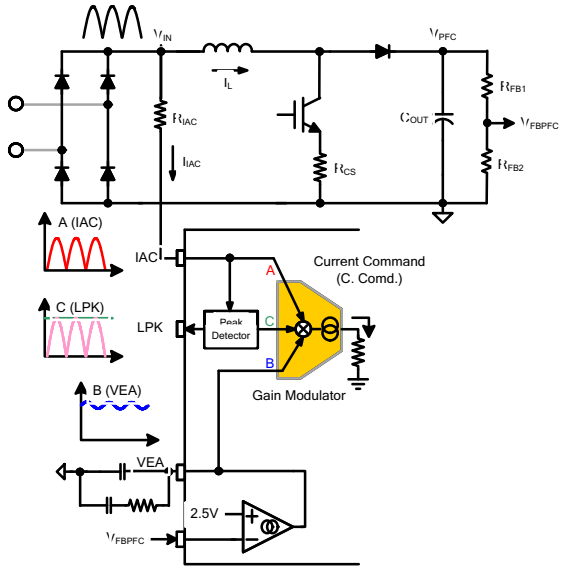


Figure 3. Line Sensing Circuits

Design Example

The PFC is designed for high−voltage single−range AC input (180 V ~ 264 V). R_{IAC} should be chosen as 12 MΩ and R_{VIR} is:

$$V_{VIR} = I_{VIR} \times R_{VIR} = 10\ \mu A \times 470\ k\Omega = 4.7\ V > 3.5\ V \quad \text{(eq. 12)}$$

470 kΩ is selected for RVIR for the AC input range of 180 V ~ 264 V.

[STEP−4] PFC Inductor Design

The duty cycle of the boost switch at the peak of line voltage is given as:

$$D_L = \frac{V_{PFC} - \sqrt{2}V_{LINE}}{V_{PFC}} \quad \text{(eq. 13)}$$

Then, the maximum current ripple of the boost inductor at the peak of minimum AC line voltage is given as:

$$\Delta I_L = \frac{\sqrt{2}V_{LINE-MIN}}{L_{PFC}} \times \frac{V_{PFC} - \sqrt{2}V_{LINE-MIN}}{V_{PFC}} \times \frac{1}{f_{SW}} \quad \text{(eq. 14)}$$

The average of boost inductor current over one switching cycle at the peak of the line voltage for minimum AC input is given by:

$$I_{L-AVG} = \frac{\sqrt{2}P_{OUT}}{V_{LINE-MIN} \times \eta} \quad \text{(eq. 15)}$$

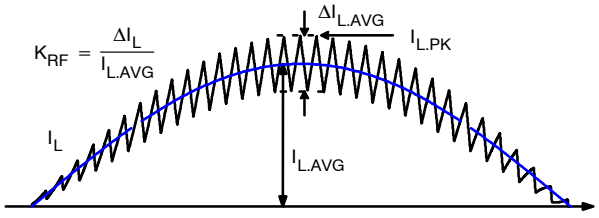


Figure 4. Inductor Current

For a given current ripple factor ($K_{RF}=DI_L/I_{LAVG}$), the boost inductor value can be obtained as:

$$L_{PFC} = \frac{\sqrt{2}V_{LINE-MIN}}{K_{RF} \times I_{L-AVG}} \times \frac{V_{PFC} - \sqrt{2}V_{LINE-MIN}}{V_{PFC}} \times \frac{1}{f_{SW}} \quad \text{(eq. 16)}$$

The maximum current of boost inductor is:

$$I_{L-PK} = I_{L-AVG} \times \left(1 + \frac{K_{RF}}{2}\right) = \frac{\sqrt{2}P_{OUT}}{V_{LINE-MIN} \times \eta} \times \left(1 + \frac{K_{RF}}{2}\right) \quad \text{(eq. 17)}$$

Design Example

The average of the boost inductor current over one switching cycle at the peak of the minimum AC line (assume it's brownout of PFC) is obtained as:

$$I_{L-AVG} = \frac{\sqrt{2} \times P_{OUT}}{V_{LINE-MIN} \times \eta} = \frac{\sqrt{2} \times 1667}{160 \times 0.95} = 15.5\ A \quad \text{(eq. 18)}$$

The boost inductor is obtained as:

$$L_{PFC} = \frac{\sqrt{2}V_{LINE-MIN}}{K_{RF} \times I_{L-AVG}} \times \frac{V_{PFC} - \sqrt{2}V_{LINE-MIN}}{V_{PFC}} \times \frac{1}{f_{SW}}$$

$$= \frac{\sqrt{2} \times 160}{1.55 \times 15.5} \times \frac{393 - \sqrt{2} \times 160}{393} \times \frac{1}{40 \times 10^3} = 100\ \mu H \quad \text{(eq. 19)}$$

The maximum current of the boost inductor is given as:

$$I_{L-PK} = \frac{\sqrt{2}P_{OUT}}{V_{LINE-MIN} \times \eta} \times \left(1 + \frac{K_{RF}}{2}\right)$$

$$= \frac{\sqrt{2} \times 1667}{160 \times 0.95} \times \left(1 + \frac{1.55}{2}\right) = 27.51\ A \quad \text{(eq. 20)}$$

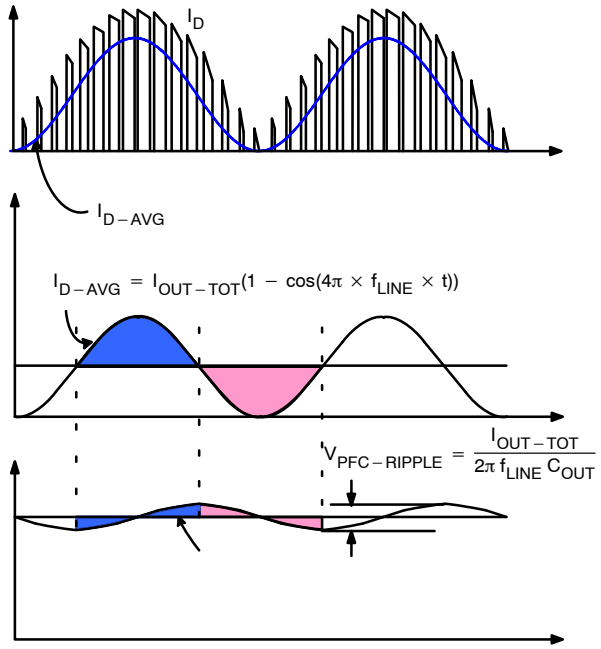


Figure 5. PFC Output Voltage Ripple

The output voltage ripple should be considered when selecting the PFC output capacitor. Figure 5 shows the line frequency ripple on the output voltage. With a given specification of output ripple, the value for the output capacitor can be obtained from:

$$C_{OUT} > \frac{I_{OUT-TOT}}{2\pi f_{LINE} V_{PFC-RIPPLE}} \quad \text{(eq. 21)}$$

where $I_{OUT-TOT}$ is nominal output current of the boost PFC stage and $V_{PFC-RIPPLE}$ is the peak−to−peak output voltage ripple.

The hold−up time should also be considered when determining the output capacitor value:

$$C_{OUT} > \frac{2 \times P_{OUT-TOT} \times t_{HOLD}}{V_{PFC}^2 - V_{PFC-MIN}^2} \quad \text{(eq. 22)}$$

where $P_{OUT-TOT}$ is nominal output power of boost PFC stage; t_{HOLD} is the required holdup time, and $V_{PFC-MIN}$ is the allowable minimum PFC output voltage during the hold−up time.

Design Example

With peak−to−peak voltage ripple specification of 5% of V_{PFC}, the capacitor should be:

$$C_{OUT} > \frac{I_{OUT-TOT}}{2\pi f_{LINE} V_{PFC-RIPPLE}}$$

$$= \frac{12.72}{2\pi \times 50 \times (393 \times 5\%)} = 2060\ \mu F \quad \text{(eq. 23)}$$

Assuming the minimum allowable output voltage during one cycle (15 ms) drop−out is 300 V, the capacitor value should be:

$$C_{OUT} > \frac{2 \times P_{OUT-TOT} \times t_{HOLD}}{V_{PFC}^2 - V_{PFC-MIN}^2}$$

$$= \frac{2 \times 5000 \times 15 \times 10^{-3}}{393^2 - 300^2} = 2327\ \mu F \quad \text{(eq. 24)}$$

In this case, three parallel connected capacitors of 680 mF are selected for the PFC output capacitor. In this design example, the target application for the three−channel PFC is a home appliance power supply, so there is no hold−up time requirement.

[STEP−6] Output Sensing & PVO Setting

To improve system efficiency, the FAN9673 incorporates the programmable PFC output voltage function (PVO). As shown in Figure 6, when the PFC output voltage is much higher than the peak voltage of the AC input, the user can send a DC signal from the MCU to the PVO pin to decrease the PFC output voltage.

It is recommended that the PFC output voltage is set at least 25 V higher than the peak voltage of AC input. Moreover, it is necessary to consider other factors closely related to the PFC output voltage regulation, such as hold−up time, PF, and THD standard of input current.

The relationship between V_{PVO} and the feedback voltage target for regulating the PFC output voltage is:

$$V_{FBPFC} = V_{REF} - \frac{V_{PVO}}{4} \quad \text{(eq. 25)}$$

Once the desired PFC output voltage, V_{PFC2}, for low AC input is determined; the required DC voltage level V_{PVO} is given by:

$$V_{PVO} = 4 \times (V_{REF} - V_{PFC2}(\frac{R_{FB3}}{R_{FB1} + R_{FB2} + R_{FB3}})) \quad \text{(eq. 26)}$$

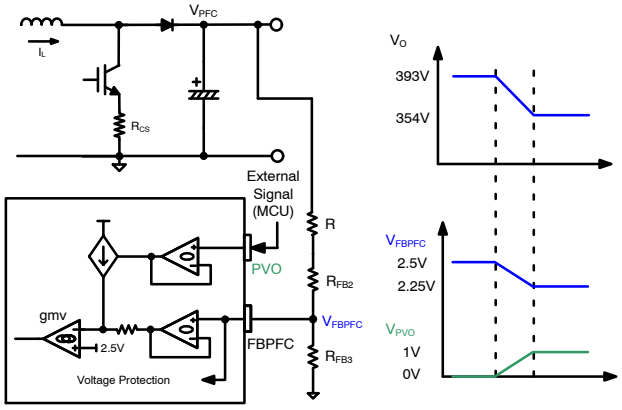


Figure 6. Two−Level PFC Output Block

Design Example

Set the PFC output level at 393 V, R_{FB3} = 23.7 kΩ:

$$R_{FB1} + R_{FB2} = \frac{R_{FB3}(V_{PFC} - V_{REF})}{V_{REF}}$$

$$= \frac{23.7 \times 10^3 (393 - 2.5)}{2.5} = 3.7\ M\Omega \quad \text{(eq. 27)}$$

Set V_{PFC2} = 350 V for low input AC 200 V, the required V_{PVO} is:

$$V_{PVO} = 4 \times (V_{REF} - V_{PFC2}(\frac{R_{FB3}}{R_{FB1} + R_{FB2} + R_{FB3}}))$$

$$= 4 \times (2.5 - 350(\frac{23.7 \times 10^3}{3.7 \times 10^6 + 23.7 \times 10^3})) = 1.09\ V \quad \text{(eq. 28)}$$

The PVO function is used to change the output voltage of PFC, V_{PFC}, which should be kept at least 25 V higher than V_{IN}.

[STEP−7] Current−Sensing & Current−Limit

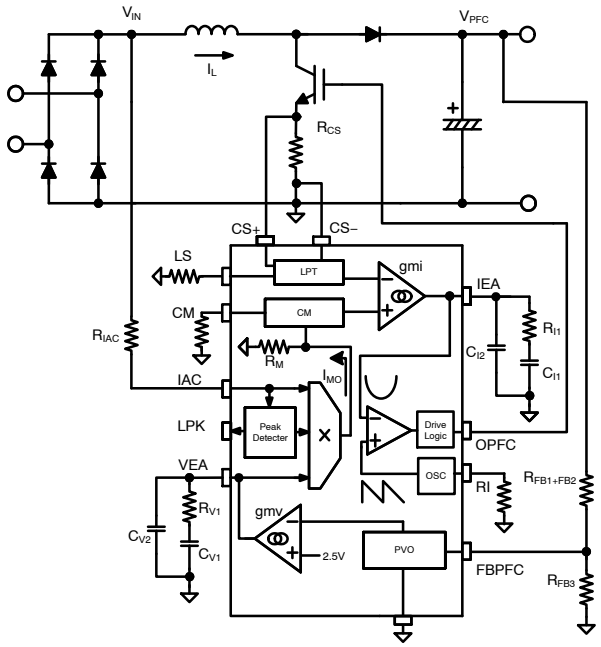


Figure 7. PFC Control Circuits

Figure 7 shows the PFC control circuits. The first step in control−circuit design is to select the current−sensing resistor of the PFC converter, considering the control window of voltage loop. Since line feed−forward is used in FAN9673, input−voltage term in control signal is eliminated and the output power is proportional to the output of voltage−control error amplifier, V_{VEA}, as:

$$P_{OUT}(V_{VEA}) = P_{OUT-MAX} \times \frac{V_{VEA} - 0.6}{V_{VEA-SAT} - 0.6} \quad \text{(eq. 29)}$$

The $P_{OUT-MAX}$ term should be calculated from maximum current command generated by the gain modulator at $V_{VEA-SAT}$. It is simplified as below:

$$P_{OUT-MAX} = \frac{V_{LINE-MIN}^{2} \times G_{MAX} \times R_M}{R_{IAC} \times R_{CS}} \quad \text{(eq. 30)}$$

The R_M is the output resistor of for multiplier to transfer the current command to a voltage type signal. G_{MAX}, which is 2, is derived from coefficients of the internal control loop and pre−assumed V_{VEA} level around 4~5V at the $P_{OUT-MAX}$ condition.

Design Example

Setting the maximum power limit of each PFC stage as 2.167 kW (130% of full load per channel), the current sensing resistor is obtained from:

$$R_{CS} = \frac{V_{LINE-MIN}^{2} \times G_{MAX} \times R_M}{R_{IAC} \times P_{OUT-MAX}}$$

$$= \frac{160^2 \times 2 \times 7.5 \times 10^3}{12 \times 10^6 \times 1.3 \times 1667} = 0.0147\ \Omega \quad \text{(eq. 31)}$$

A 15 mΩ resistor is selected.

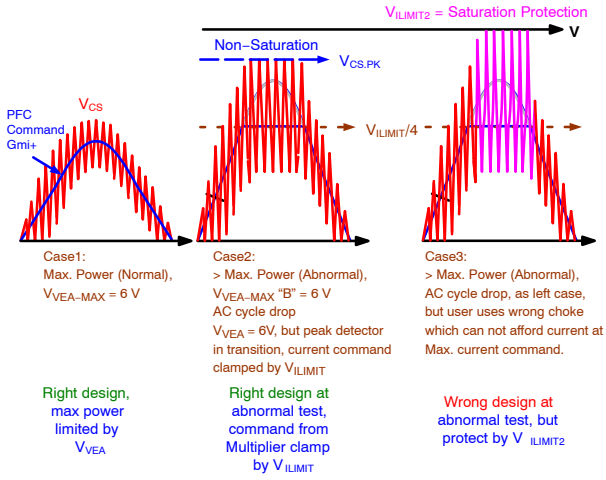


Figure 8. I_{LIMIT} and I_{LIMIT2} Function

The FAN9673 has three factors of current limit to protect from output over−current and inductor saturation: V_{EA}, V_{ILIMIT}, and $V_{ILIMIT2}$. V_{EA} controls average delivered power. V_{ILIMIT} clamps maximum current command generated by the gain modulator. $V_{ILIMIT2}$ set pulse−by−pulse current limit. We had dealt with V_{EA} with designing R_{CS}. ILIMIT and ILIMIT2 pins sourcing mirrored current from RI pin. The user can program the current limit thresholds $V_{ILIMIT1}$ and $V_{ILIMIT2}$ by connecting resistors, R_{LIMIT} and $R_{ILIMIT2}$ on those two pins.

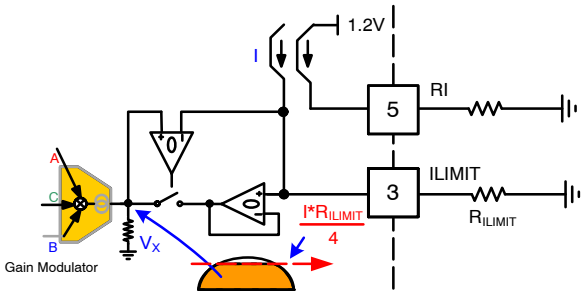


Figure 9. Internal Block of I_{LIMIT}

Generally, V_{ILIMIT} should be triggered before $V_{ILIMIT2}$ during increasing of output power, because I_{LIMIT2} is used to prevent saturation of the inductor from damaging switches.

It is typical to set the maximum power limit of the PFC stage to around 120% ~ 150% of full load, such that the V_{VEA} is around 4 ~ 4.5 V.

Resistor R_{ILIMIT} can be calculated from:

$$\frac{I_{ILIMIT} \times R_{ILIMIT}}{4} = 1.8 \times \sqrt{2} \times \frac{P_{IN}}{3 \times V_{LINE-MIN}} \times R_{CS} \quad \text{(eq. 32)}$$

where "3" is channel number of FAN9673, and 1.8 is a chosen clamping ratio.

Regarding the choice for I_{LIMIT2} level, the user can use 150% of maximum power as the setting. It's used to protect the switching devices. User can also use the maximum current rating of the semiconductor device with 10% to 20% de−rating as the limit level. I_{LIMIT2} setting is obtained as:

$$I_{ILIMIT} \times R_{ILIMIT} = 150\% \times V_{CS-PK} \quad \text{(eq. 33)}$$

Design Example

$$V_{CS-PK} = R_{CS} \times I_{L-PK} = 0.015 \times 27.51 = 0.413\ V \quad \text{(eq. 34)}$$

f_{SW} = 40 kHz is selected. Mirrored $I_{ILIMIT2}$ and I_{ILIMIT} are:

$$I_{ILIMIT} = \frac{1.2 \times 1.0208}{R_{RI}} = \frac{1.225}{20 \times 10^3} = 6.13 \times 10^{-5}\ A \quad \text{(eq. 35)}$$

$$I_{ILIMIT2} = \frac{1.2 \times 1.03125}{R_{RI}} = \frac{1.2375}{20 \times 10^3} = 6.19 \times 10^{-5}\ A \quad \text{(eq. 36)}$$

$$R_{ILIMIT2} = \frac{150\% \times V_{CS-PK}}{I_{ILIMIT2}} = \frac{1.5 \times 0.413}{6.19 \times 10^{-5}} = 10\ k\Omega \quad \text{(eq. 37)}$$

A 10 kΩ resistor is selected for setting $V_{ILIMIT2}$.

The setting of V_{ILIMIT} is obtained as:

$$R_{ILIMIT} = \frac{1.8 \times (P_{IN}/3) \times \sqrt{2} \times R_{CS}}{V_{LINE-MIN}} \times \frac{4}{I_{ILIMIT}}$$

$$= \frac{1.8 \times 1754 \times \sqrt{2} \times 0.015}{160} \times \frac{4}{6.13 \times 10^{-5}} = 27.3\ k\Omega \quad \text{(eq. 38)}$$

A 30 kΩ resistor is selected for R_{ILIMIT}.

[STEP−8] LS & GC Design

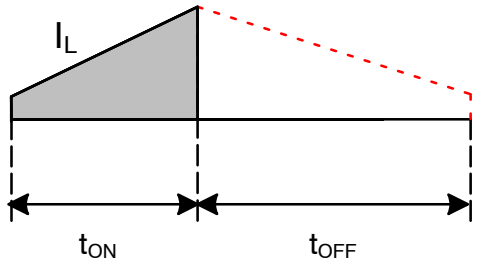


Figure 10. LPT Function for Inductor Current at t_{OFF}

The Linear Predict (LPT) function, shown in Figure 10, is used to anticipate the behavior of inductor current in the switch turn−off region. The Gain Change (GC) pin and LS pin are used to adjust the parameters of LPT function. LS sets emulated inductance value, and GC aligns sensed input and output voltages, from IAC and FBPFC pins. The LS resistance can be determined by following equation. Note the R_{LS} value need to be within 12 ~ 87 kΩ.

$$R_{LS} = \frac{L_{PFC}}{1.5 \times 10^{-9} \times R_{CS} \times \frac{(R_{FB1}+R_{FB2}+R_{FB3})}{R_{FB3}}} \quad \text{(eq. 39)}$$

Gain change is to use to adjust the output of the gain modulation. The resistor value is given by:

$$R_{GC} = \frac{6 \times 10^6}{\left(\frac{R_{FB1}+R_{FB2}+R_{FB3}}{R_{FB3}}\right)} \quad \text{(eq. 40)}$$

Design Example

Inductance of 100 μH is selected. R_{LS} and R_{GC} are obtained as:

$$R_{LS} = \frac{100 \times 10^{-6}}{1.5 \times 10^{-9} \times 0.015 \times \left(\frac{3.7 \times 10^6 + 23.7 \times 10^3}{23.7 \times 10^3}\right)} = 23.8\ k\Omega \quad \text{(eq. 41)}$$

$$R_{GC} = \frac{6 \times 10^6}{\left(\frac{3.7 \times 10^6 + 23.7 \times 10^3}{23.7 \times 10^3}\right)} = 38.19\ k\Omega \quad \text{(eq. 42)}$$

R_{LS} and R_{GC} are 28.4 kΩ and 38.2 kΩ used.

[STEP−9] PFC Current Loop Design

The transfer function that relates the duty cycle to the inductor current of boost power stage is given as:

$$\frac{\hat{i}_L}{\hat{d}} = \frac{V_{PFC}}{s \times L_{PFC}} \quad \text{(eq. 43)}$$

The transfer function relating the output of the current control error amplifier to the inductor current−sensing voltage is obtained by:

$$\frac{\hat{v}_{CSn}}{\hat{v}_{IEA}} = \frac{R_{CSn} \times V_{PFC}}{V_{RAMP} \times s \times L_{PFC}} \quad \text{(eq. 44)}$$

where V_{RAMP} is the peak−to−peak voltage of the ramp signal for the current−control PWM comparator, which is 5 V. R_{CSn} is current−sensing resistor of each channel.

The transfer function of the compensation circuit is given as:

$$\frac{\hat{v}_{IEA}}{\hat{v}_{CSn}} = \frac{2\pi f_{II}}{s} \times \frac{1 + \frac{s}{2\pi f_{IZ}}}{1 + \frac{s}{2\pi f_{IP}}} \quad \text{(eq. 45)}$$

where:

$$f_{II} = \frac{G_{MI}}{2\pi C_{IC1}}, f_{IZ} = \frac{1}{2\pi \times R_{IC} \times C_{IC1}} \text{ and } f_{IP} = \frac{1}{2\pi \times R_{IC} \times C_{IC2}} \quad \text{(eq. 46)}$$

G_{MI} is transconductance of current−loop error amplifiers in FAN9673. The procedure to design the feedback loop is as follows:

1. Determine the crossover frequency (f_{IC}) around $1/10^{th}$ ~ $1/6^{th}$ of the switching frequency. Then calculate the gain of the transfer function of Equation (46) at crossover frequency as:

$$\left|\frac{\hat{v}_{CSn}}{\hat{v}_{IEA}}\right|_{@f=f_{IC}} = \frac{R_{CS} \times V_{PFC}}{V_{RAMP} \times 2\pi f_{IC} \times L_{PFC}} \quad \text{(eq. 47)}$$

2. Calculate R_{IC} such that it makes the closed loop gain unity at crossover frequency:

$$R_{IC} = \frac{1}{G_{MI} \times \left|\frac{v_{CS}}{v_{IEA}}\right|_{@f=f_{IC}}} \quad \text{(eq. 48)}$$

3. Since the control−to−output transfer function of the power stage should have −20 dB/decade slope and −90° phase at the crossover frequency of 0 dB as shown in Figure 11, it is necessary to place the zero of the compensation network (f_{IZ}) around one third (1/3) of the crossover frequency so that more than 45° phase margin is obtained. So, the capacitance C_{IC1} is determined as:

$$C_{IC1} = \frac{1}{R_{IC} \times 2\pi f_{IC}/3} \quad \text{(eq. 49)}$$

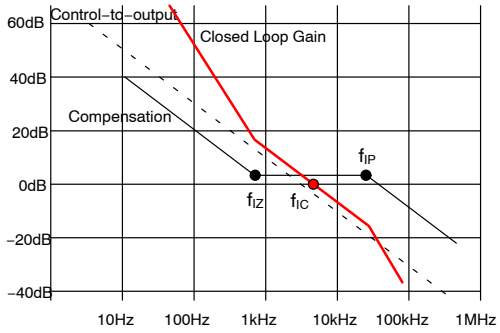


Figure 11. Current Loop Compensation

4. Place high−frequency pole (f_{IP}) at least a decade higher than f_{IC} to ensure that it does not interfere with the phase margin of the current loop at its crossover frequency.

$$C_{IC2} = \frac{1}{2\pi \times f_{IP} \times R_{IC}} \quad \text{(eq. 50)}$$

Design Example

Set crossover frequency as 4kHz:

$$\left|\frac{\hat{v}_{CSn}}{\hat{v}_{IEA}}\right|_{@f=f_{IC}} = \frac{0.015 \times 393}{5 \times 2\pi \times 4000 \times 100 \times 10^{-6}} = 0.469 \quad \text{(eq. 51)}$$

$$R_{IC} = \frac{1}{G_{MI} \times \left|\frac{v_{CS}}{v_{IEA}}\right|} = \frac{1}{88 \times 10^{-6} \times 0.469} = 24.2\ k\Omega \quad \text{(eq. 52)}$$

$$C_{IC1} = \frac{1}{R_{IC} \times 2\pi f_{IC}/3} = \frac{1}{24.2 \times 10^{3} \times 2\pi \times 4 \times 10^{3}/3} = 4.93\ nF \quad \text{(eq. 53)}$$

$$C_{IC2} = \frac{1}{2\pi \times f_{IP} \times R_{IC}} = \frac{1}{2\pi \times 4 \times 10^{4} \times 24.2 \times 10^{3}} = 0.16\ nF \quad \text{(eq. 54)}$$

Use 24.3 kΩ for R_{IC}, 4.7 nF for C_{IC1}, and 150 pF for C_{IC2}.

[STEP−10] PFC Voltage Loop Design

Since FAN9673 employs line feed−forward control, the power stage transfer function becomes independent of the line voltage. Then, the low−frequency, small−signal, control−to−output transfer function is obtained as:

$$\frac{\hat{v}_{PFC}}{\hat{v}_{VEA}} \cong \frac{I_{OUT-TOT} \times K_{MAX}}{5} \times \frac{1}{sC_{OUT}} \quad \text{(eq. 55)}$$

where $K_{MAX} = P_{OUT}{}^{MAX}/P_{OUT}$ and 5 V is window of error amplifier's linear range (5.6 V−0.6 V = 5 V)

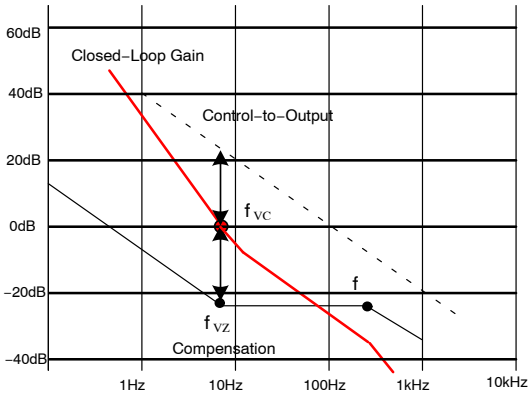


Figure 12. Voltage Loop Compensation

Proportional and integration (PI) control with high−frequency pole typically used for compensation. The compensation zero (f_{VZ}) introduces phase boost, while the high−frequency compensation pole (f_{VP}) attenuates the switching ripple, as shown in Figure 12.

The transfer function of the compensation network is obtained:

$$\frac{\hat{v}_{COMP}}{\hat{v}_{PFC}} = \frac{2\pi f_{VI}}{s} \times \frac{1 + \frac{s}{2\pi f_{VZ}}}{1 + \frac{s}{2\pi f_{VP}}} \quad \text{(eq. 56)}$$

where:

$$f_{VI} = \frac{2.5}{V_{out}} \times \frac{G_{MV}}{2\pi C_{VC1}}, f_{VZ} = \frac{1}{2\pi \times R_{VC} \times C_{VC1}}$$

$$f_{VP} = \frac{1}{2\pi \times R_{VC} \times C_{VC2}} \quad \text{(eq. 57)}$$

G_{MV} is transconductance of voltage−loop error amplifier. The procedure to design the feedback loop is as follows:

1. Determine the crossover frequency (f_{VC}) around 1/10~1/5 of the line frequency. Since the control−to−output transfer function of power stage should have −20 dB/decade slope and −90° phase at the crossover frequency, as shown in Figure 12, it is necessary to place the zero of the compensation network (f_{VZ}) around the crossover frequency so that 45° phase margin is obtained. Then, the capacitance C_{VC1} is determined as:

$$C_{VC1} = \frac{G_{MV} \times I_{OUT-TOT} \times K_{MAX}}{5 \times C_{OUT} \times (2\pi f_{VC})^2} \times \frac{2.5}{V_{PFC}} \quad \text{(eq. 58)}$$

To place the compensation zero at the crossover frequency, the compensation resistance is obtained as:

$$R_{VC} = \frac{1}{2\pi \times f_{VC} \times C_{VC1}} \quad \text{(eq. 59)}$$

2. Place compensator high−frequency pole (f_{VP}) at least a decade higher than f_{VC} to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter so noise can be effectively attenuated. Then, the capacitor C_{VC2} is determined as:

$$C_{VC2} = \frac{1}{2\pi \times f_{VP} \times R_{VC}} \quad \text{(eq. 60)}$$

Design Example

Set the crossover frequency as 20 Hz:

$$C_{VC1} = \frac{100 \times 10^{-6} \times 12.72 \times 1.3}{5 \times 2040 \times 10^{-6} (2\pi \times 20)^2} \times \frac{2.5}{393} = 65.35\ \text{nF} \quad \text{(eq. 61)}$$

$$R_{VC} = \frac{1}{2\pi \times 20 \times 65.35 \times 10^{-9}} = 121\ \text{k}\Omega \quad \text{(eq. 62)}$$

$$C_{VC2} = \frac{1}{2\pi \times f_{VC} \times R_{VC}} = \frac{1}{2\pi \times 20 \times 10 \times 121 \times 10^{3}} = 6.58\ \text{nF} \quad \text{(eq. 63)}$$

Use 118 kΩ for R_{VC}, 68 nF for C_{VC1}, and 6.8 nF for C_{VC2}.

[STEP−11] Channel Management Control

Figure 13 shows the CM pin control with an external voltage signal. The V_{VEA} control voltage is generated by voltage−loop error amplifier and is proportional to average of input power. When V_{CM} is pulled LOW to 0 V, the PFC channel is enabled. When the V_{CM} is pulled HIGH and over 4 V, the channel is disabled. Figure 14 shows that channel 3 is disabled by an external signal when the system is operating at half−load condition.

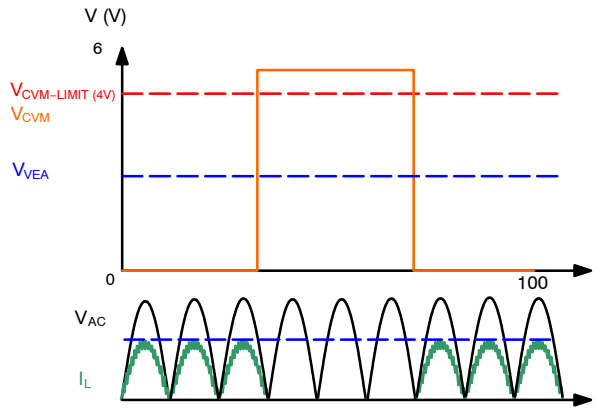


Figure 13. Channel Management by MCU

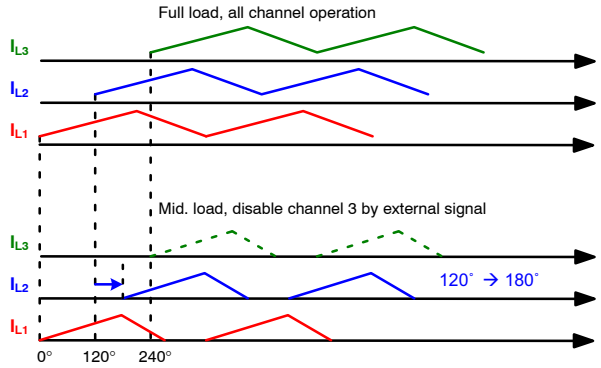


Figure 14. Phase Change of External Signal Control

Figure 15 shows an external circuitry used to change the slope of $V_{CM2/3}$. When $V_{CM2/3}$ is between 4 V ~ 0 V, changing the slope of $V_{CM2/3}$ can affect the overshoot/undershoot of the PFC output voltage during increase/decrease the loading, as shown in Figure 16. This method significantly improves the dynamic load performance of the PFC converter.

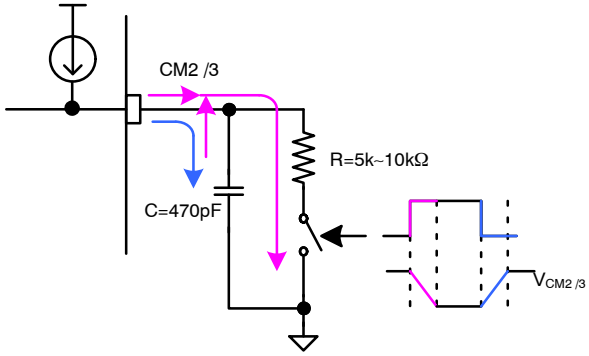


Figure 15. Circuity for Channel Management by MCU

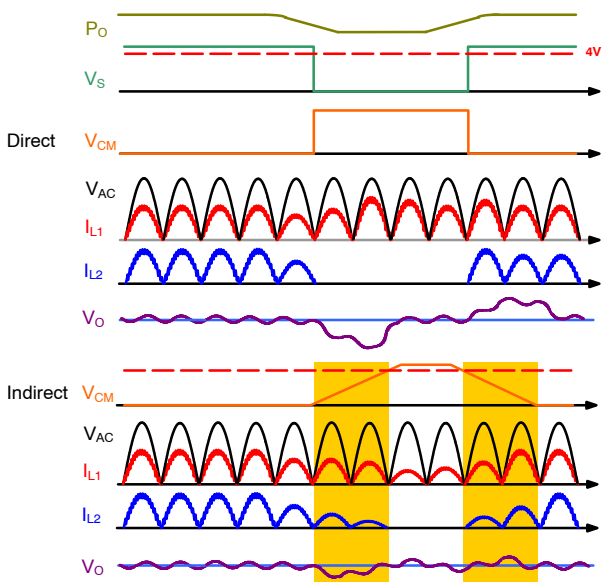


Figure 16. Channel Management by MCU

[STEP−12] Soft Start

Figure 17 shows the soft start (SS) waveform. FAN9673 uses soft−start voltage, V_{SS}, to clamp the PFC power command of voltage loop, V_{VEA}. To increase the soft−start time, the value of the soft−start capacitance C_{SS} can be increased.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{SS}} \quad \text{(eq. 64)}$$

Design Example

Assuming that V_{VEA} is out of clamping by V_{SS} at 5 V, design soft−start time t_{SS} as 100 ms. Since I_{SS} is 20 μA, the required soft−start capacitor value is:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{SS}} = \frac{20 \times 10^{-6} \times 100 \times 10^{-3}}{5} = 0.4\ \mu F \quad \text{(eq. 65)}$$

0.47 μF is selected for C_{SS}.

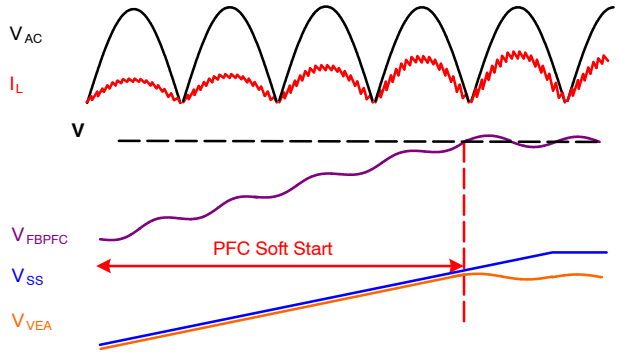


Figure 17. Soft−Start Waveform

[STEP−13] R_{LPK} Setting

The relationship between input voltage and V_{LPK} is shown in Figure 18. The peak−detection circuits identify the V_{IN} information from the I_{AC} current and represent it on V_{LPK} through a ratio. Note that the maximum V_{LPK} can't be over 3.8 V when system operation at maximum AC input.

$$V_{LPK} = \frac{V_{IN.PK}}{100} \times \frac{R_{RLPK}}{12.4k} \quad \text{(eq. 66)}$$

As with the below design example, assume the maximum $V_{IN.PK}$ at 373 V (264 V AC). The relationship of $V_{IN.PK}/V_{LPK}$ is 100, then the V_{LPK} = 3.73 V < 3.8 V.

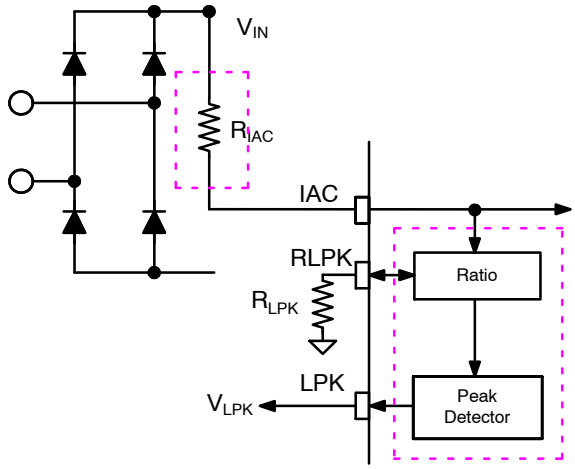


Figure 18. Soft−Start Waveform

Design Example

Assuming the V_{LPK} is 3.73 V when $V_{IN.PK}$ is 373 V, (AC264V):

$$R_{RLPK} = 12.4k \times V_{LPK} \times \frac{100}{V_{IN.PK}} = 12.4\ k\Omega \quad \text{(eq. 67)}$$

[STEP−14] Line Sensing for Brown−In/Out

The FAN9673 has an internal AC UVP comparator that monitors the AC input voltage and disables PFC stage when the V_{BIBO} is less than 1.05 V for 450 ms. If the V_{BIBO} voltage is over 1.9 V/1.75 V, the PFC stage will be enabled. The VIR pin is used to set the AC input range, as shown in Table 2.

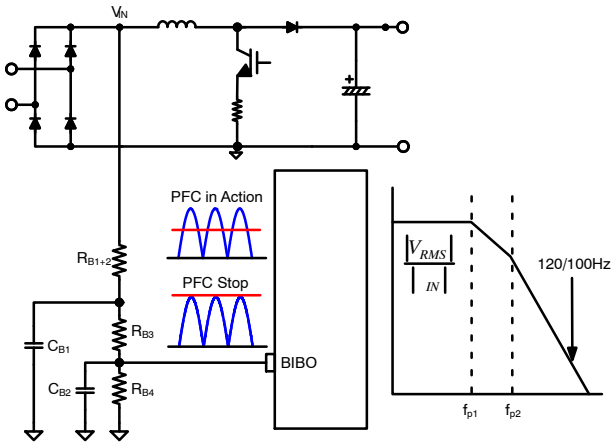


Figure 19. Brown−In/Out Circuits

Table 2. AC INPUT RANGE WITH CONTROLLER SETTING

Input Range	AC (V)	R_{VIR} Setting	R_{IAC} Setting	Brown−In/ Out Level
Full−Range	85 ~ 264	10 kΩ	6 MΩ	AC 85 V/75 V
HV−Single	180 ~ 264	470 kΩ	12 MΩ	AC 170 V/160 V

The FAN9673 senses average value of the input voltage using the BIBO pin as shown in Figure 19. The average value of the input voltage is obtained by an averaging circuit using a low−pass filter with two poles.

The sensing circuit should be designed considering the nominal operation range of line voltage and brownout protection trip point as:

$$V_{BIBO.L} = V_{LINE.MIN} \times \frac{\sqrt{2} \times R_{B4}}{R_{B1+2} + R_{B3} + R_{B4}} \times \frac{2}{\pi} \quad \text{(eq. 68)}$$

$$V_{BIBO.L} + \Delta V_{BIBO} < V_{LINE.BI} \times \frac{\sqrt{2} \times R_{B4}}{R_{B1+2} + R_{B3} + R_{B4}} \quad \text{(eq. 69)}$$

where $V_{LINE.MIN}$ and $V_{LINE.BI}$ are specified brownout/in threshold in r.m.s. value.

When V_{AC} is full range input (universal input), the brown−out/in thresholds $V_{BIBO-FL}$ and $V_{BIBO-FL} + \Delta V_{BIBO-F}$ are 1.05 V and 1.9 V. But if the V_{AC} is high−voltage single−range input (180 ~ 264 V AC), the brown−out/in thresholds of $V_{BIBO-HL}$ and $V_{BIBO-HL} + \Delta V_{BIBO-H}$ become 1.05 V and 1.75 V.

It is typical to set R_{B3} as 10% of R_{B1+2}. The poles of the low−pass filter are given as:

$$f_{P1} \cong \frac{1}{2\pi \times C_{B1} \times R_{B3}} \quad \text{(eq. 70)}$$

$$f_{P2} \cong \frac{1}{2\pi \times C_{B2} \times R_{B4}} \quad \text{(eq. 71)}$$

To properly attenuate the twice line frequency ripple in V_{RMS}, it is typical to set the poles around 10 ~ 20 Hz.

Design Example

The brownout protection thresholds are 1.05 V ($V_{BIBO-HL}$) and 1.75 V ($V_{BIBO-HL} + \Delta V_{BIBO-H}$) respectively. The scaling down factor of the voltage divider is:

$$\frac{R_{B4}}{R_{B1+2} + R_{B3} + R_{B4}} = \frac{V_{BIBO-HL}}{V_{LINE.MIN}} \times \frac{\pi}{2 \times \sqrt{2}} = \frac{1.05}{160} \times \frac{\pi}{2 \times \sqrt{2}} = 7.289\ \text{m} \quad \text{(eq. 72)}$$

The startup of the PFC controller at the minimum line voltage is checked as:

$$\frac{\sqrt{2} \times V_{LINE.BI} \times R_{B4}}{R_{B1+2} + R_{B3} + R_{B4}} = 170 \times \sqrt{2} \times 7.289\ \text{m} = 1.752 > 1.75\ \text{V} \quad \text{(eq. 73)}$$

The resistors of the voltage divider network are selected as $R_{B1} = R_{B2} = 1\ M\Omega$, $R_{B3} = 200\ k\Omega$, $R_{B4} = 16.2\ k\Omega$. To place the poles of the low−pass filter at 15 Hz and 22 Hz, the capacitors are obtained as:

$$C_{B1} = \frac{1}{2\pi \times f_{P1} \times R_{B3}} = \frac{1}{2\pi \times 15 \times 200 \times 10^3} = 53\ \text{nF} \quad \text{(eq. 74)}$$

$$C_{B2} \cong \frac{1}{2\pi \times f_{P2} \times R_{B4}} = \frac{1}{2\pi \times 22 \times 16.2 \times 10^3} = 447\ \text{nF} \quad \text{(eq. 75)}$$

DESIGN SUMMARY

Application	Output Power	Input Voltage	Output Voltage/ Output Current
Single−Stage Three−Channel PFC	5000 W	85 ~ 264 V_{AC}	393 V/12.72 A

Features

- 180V ~ 264 V AC, Three−Channel PFC Using FAN9673
- Switch−Charge Technique of Gain Modulator for Better PF and Lower THD
- 40 kHz Low Switching Frequency Operation with IGBT
- Protections: Over−Voltage Protection (OVP), Under−Voltage Protection (UVP), and Over−Current Protection (I_{LIMIT}), Inductor Saturation Protection (I_{LIMIT2})

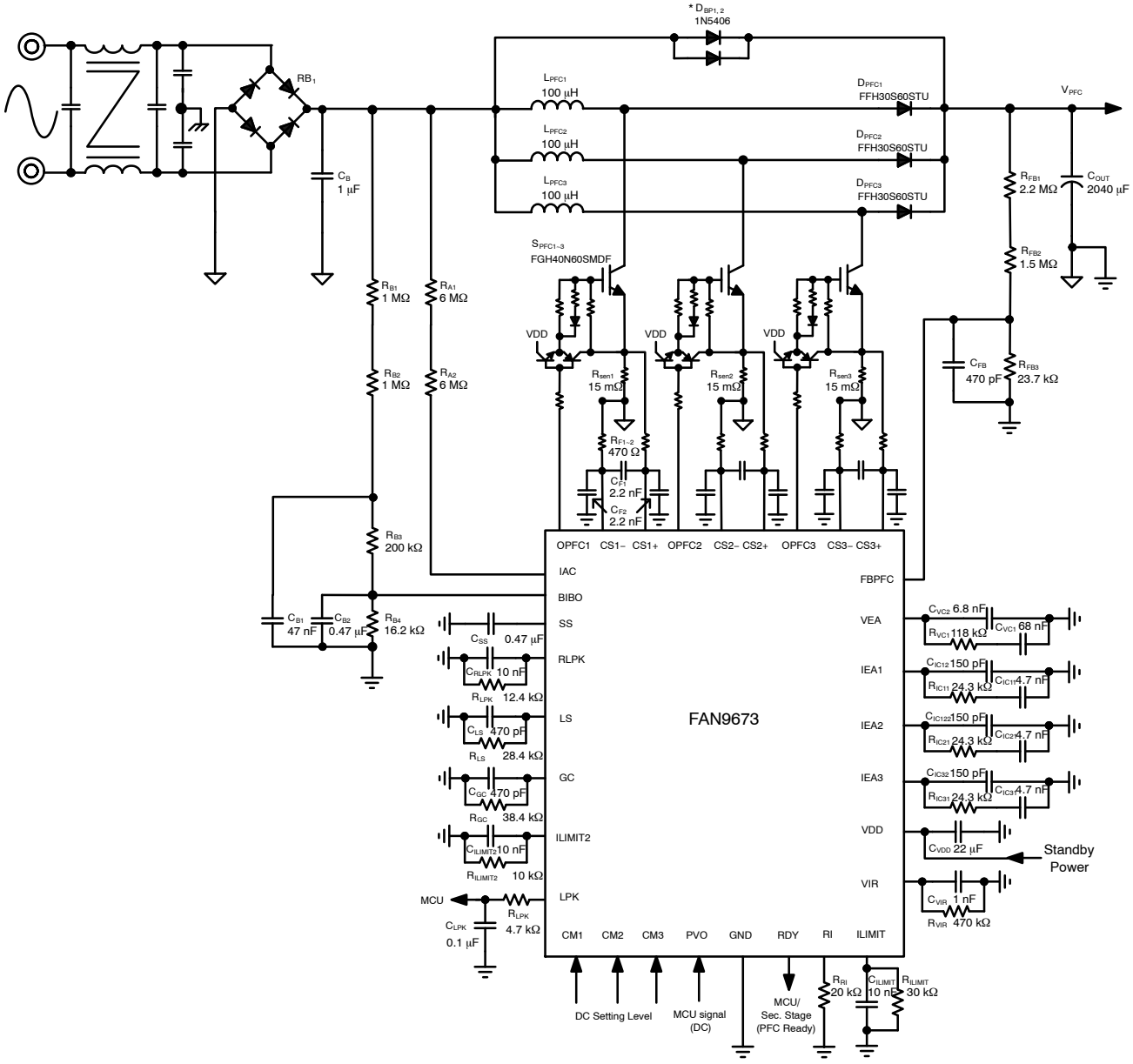


Figure 20. Final Schematic of Design Example

APPENDIX

Table 3. PARAMETERS OF FAN9673 EVALUATION BOARD

V_{DD} Maximum Rating	20 V
V_{DD} OVP	24 V
V_{CC} UVLO	10.3 V/12.8 V
PVO	0 V ~ 1 V
PFC Soft−Start	106 ms
Brown−In/Out	170 V/160 V
V_{FBPFC} for RDY	2.4 V/1.55 V (96% / 62%)

Table 4. MOSFET AND DIODE REFERENCE SPECIFICATION

IGBTs	
Voltage Rating	
600 V (IGBT)	FGH40N60SMDF
Boost Diodes	
600 V	FFH30S60STU

System Design Precautions

- Pay attention to the inrush current when AC input is first connected to the boost PFC convertor. It is recommended to use NTC and a parallel connected relay circuit to reduce inrush current.
- Add bypass diode D_{BP} to provide a path for inrush current when PFC starts up.
- The PFC stage is normally used to provide power to a downstream DC−DC or inverter. It's recommend that downstream power stage is enabled to operate at full load once the PFC output voltage has reaches a level close to the specified steady−state value.
- The PVO function is used to change the output voltage of PFC, V_{PFC}. The V_{PFC} should be kept at least 25 V higher than V_{IN}.

LAYOUT GUIDE

- The current−sense resistor and current−sense filter (C_{F1}, C_{F2}) should be as close to the CS+/CS− pins as possible. (1)
- Similar to other power management devices, when laying out the PCB, it is important to use star grounding techniques and to keep the filter capacitor and control components to the controller IC and its GND pin as close as possible. (2, 3)
- Keep high−current power ground paths separate from the signal ground path. Make a single−point connection from signal ground to the power ground. The single−point connection is preferable to be close to FAN9673's GND and the power ground close to the current−sensing resistors. (4, 5)
- Keep the routing of the current−sense signals and the routing of the single−point ground connection as close as possible.
- Place the external gate drivers close to the power switches. Keep the PCB tracks for the power switches' gate drive short and wide to handle the peak value of gate drive current.
- With non−isolated gate driver, the return path for the OPFC gate drive currents go through the power ground. Minimize the loops between the OPFC driver outputs, external gate−driver buffer transistors, current−sensing resistor, and power ground to avoid inducing noise. That is, keep the controller to the switching devices as close as possible. (6)
- To minimize the possibility of interference caused by magnetic coupling from the boost inductor, the device should be located at least 2.5 cm (1 inch) away from the boost inductor. It is also recommended that the device not to be placed underneath the magnetic components.

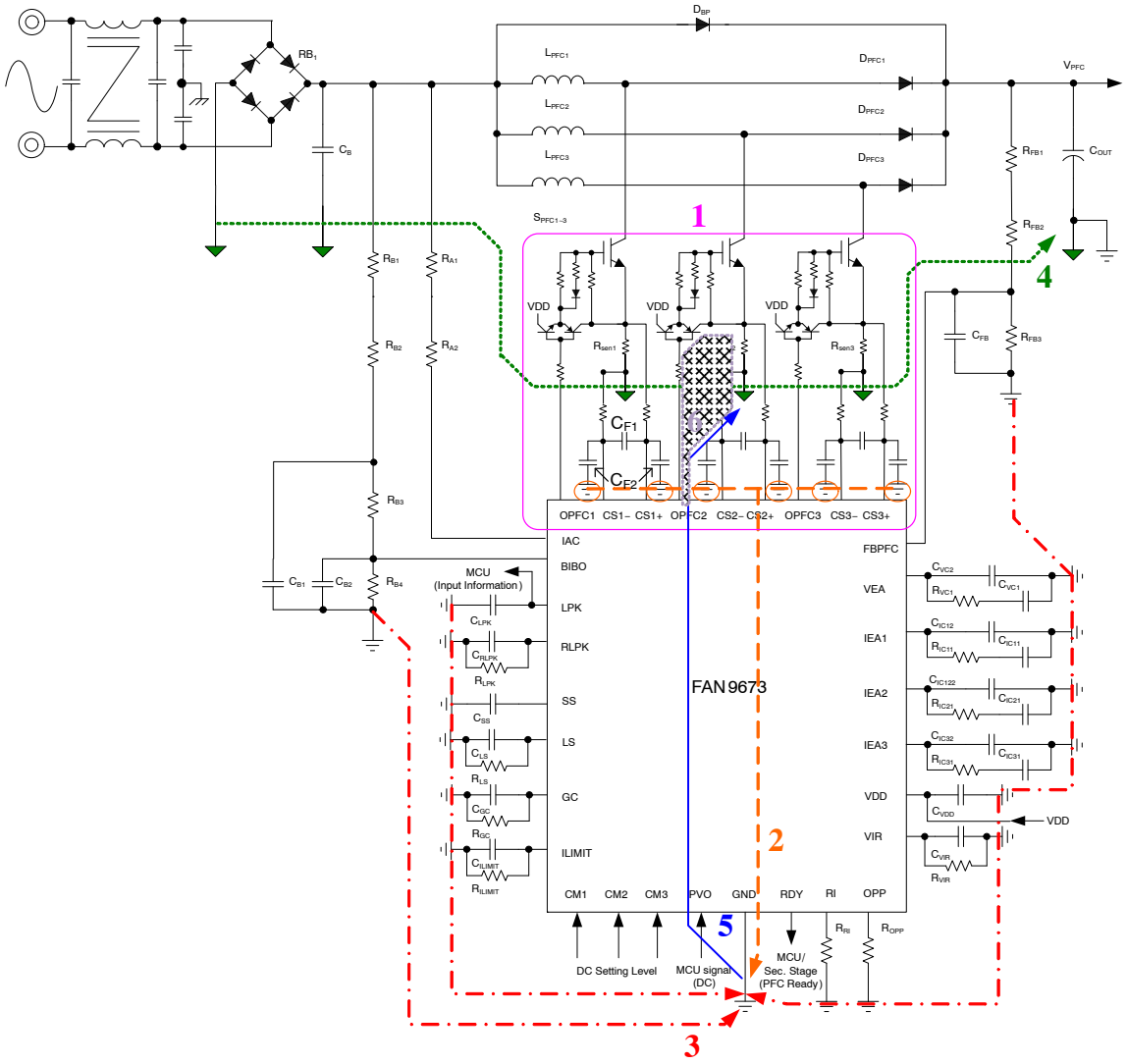


Figure 21. Layout Diagram

RELATED PRODUCT INFORMATION

- FAN9673 – Three Channels Interleaved CCM PFC Controller
- FAN6982 – CCM Power Factor Correction Controller
- AN−8027 – FAN480X PFC+PWM Combo Controller Application

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