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Using Wire-OR Ties in ECLinPS™ Designs

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APPLICATION NOTE

This application note discusses the use of wire-OR ties in EClinPS designs. Theoretical Descriptions of the problems associated with wire-OR ties are included as well as an evaluation and SPICE simulation results. In addition, general guidelines and recommendations are provided to assist the system designer in successfully using wire-OR ties in ECLinPS designs.

INTRODUCTION

The use of wired-OR connections in ECL designs is a popular way to reduce the total part count and optimize the speed performance of a system. The limitations of OR-tying ECL outputs has always been a combination of increased delay per OR-tie, and the negative going disturbance seen at the output when one output switches from a high to a low state while the rest of the outputs remain high. As the speed of the output transition times increase, the latter problem becomes the primary limitation on the practice of OR-tying ECL outputs. This fact is due to the sensitivity of this phenomena to decreasing output transition times.

This application note will address the practice of OR-tying outputs in the implementation of designs using the ECLinPS family of logic devices. A theoretical description of the problem, as well as evaluation and simulation results, will be presented. In addition, guidelines will be offered which, if followed, will help to ensure the desired operation of ECLinPS designs using wired-OR outputs.

THEORETICAL DESCRIPTION

Figure 1 illustrates a typical wire-OR situation. For simplicity, the discussion will deal with only two outputs; however, the argument could easily be expanded to include any number of outputs. If both the A and the B outputs start in the high state, they will both supply equal amounts of current to the load. If the B output then transitions from a high to a low, the line at the emitter of B will see a sudden decrease in the line voltage. This negative going transition will continue downward at the natural transition time of the output until the A output responds to the voltage change and supplies the needed current to the load. This lag in the time it takes for A to correct the load current and return the line to a quiescent high level is comprised of three elements: the natural response time of the A output, the delay associated with the trace length between the two outputs, and the time it takes for the signal to propagate through the package. The trace delay can be effectively forced to zero by OR-tying adjacent output pins. The resulting situation can then be considered “best case.” In this best case situation, if the delay through the package is not a significant portion of the transition time of the output, the resulting negative going glitch will be relatively small as the response time for A to provide the extra current is only slightly larger than the time it takes for B to turn off. However, in the world of ECLinPS devices, even the small delays associated with the 28-lead PLCC package are a significant portion of the transition time of an ECLinPS output. As a result, the best case situation for an ECLinPS device in an OR-tied application will create a significantly larger negative going glitch than previous slower ECL families.

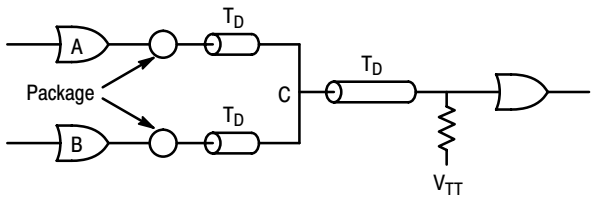


Figure 1. Typical Wire-OR Configuration

EVALUATION AND SIMULATION RESULTS

To gauge the magnitude of the “best case” wire-OR glitch for an ECLinPS device, a laboratory analysis was completed. Two adjacent pins were OR-tied on an ECLinPS device and the glitch was monitored under several different input conditions. The plots of Figure 2, Figure 3, and Figure 4 illustrate the results from this analysis. To further test the theory, a delay was added between the two outputs (1/2” semi-rigid coaxial cable) and the glitch was monitored under the same input conditions.

As can be seen in Figure 5, Figure 6, and Figure 7, the magnitude of the glitch is significantly larger with this relatively small amount of delay added between the OR-tied outputs. Also of interest was the dependence of the magnitude of the glitch on the amount of time *both* outputs are in the high state.

To get an explanation of this phenomena and also generate recommended guidelines for OR-tying ECLinPS outputs, SPICE simulations were run to facilitate examining different external conditions as well as monitoring behaviors internal to the device. To simulate worst case conditions, a worst case model was developed. Using nominal values for the device parameters, the package model was fine tuned so that the simulation results correlated very closely with the evaluation results. The model parameters were then adjusted to give a worst case transition time of 275 ps. This model was then used to generate all of the simulation results in this document.

Figure 8 shows the behavior of the current flowing from the outputs under a wire-OR condition. In the plot, both outputs start in a low state with each output supplying half the load current. One of the outputs then switches high and supplies all of the current to the load until the other output also switches to the high state. Theoretically, when the second output switches high, the load current should be shared equally between the two outputs. However, as seen in Figure 8, because of the parasitics of the package and the output device, the current takes a significant amount of time to equalize between the two outputs. Once one of the outputs switches back low, it takes very little time for the remaining high output to supply the needed current to the load.

Because of this time constant like equalization of the output currents, the magnitude of the wire-OR glitch will be dependent on the amount of time both outputs are in the high state before one switches low. If an output switches low while it is supplying more than half the current, the glitch will be larger than if the output switches low while supplying less than half of the current. If more than 3 ns pass before one of the outputs switches low, the currents will equalize and the glitch will be of a nominal magnitude; this magnitude will be insensitive to times greater than 3 ns. Therefore, to look at the worst case situation, the glitch should be monitored with an output supplying the majority of the load current switching from a high to a low state. Figure 9, Figure 10, and Figure 11 illustrate the results of simulating the wire-OR glitch when two adjacent pins are tied together. These plots clearly show the dependence of the magnitude of the disturbance with the time both outputs are in the high state.

With a dependence established between the size of the glitch and the amount of current being switched, one would expect the size of the glitch to be somewhat dependent on the termination resistance. In particular, one would expect the glitch to be reduced for increasing termination resistance. Figure 12, Figure 13, and Figure 14 illustrate the results of terminating into 100 Ω, rather than the normal 50 Ω termination. The magnitude of the glitch is indeed smaller. In addition, the high load resistance results in a higher V_{OH} and thus an extra level of high end noise margin. Terminating into a higher resistance results in both a reduction in the magnitude of the glitch and an increase in the noise margin of the receiving device.

The next goal of the simulation exercise is to determine how much trace delay between outputs can be tolerated without adversely affecting the operation of a design. From Figure 1, the only time delay of importance is the delay from point C to the output which must supply the additional current to the load. The delay from point C to the load is common to both the negative transition and the correcting positive transition and thus has no effect on the magnitude of the glitch. Likewise, the delay between the output turning off and point C will have no effect on the glitch as this path is also common among the trip to the load and the correcting output. Therefore, if one of the outputs will always be turning off first, the terminating line should be started as close to the other output as possible to minimize the magnitude of the disturbance. If, however, the output turning off first is random, the termination carrying line should be connected at the midpoint of the trace connecting the two outputs, Figure 1, so that the worst case disturbance will be minimized. By tapping into the midpoint of the trace connecting the two outputs, the effective delay between outputs is only half of the total delay of the trace connecting the outputs.

Simulations were run with time delays between the outputs of 50 ps and 100 ps representing typical 1/2” and 1” lines respectively when implemented per Figure 1. Figure 15 through Figure 20 represent the results of these simulations. Note that the extra delay added to the simulations, although relatively small, have a large impact on the magnitude of the generated voltage glitch.

The question remains at what point will the disturbance resulting from wire-O–Ring outputs start to create problems in a system. There are two cases which can cause problems: the magnitude of the glitch can be large enough to enter the threshold region of the receiving device, or the glitch can cause a setup time failure of a flip flop connected to the line. The first phenomena will typically prove damaging only if the receiving device is using the OR-tie as a clock input; in which case false clocking could occur. For combinational logic, unless the disturbance goes all of the way through the threshold region, a highly unlikely situation, the disturbance will be attenuated at each gate it passes through. Figure 21, Figure 22, and Figure 23 illustrate the attenuation of the glitch after passing through one additional gate. Notice that for the situation of OR-tying adjacent pins, time delay = 0, the glitch is completely attenuated by the receiving gate. If the receiving gate V_{BB} switching reference is at the upper end of the specification range a larger portion of the glitch will be propagated for the same trace delay between outputs (Figure 24).

As the vast majority of designs are eventually synchronized to a clock through a flip-flop, the second failure mode will usually prove to be the limiting factor.

There are three transitory states for an OR-tied line: a low to a high transition, a high to a low transition and the previously discussed glitch condition. The designer has necessarily allowed for the setup times for the two normal transition cases, therefore, as long as the glitch case does not create a transient which extends in time beyond either of the two normal transitions the setup times of the clocked devices will be maintained. However, if the glitch is of sufficient magnitude to push the transient voltage out in time such that it appears at a time later than a normal transition, the specified setup time of a device could be violated. This argument becomes clearer when shown pictorially. Referring to Figure 25, Figure 26, and Figure 27, one can see that for the adjacent pin case the glitch transient is always inside the envelope created by the other two transitions; however, when a delay is introduced between the outputs this is not the case. For both the 50 ps and 100 ps delay cases, the transient voltage moves outside the envelope. In the case of the 50 ps delay, the transient remains in the envelope inside the threshold region and thus will not cause a problem when clocking the subsequent device. The 100 ps delay case, on the other hand, shows the glitch to lie well outside the envelope inside the threshold region and very well could cause a setup time violation of the next stage. One item to note, if there are further stages of combinational logic between the OR-tie and the flip flop input the glitch attenuation will alleviate the setup problem even in the 100 ps delay case.

As time delays between outputs grow larger, another potential problem begins to enter the picture. In addition, to the glitch growing in both magnitude and duration, significant ringing starts to occur as the trace connecting the two outputs starts to look more and more like an unterminated stub. Figure 28 and Figure 29 show the SPICE response for 150 ps and 250 ps time delays respectively. Note the increased waveform degradation with increasing distance between OR-tied outputs.

DESIGN GUIDELINES

General guidelines and recommendations in the area of wire-ORed outputs can be difficult due to the myriad of combinations of different termination, loading, clocking and other design variables. To push the use of OR-tied outputs to its fullest capabilities, designers are encouraged to use the ECLinPS I/O SPICE Modeling Kit (ON Semiconductor Application Note AN1503/D) to run SPICE level simulations on the interconnect of their proposed designs, thus taking into account all of the peculiarities and idiosyncrasies of their systems. In this way, the designer will be able to extend the guidelines mentioned below.

For a conservative approach to OR-tying ECLinPS outputs, the following guidelines can be used:

1. First OR-tying of clock lines should be avoided as even in the best case situation the disturbance on the line is significant and could cause false clocking in some situations.

2. Wire-ORed outputs should be from the same package and preferably should be adjacent pins. If non-adjacent pins or different packages are to be OR-tied, they should be within 1/2” of each other with the load resistor connection situated near the midpoint of the trace (Figure 1).

3. If possible, the termination resistance of the OR-tied line should be made higher than the standard 50W to both reduce the magnitude of the glitch and add to the high end noise margin of the interconnect.

By following these guidelines, the practice of wire-O–Ring ECL outputs can be extended to the ECLinPS family without encountering performance problems in the system.

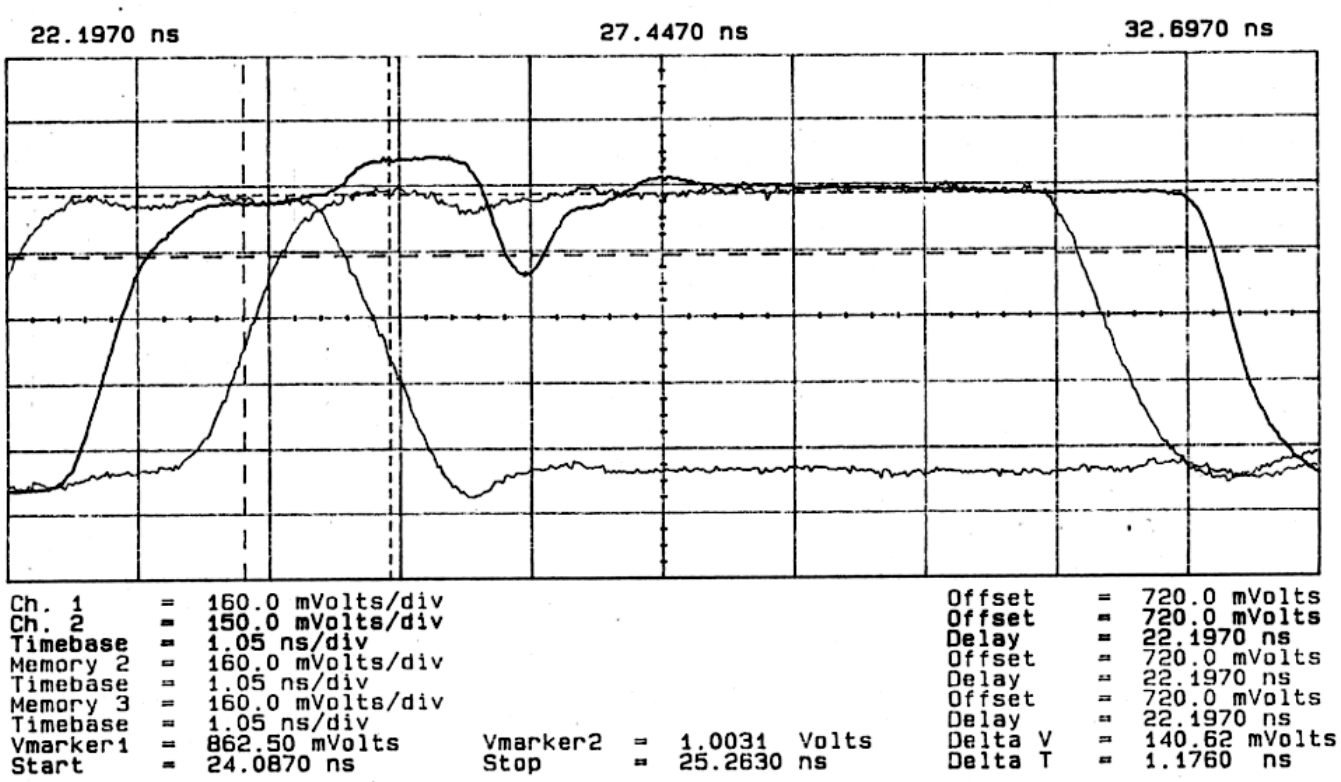


Figure 2.

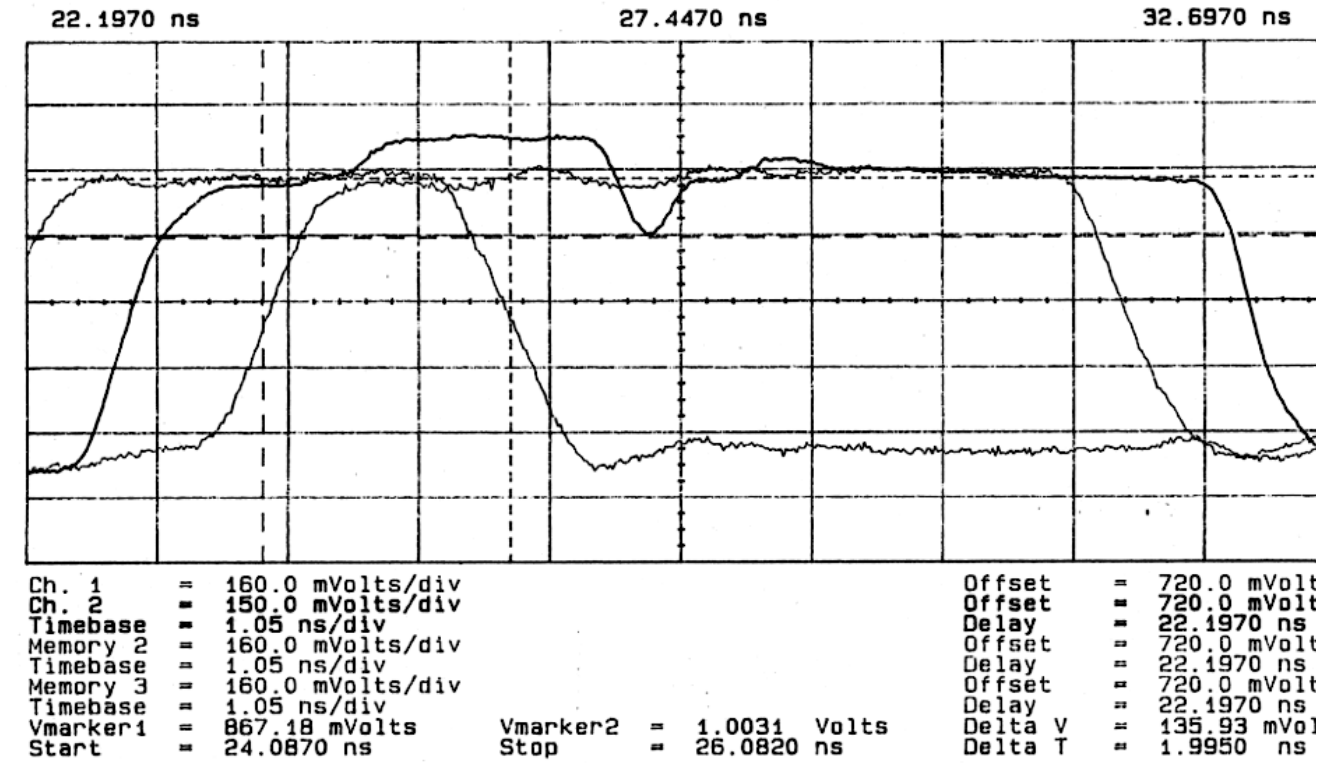


Figure 3.

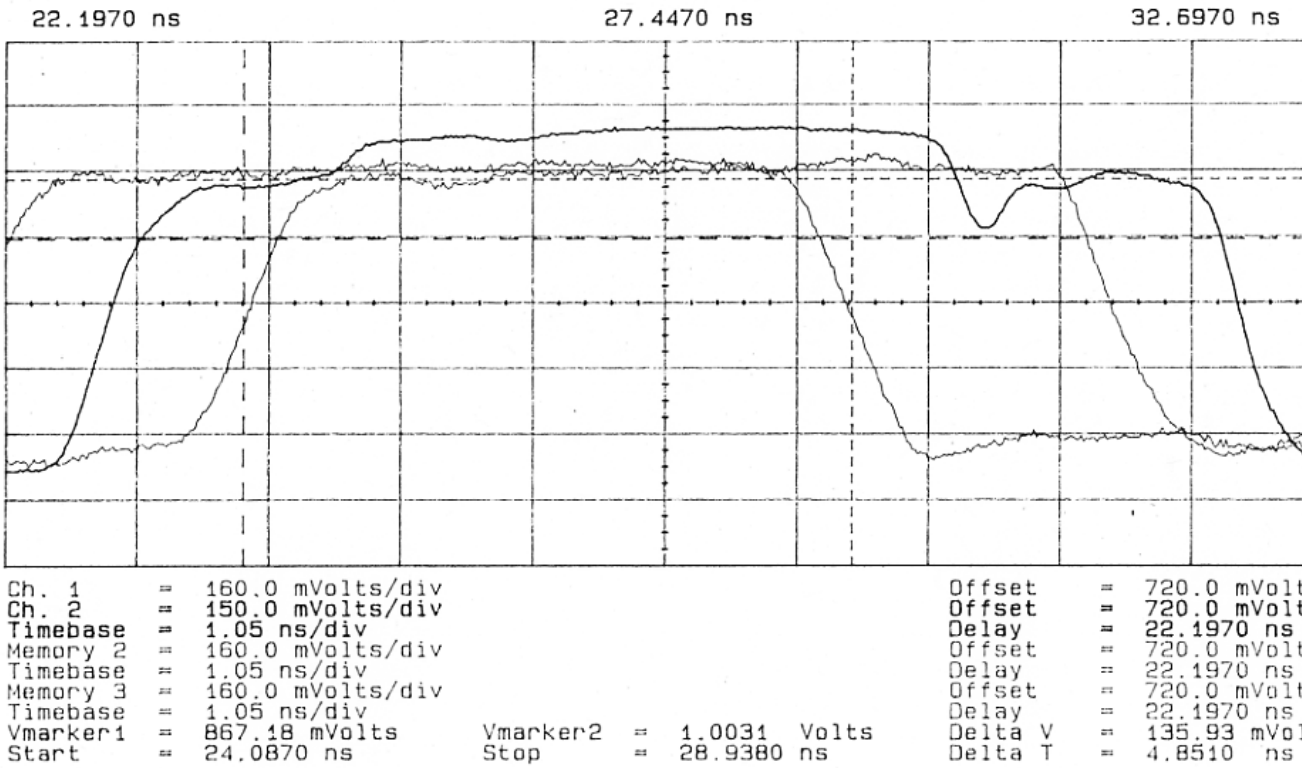


Figure 4.

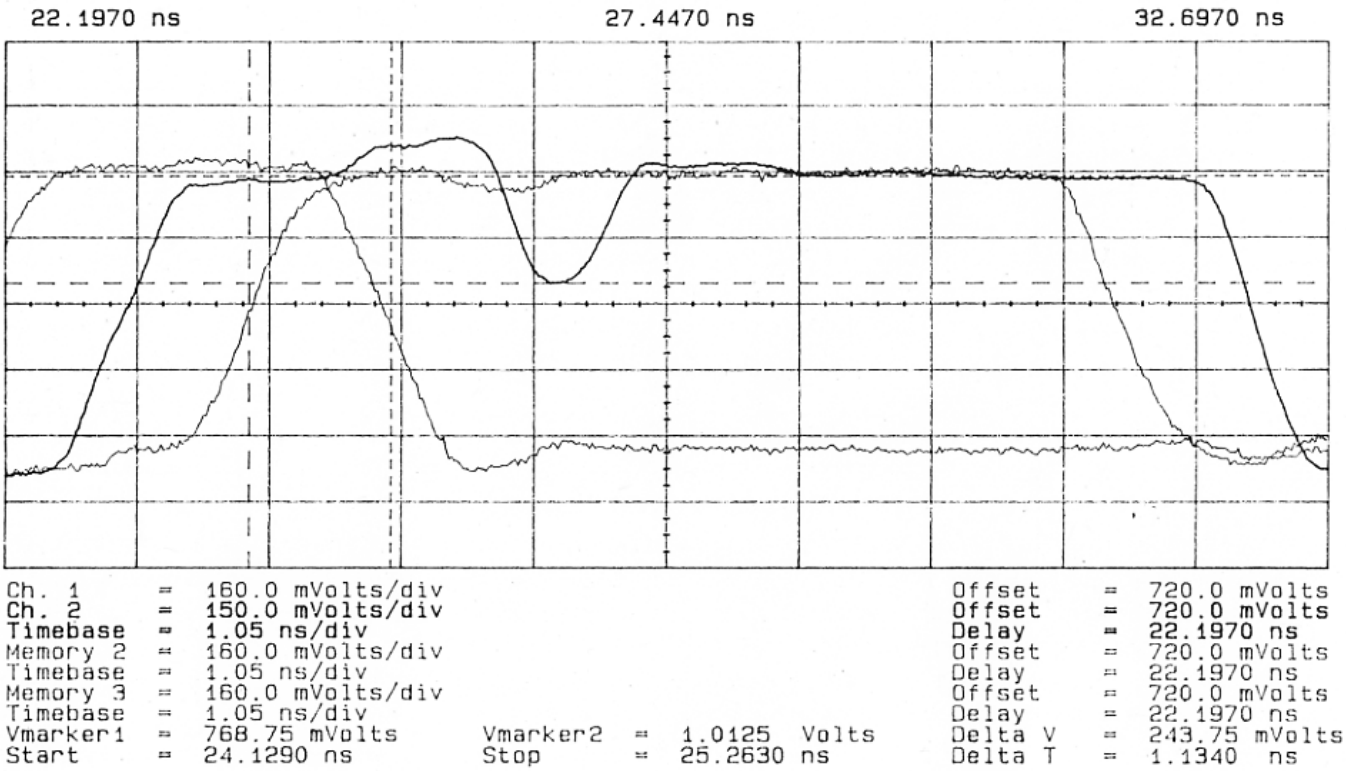


Figure 5.

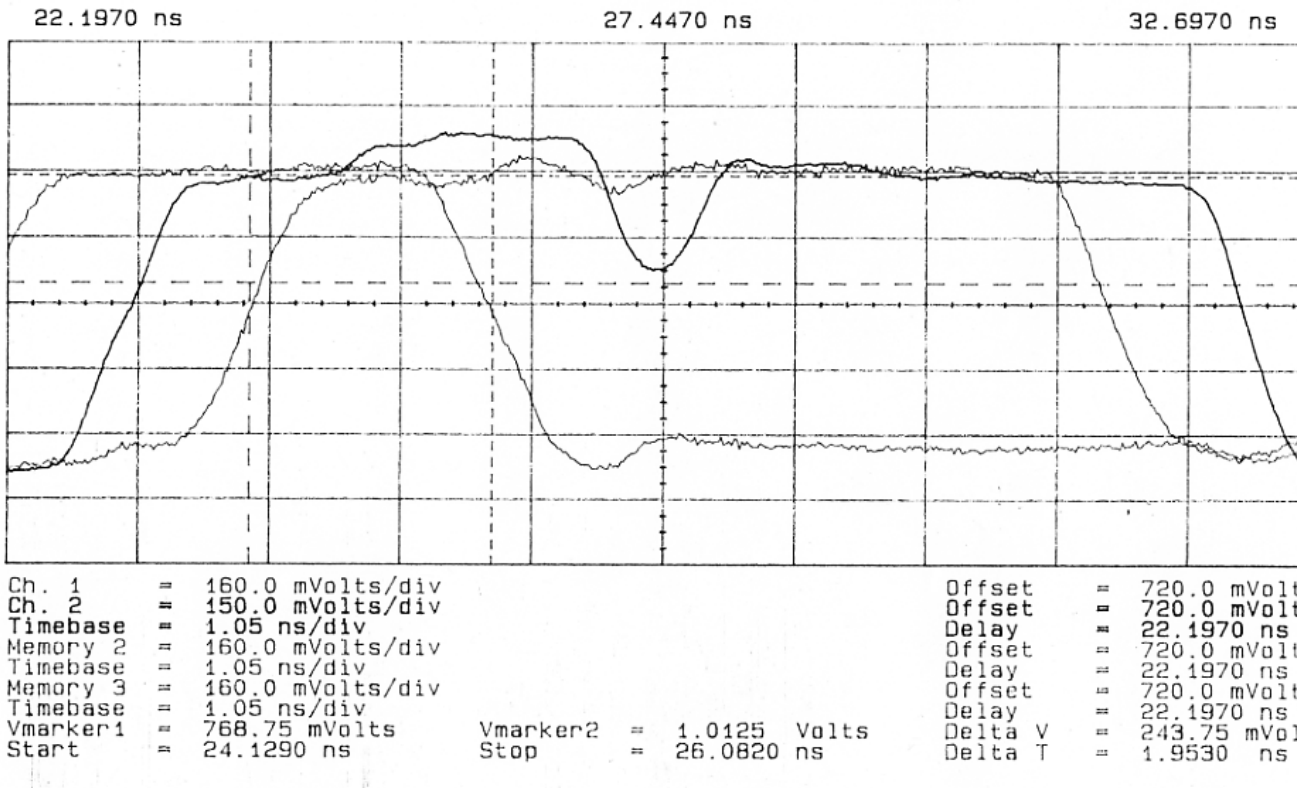


Figure 6.

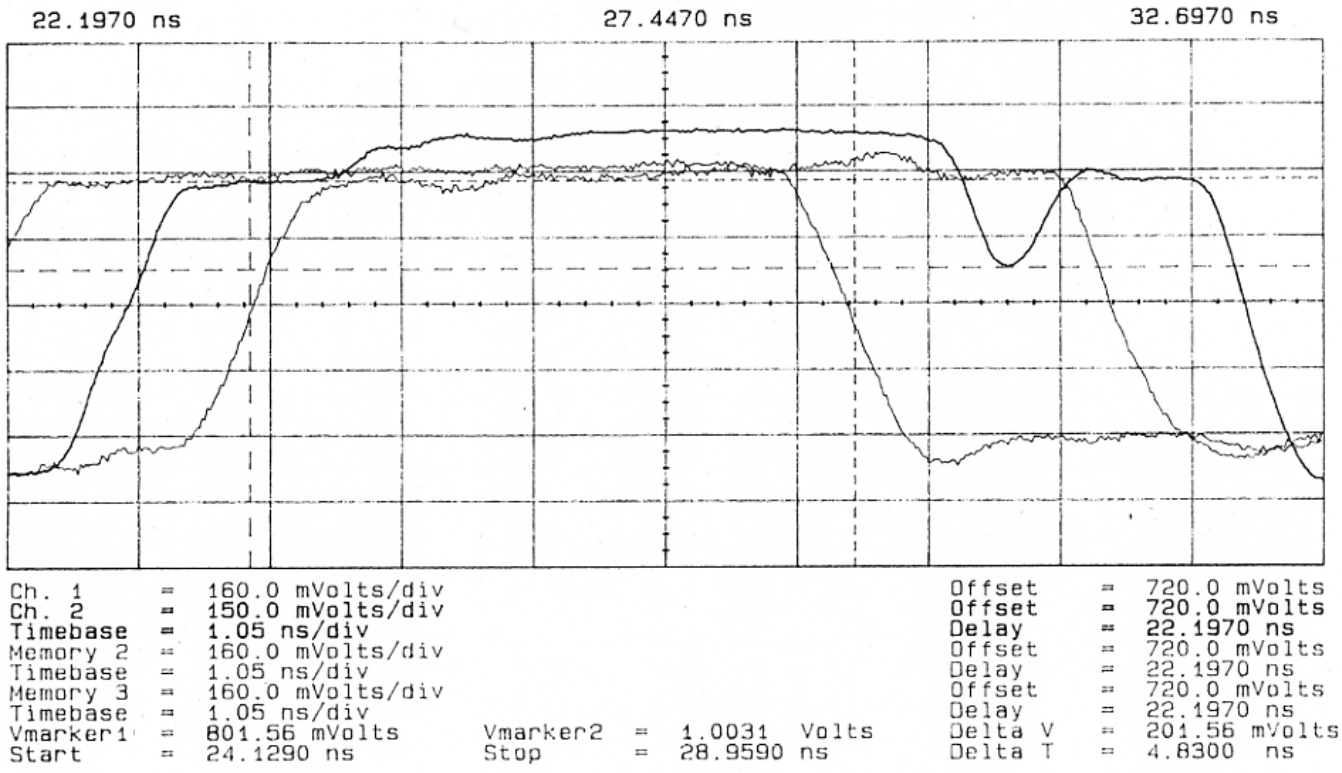


Figure 7.

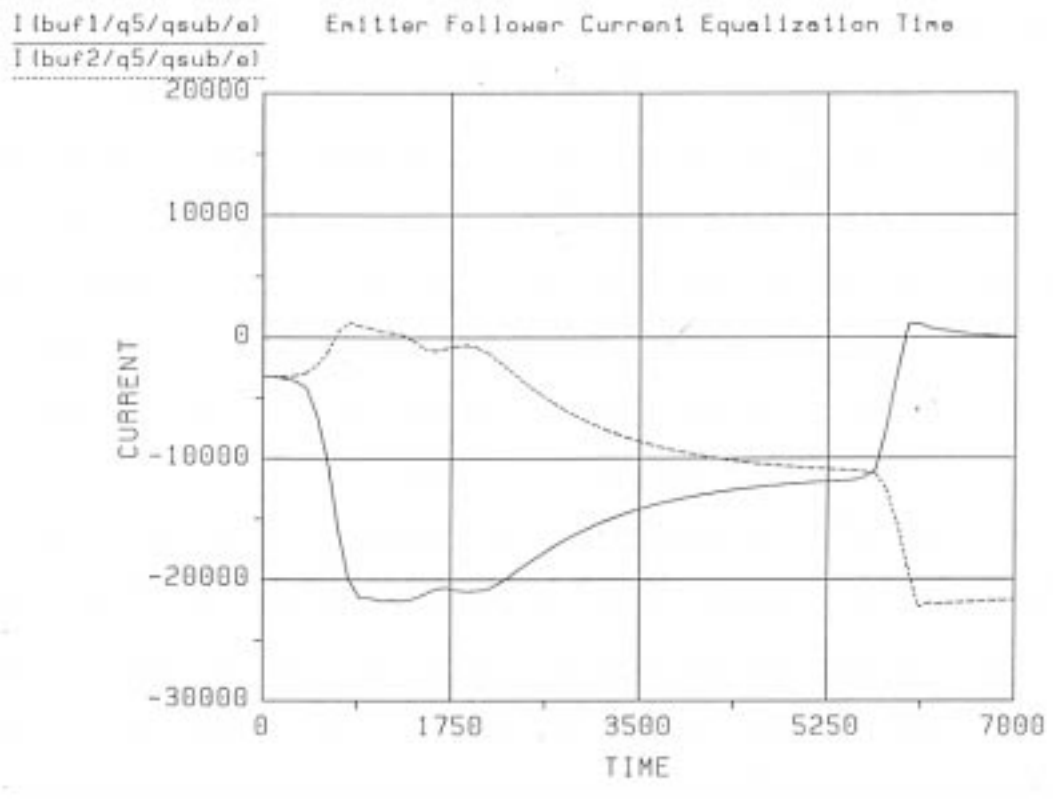


Figure 8.

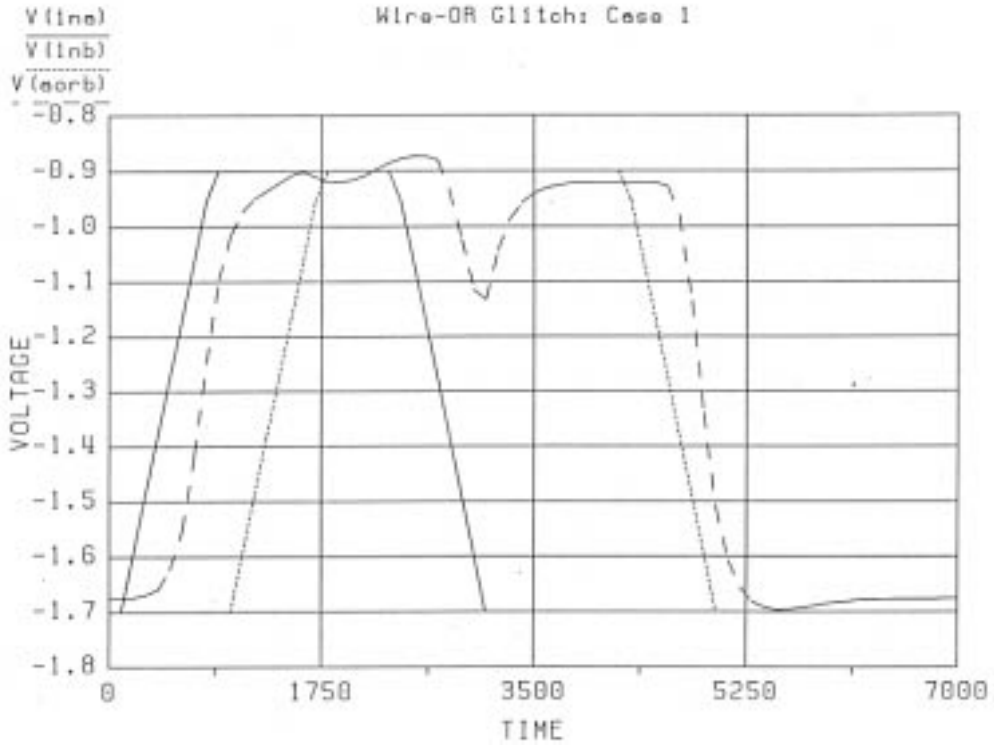


Figure 9.

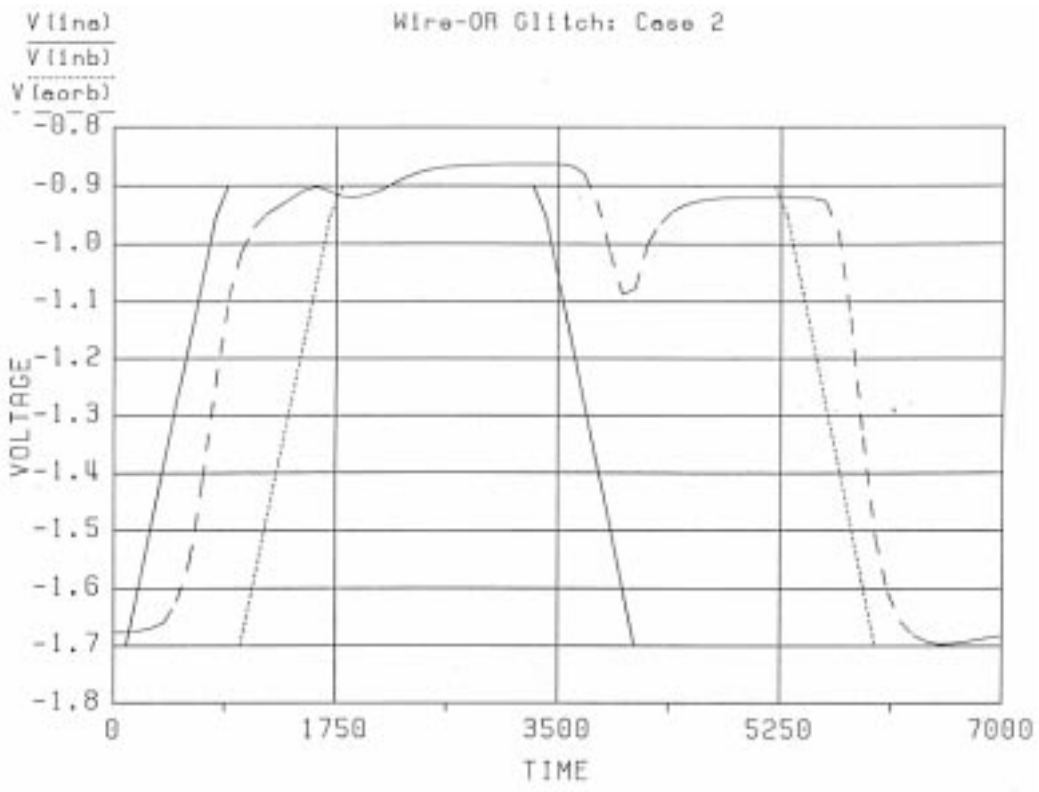


Figure 10.

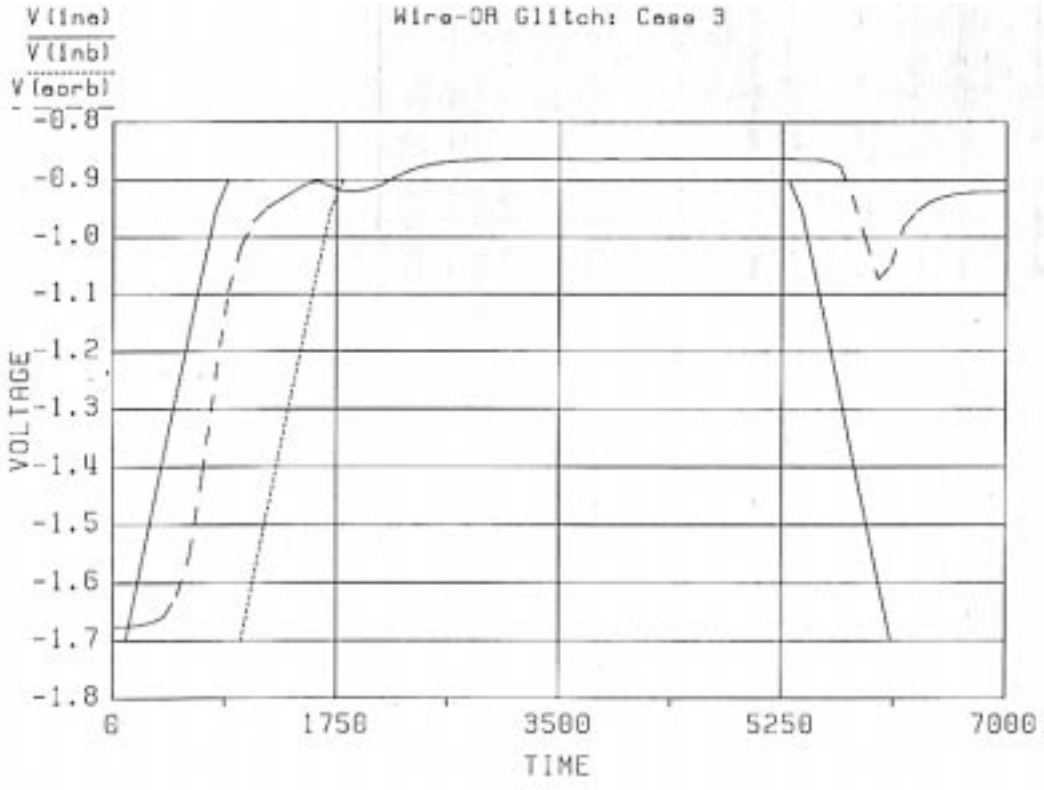
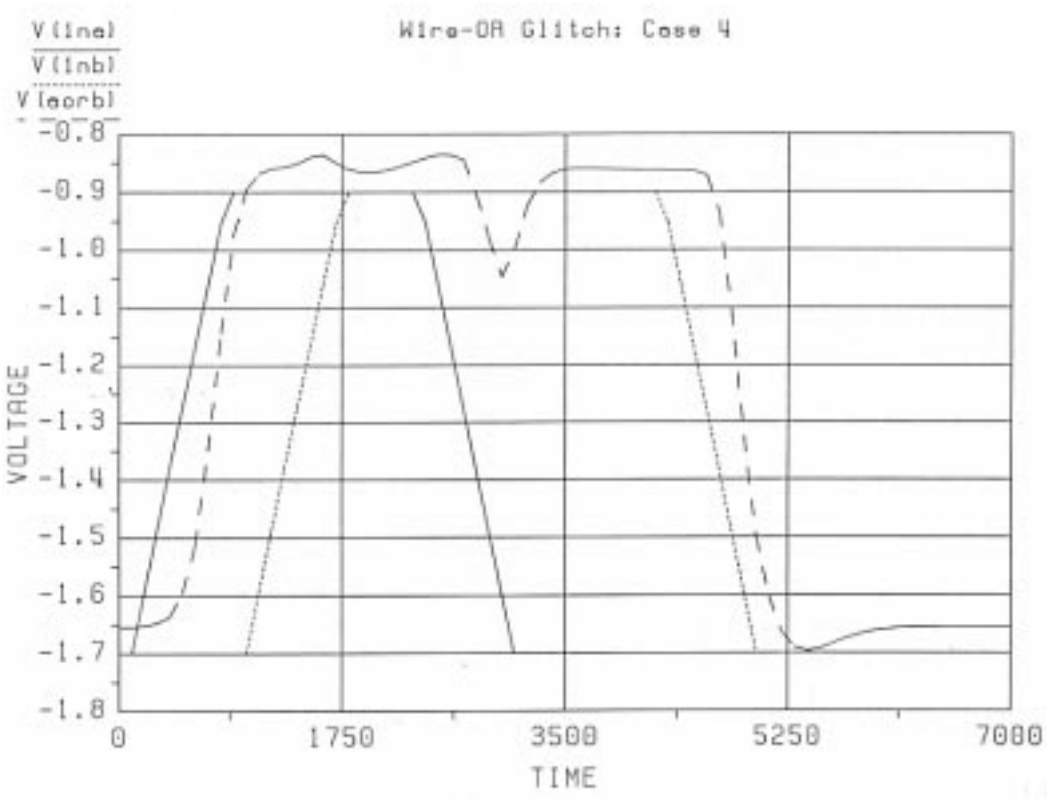


Figure 11.



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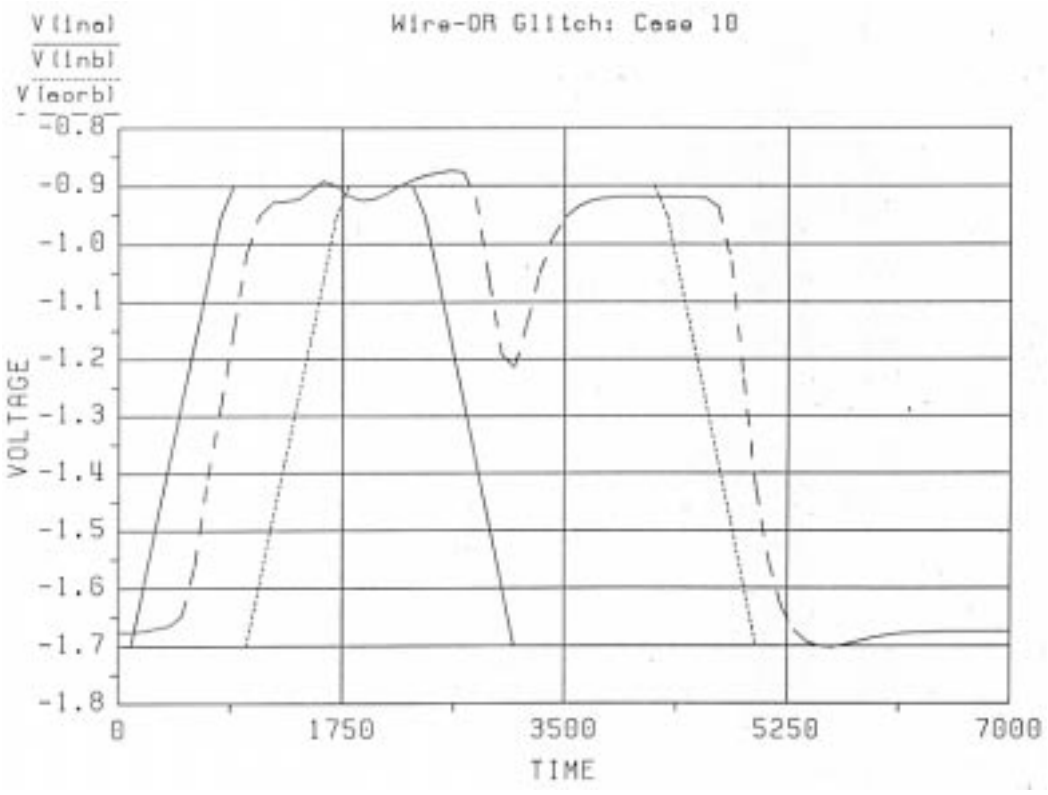
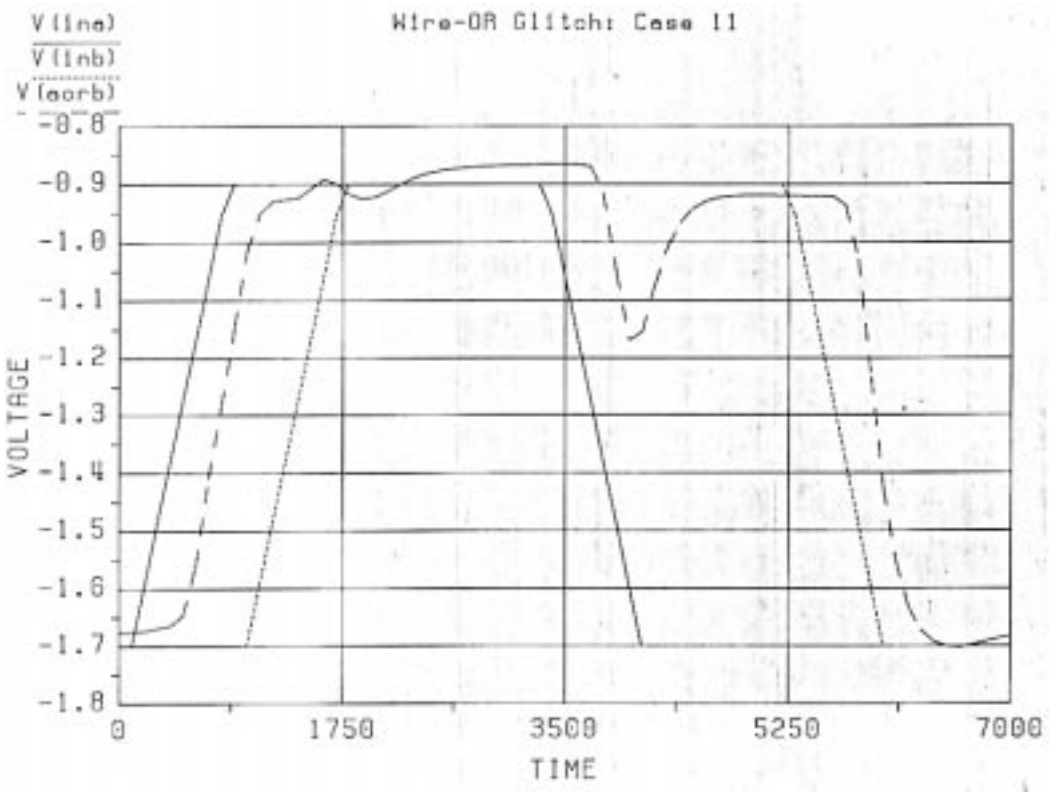


Figure 15.



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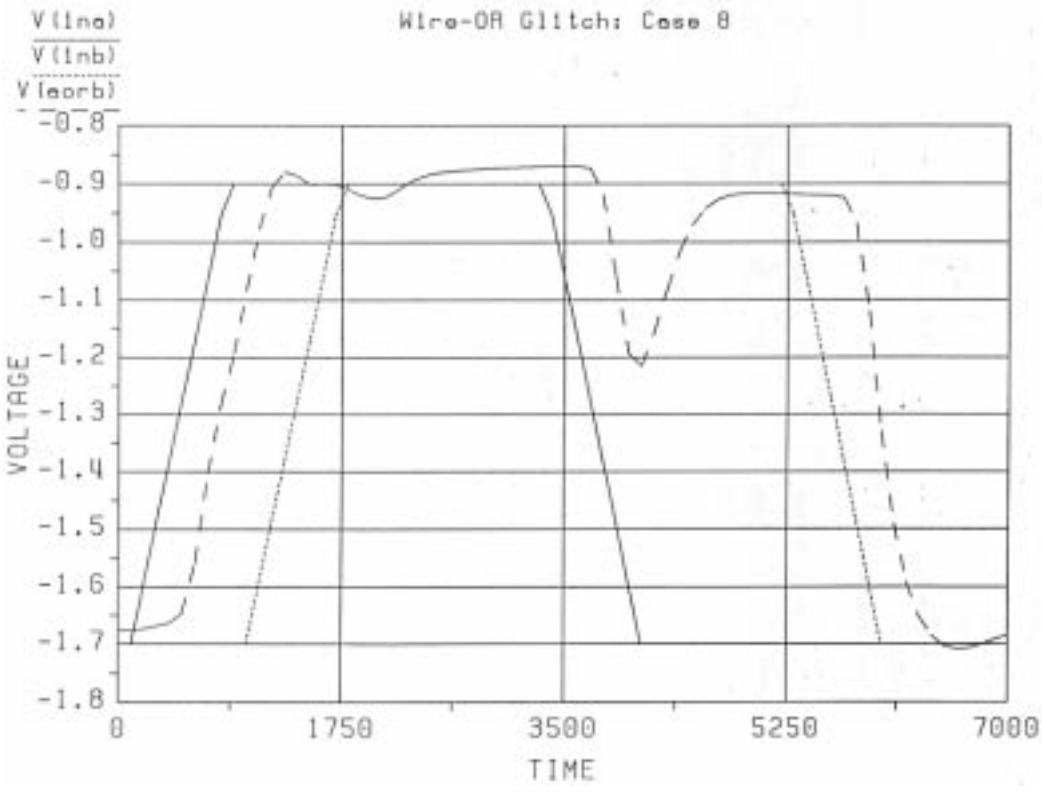

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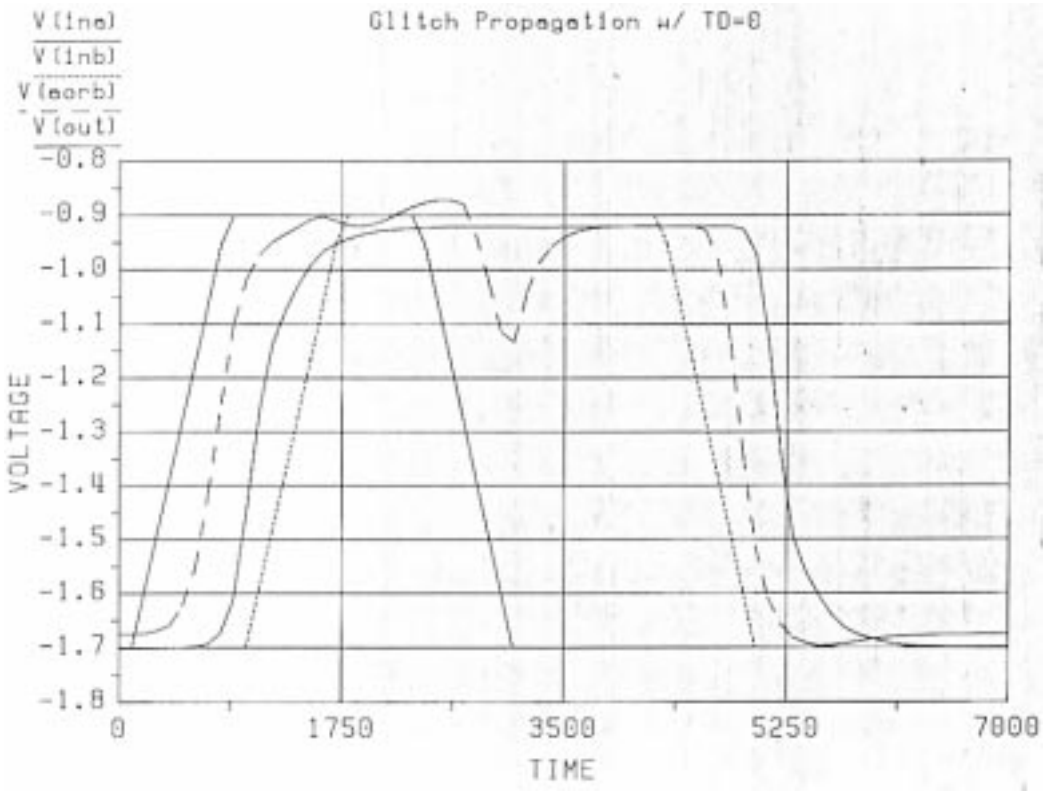


Figure 21.

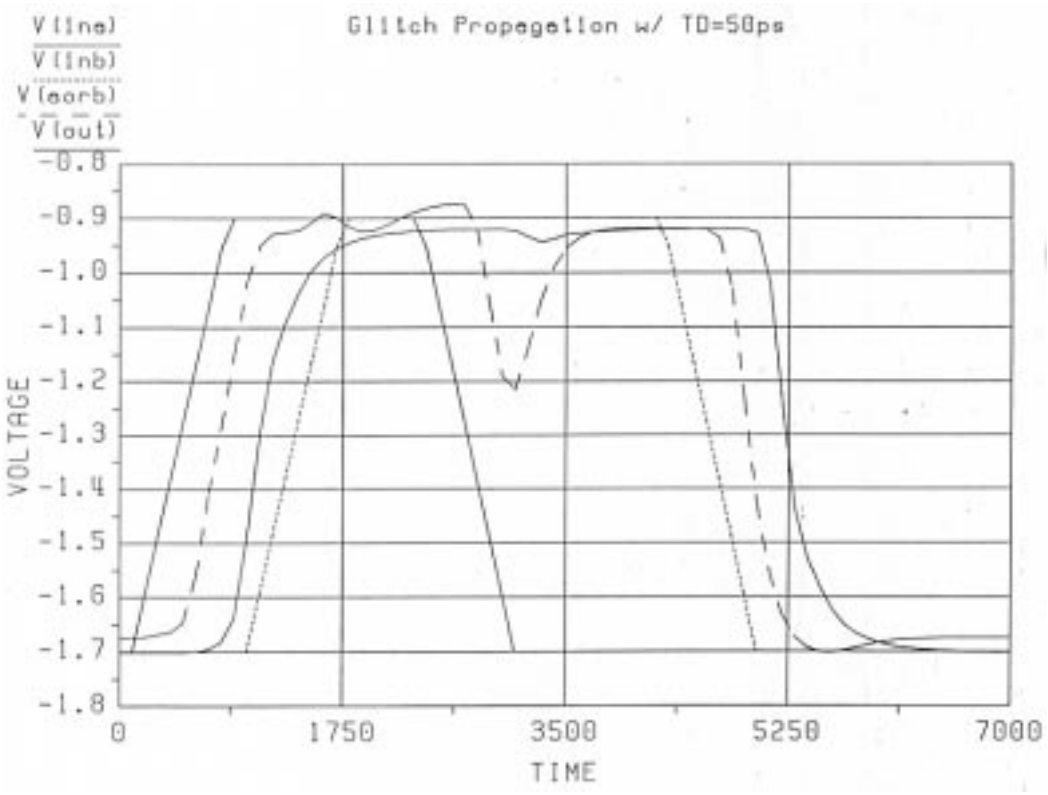


Figure 22.

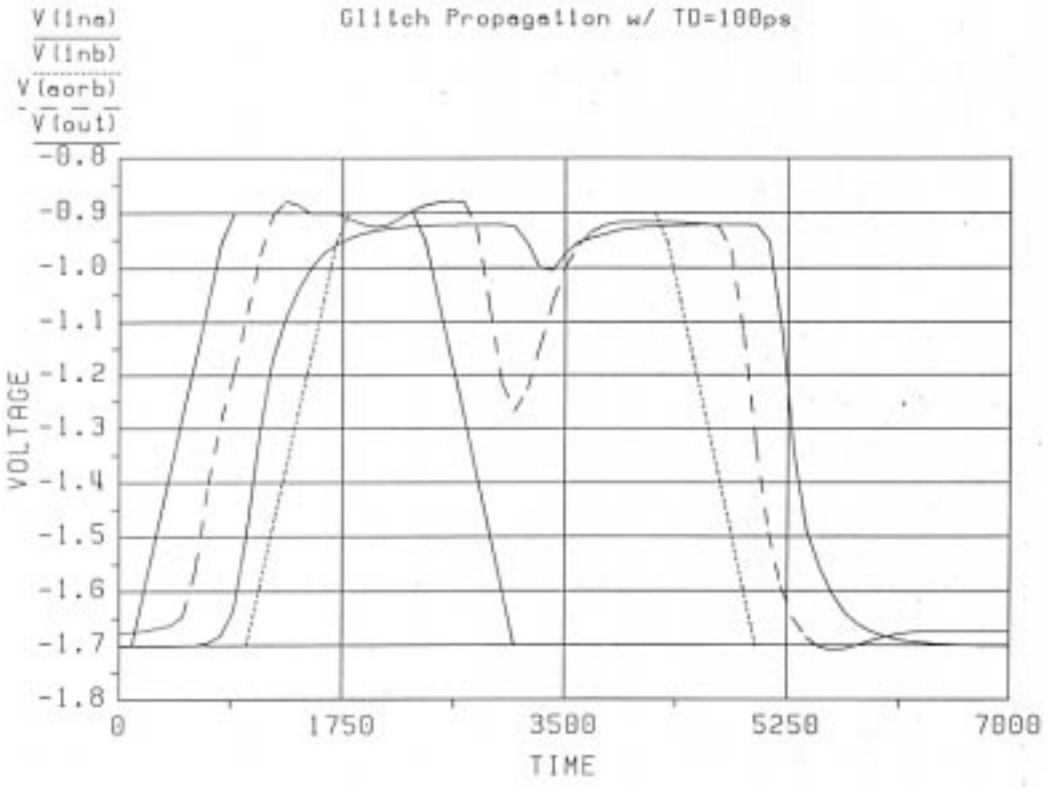


Figure 23.

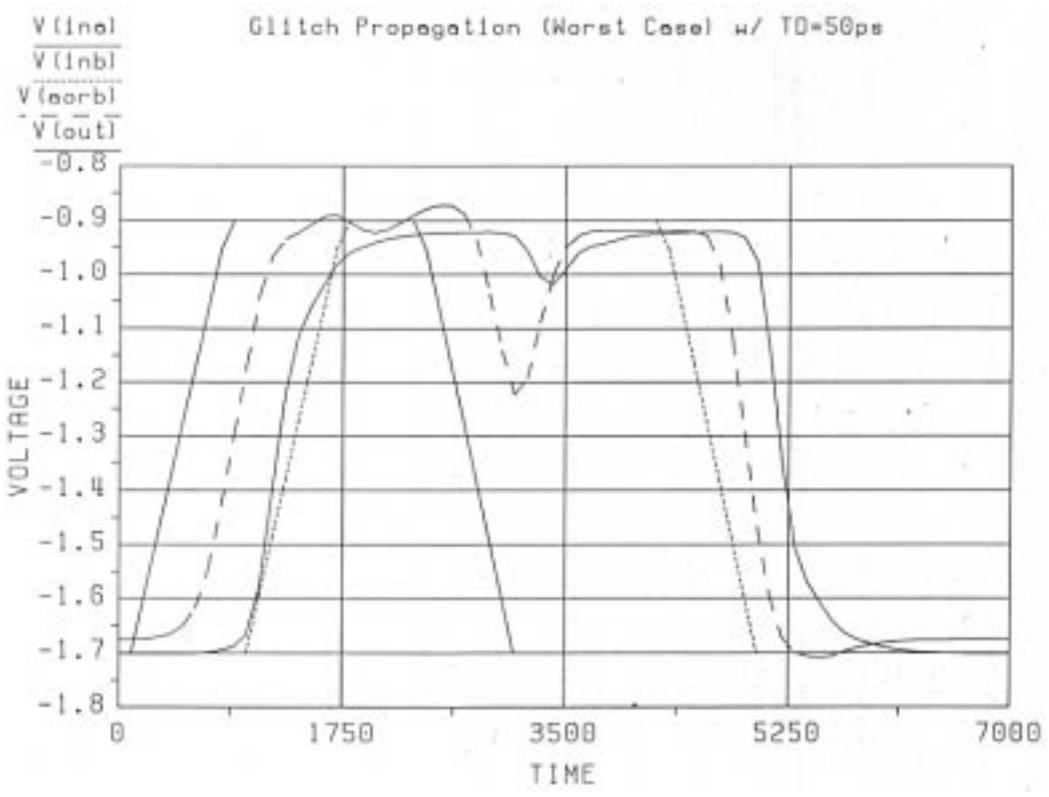


Figure 24.

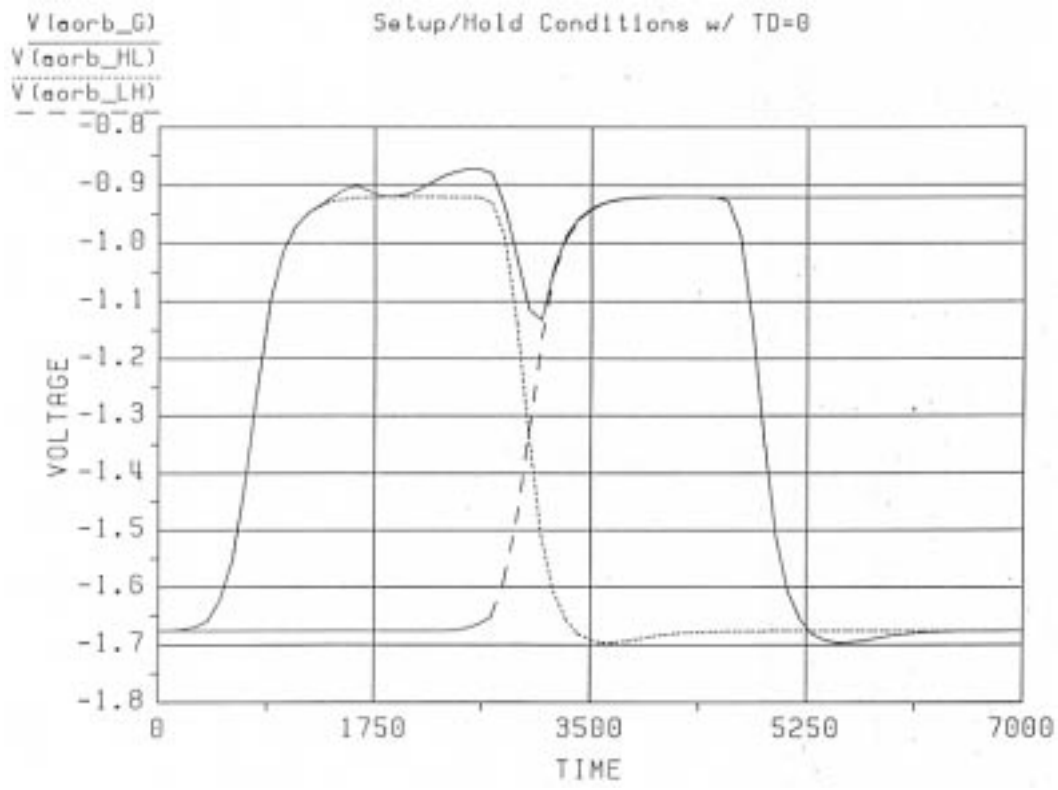


Figure 25.

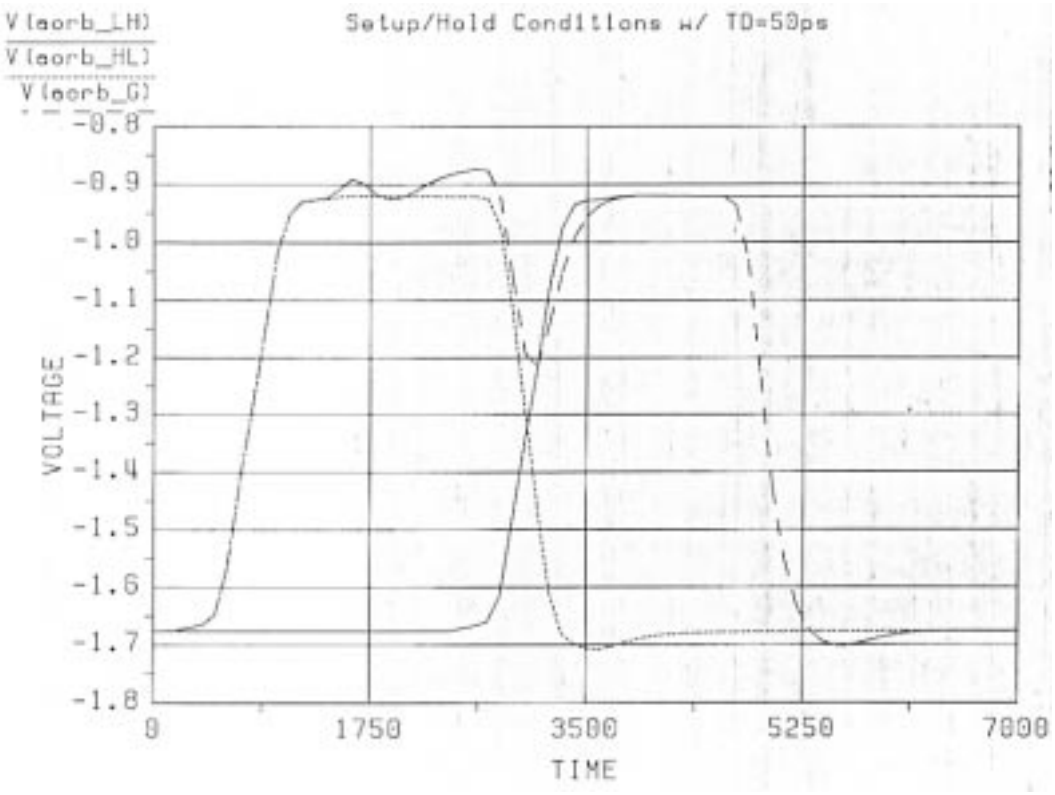
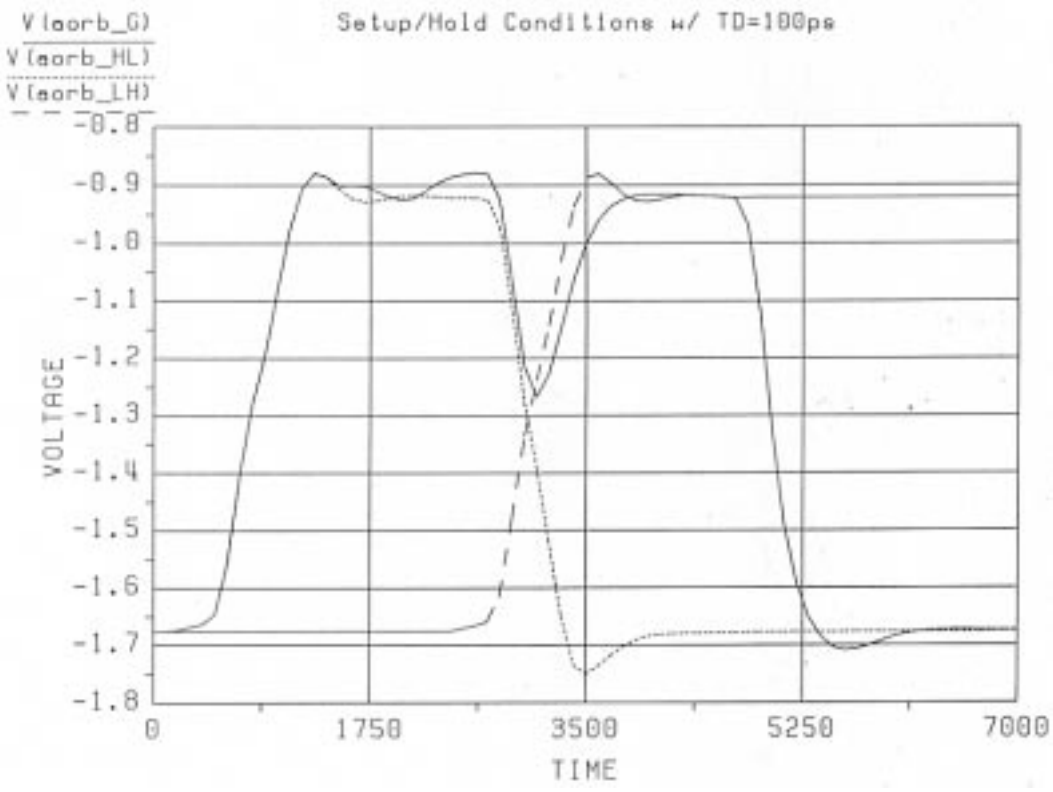


Figure 26.



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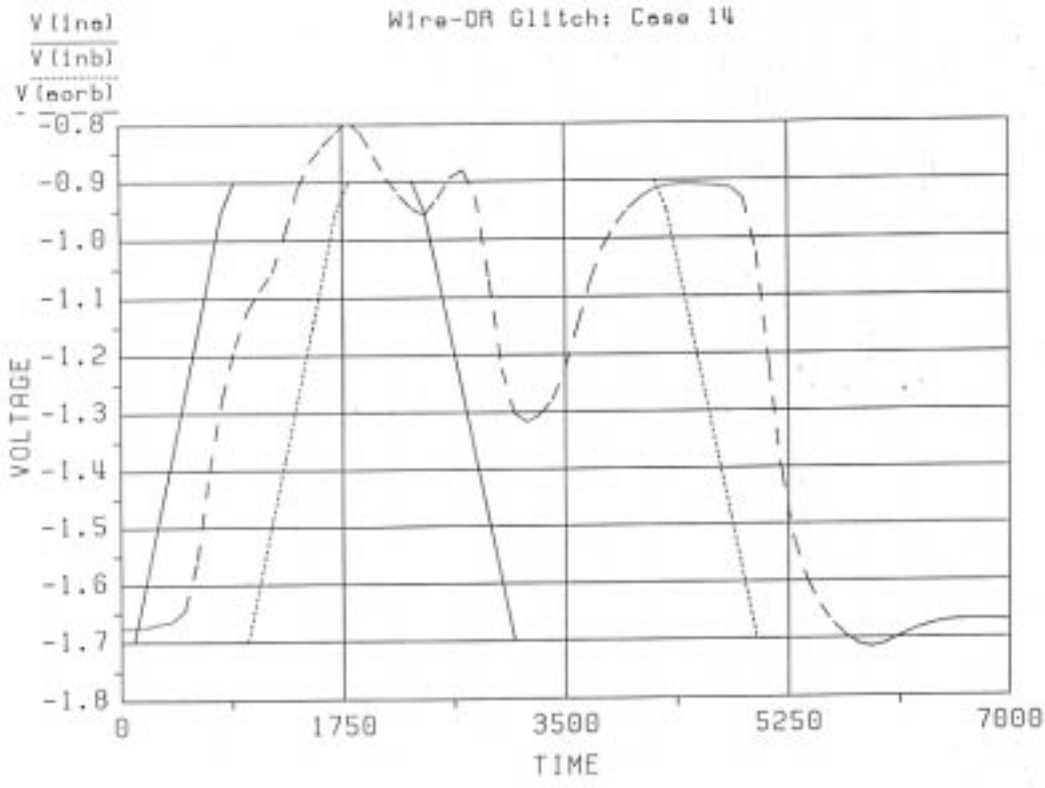

Figure 29.

Notes

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