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# AN1596/D

# ECLinPS Lite™ Translator ELT Family SPICE I/O Model Kit

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**APPLICATION NOTE**

## Introduction

The objective of this kit is to provide customers with enough schematic and SPICE parameter information to perform system level interconnect modeling with the ECLinPS Lite Translator ELT family. The ELT devices MC10ELT2xD and MC100ELT2xD are single or dual supply 1 or 2 Bit translators between the TTL and ECL world. Single supply devices translate between TTL and PECL, dual supply devices translate to or from negative supplied ECL. All devices are designed as 100K compatible 100ELT2x or as 10H compatible 10ELT2x.

The family specifications are located in the High Performance ECL Data book DL140/D. Section 3 represents the temperature and power supply variations that can be expected from the family.

The kit contains representative schematics and model files for the I/O circuits used by the ELT devices. In addition a worst case package model schematic is included for more accurate system level modeling. The package model should be placed on all external inputs, outputs and supply pins.

This note includes the schematics necessary to do I/O modeling and the model text−files.

## Input and Output Schematics

One schematic represents the PECL inputs of single supply translators Figure 1, subcircuit PECL_IN. The translation function of the dual supply ECL−TTL−Translator MC10/100ELT25 is represented in Figure 2 ECL_TTL_ELT25. This translator requires a BVOHH reference signal. It is generated in the BVOHH−generator (Figure 2a).

The TTL−(P)ECL Translator function uses separate circuits for PECL and ECL outputs in 10ELT− or 100ELT version shown in Figures 3 and 4 and subcircuits TTL_ECL_100K, TTL_ECL_10H, TTL_PECL_100K, TTL_PECL_10H.

The 10ELT and the 100ELT version of the (P)ECL outputs are identical beside the temperature compensation network included in the 100ELT−type output.

To simulate the TTL outputs the schematic Figure 5 TTL_OUT is used. The bias regulators ETXR, Figure 6 and VCLP, Figure 7 are necessary to generate reference signals. Replacing those subcircuits by voltage/current sources would result in incorrect output modeling.

All inputs and outputs of the ELT family are protected by ESD protection circuitry. The ESDPD subcircuit (Figure 8) is used for ECL and PECL inputs. It contains ESD protection and the standard ECL 75kΩ input pulldown resistors. The ESD circuit of Figure 9 is used for TTL I/Os and the ECL/PECL outputs.

If the user would like to just simulate the output behavior of an TTL output the TTL_OUT circuit can be stimulated with internal signals.

To all external pins the package model PKG8 drawn in Figure 10 needs to be added.

If users want to reduce simulation time and just simulate 1 channel or only the output of a circuit, they need to take care of the correct power supply management. The channels share power supply pins. Dynamic ICC current will add up at power pins. When a simulation is performed with only one channel, the package models of the power pins need to be adjusted. The parasitic capacitance should be divided by two and inductance should be doubled.

## Modeling

The bias driver schematics for VBB and VCS generation are not included in this kit, as they are unnecessary for interconnection simulation. In addition their use would result in a relatively large increase in simulation time. Alternatively the internal reference voltages should be driven with ideal constant voltage sources.

| Parameter | Typical Level | Worst Case |
|---|---|---|
| VBB | VCC−1.325 | Data Book |
| VCS | VEE+1.3V | ±50mV |

This model kit is intended for simulations within the specified power supply range. If supply voltages drop below minimum specification, VBB and VCS can no longer be assumed to be constant. Thus this model kit can not been used for power up or power down simulations.

For all schematics the resistors should **NOT** be simulated as simple SPICE resistors. Because these resistors are realized by a diffusion step in wafer processing there are parasitic capacitance associated with each like shown in Figure 11. The capacitance is a function of the resistor value.

| | | |
|---|---|---|
| R<2500Ω | CJ0=4.72E−16*R+58E−16 | |
| R>2500Ω | CJ0=0.265E−16*R+29E−16 | |
| R=50kΩ | CJ0=0.1149pF | input pulldown resistor |

In the model file, 3 subcircuits are used: RES for resistor values <2.5kΩ, RESK for R>2.5kΩ and RPD for the input pulldown resistors. As the parasitic capacitance of the Diode is a function of the resistivity, the capacitance needs to be calculated. As calculations of model parameters are not equal for each SPICE simulator, model files are available for H−SPICE and Berkeley SPICE (P−SPICE). If the user's tool is not able to work with one of those files, they need to be adapted.

Beside the resistor models this kit contains all process parameters and all subcircuits (Figure 12 to Figure 20) necessary to simulate the ELT devices.

The Global nodes in the model files and the schematics are:

| | |
|---|---|
| VCC | Top rail power supply |
| VCCP | PECL VCC voltage |
| VCCT, VCC | TTL VCC voltage |
| VEE | Bottom Rail Power supply |
| PGND | Ground for PECL signals |
| VBB | Switching Bias Voltage |
| VCS | Current Source Base Voltage (VEE+1.3V) |
| VCLMP | VCS+0.8V |
| SUB | Substrate contact. Most negative supply voltage |
| VTT | External termination sink supply (VCC−2V) |
| In | Input |
| InB | Inverted Input |
| Q | Output |
| QB | Inverted Output |

For typical load ECL and PECL outputs should be terminated 50Ω to VTT=VCC−2V. TTL outputs are loaded with 20pF to GROUND and 500Ω to GROUND.

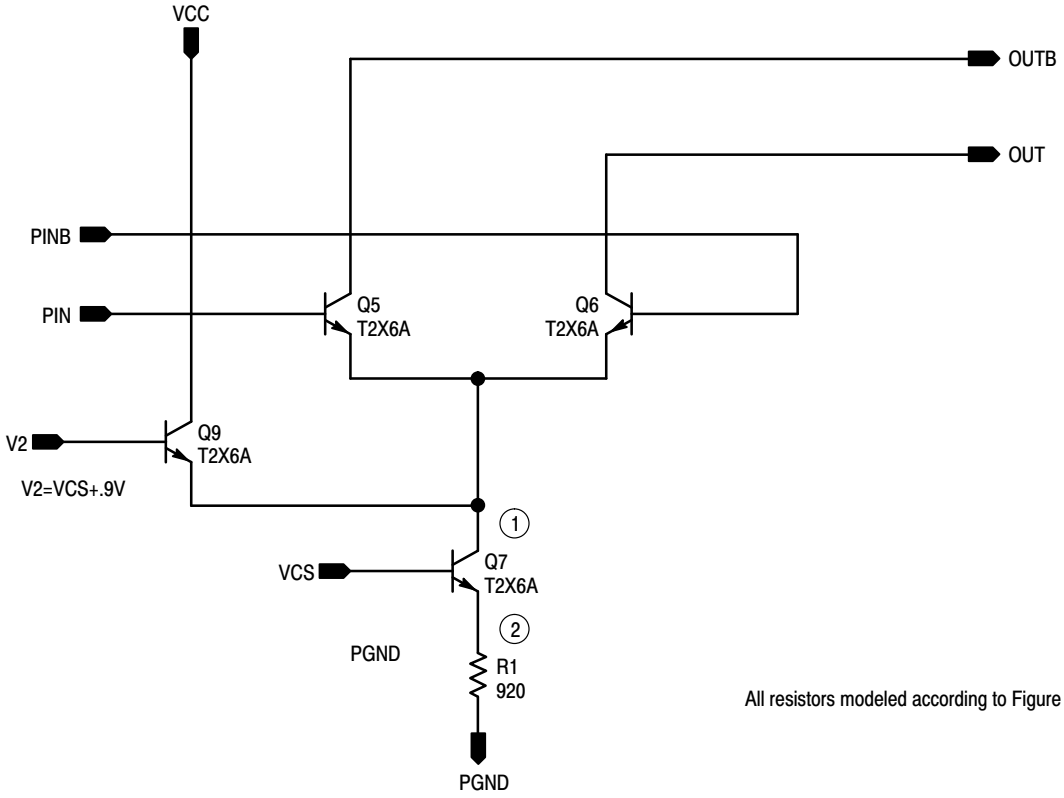
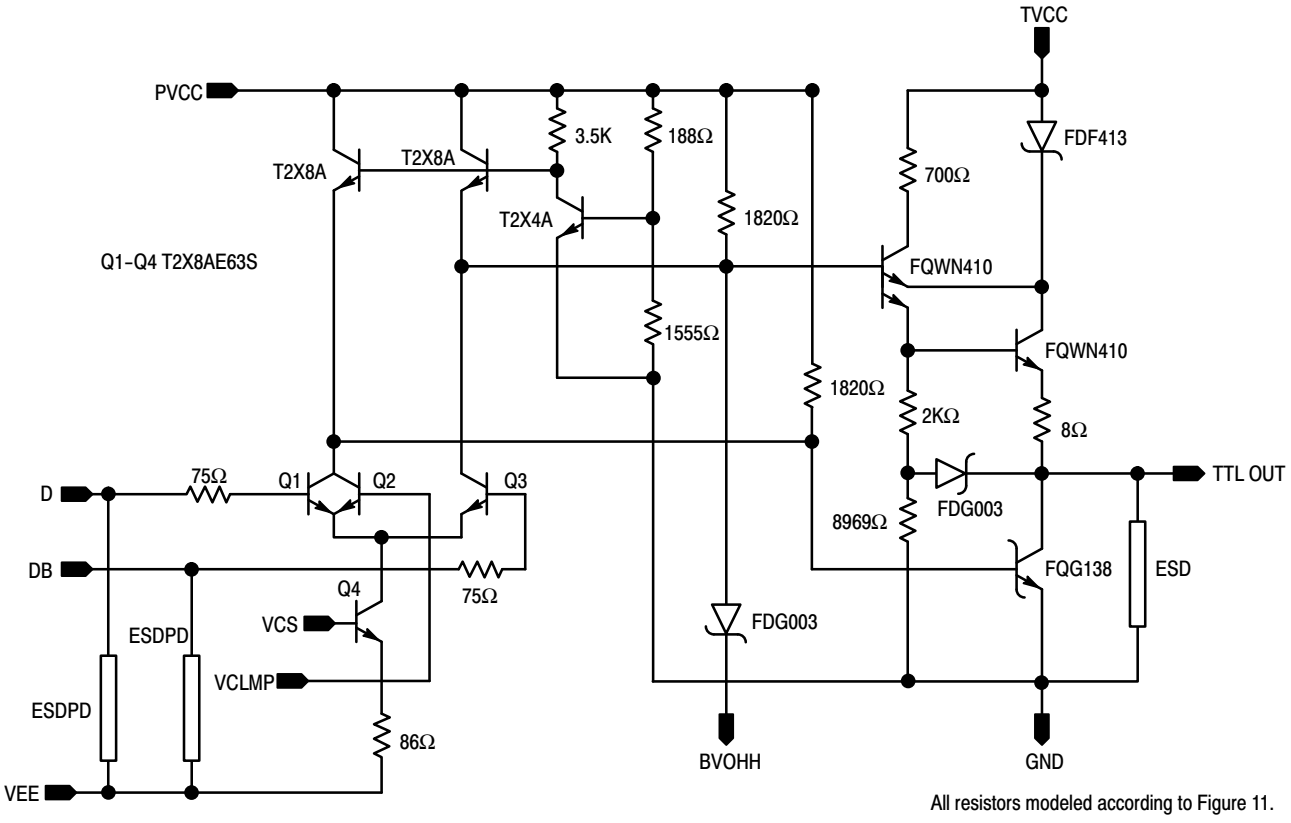
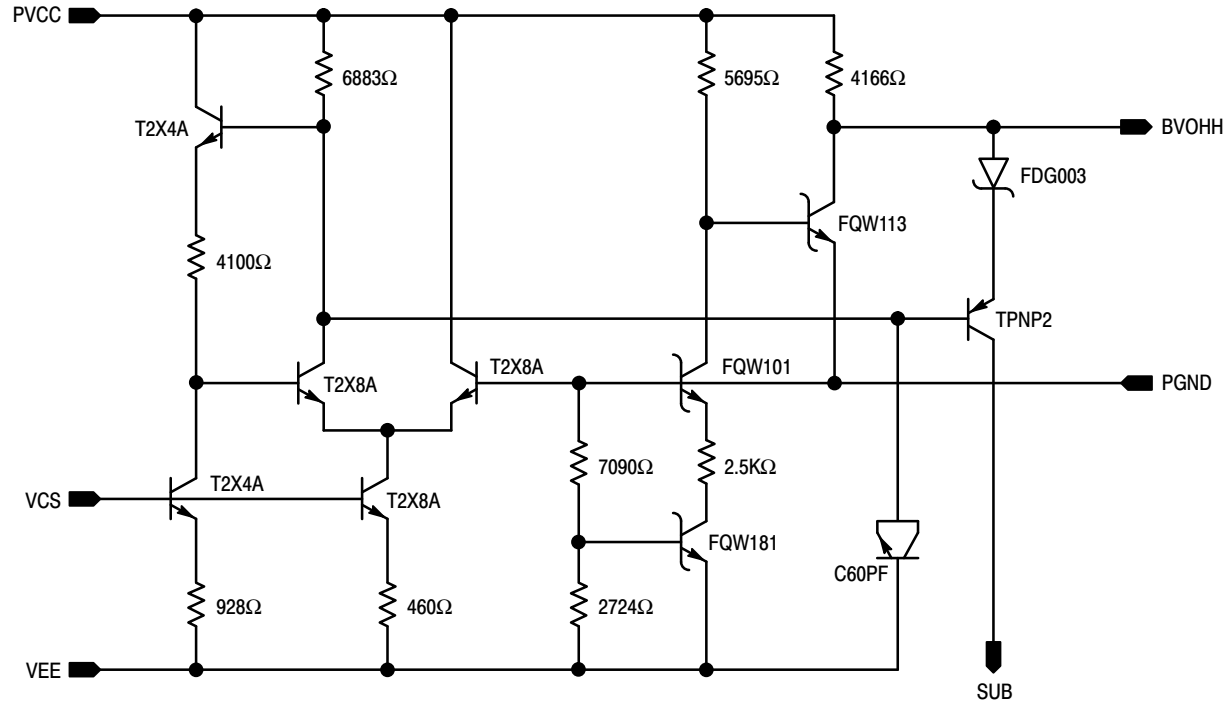



**Figure 1. . PECL_IN**



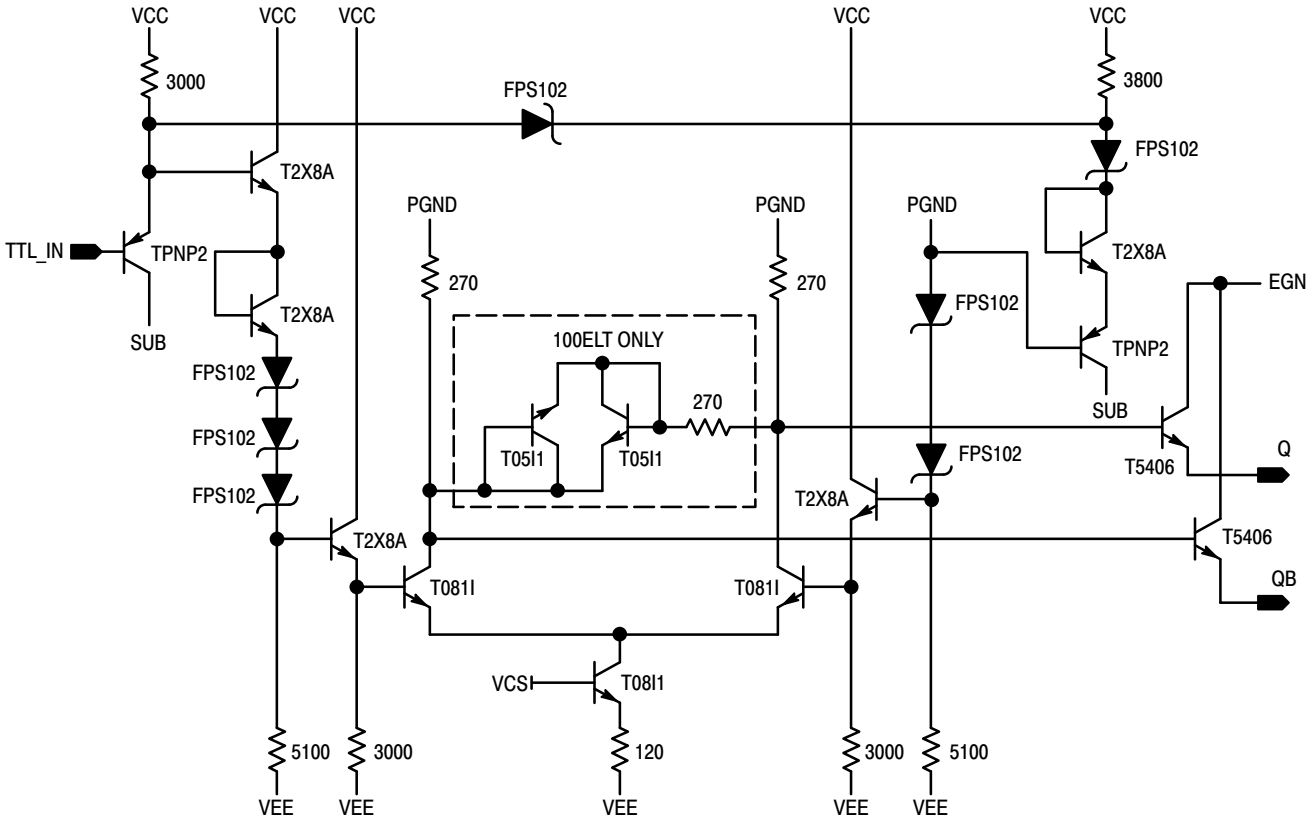

All resistors modeled according to Figure 11.

**Figure 2. . ECL to TTL MC10/100ELT25**



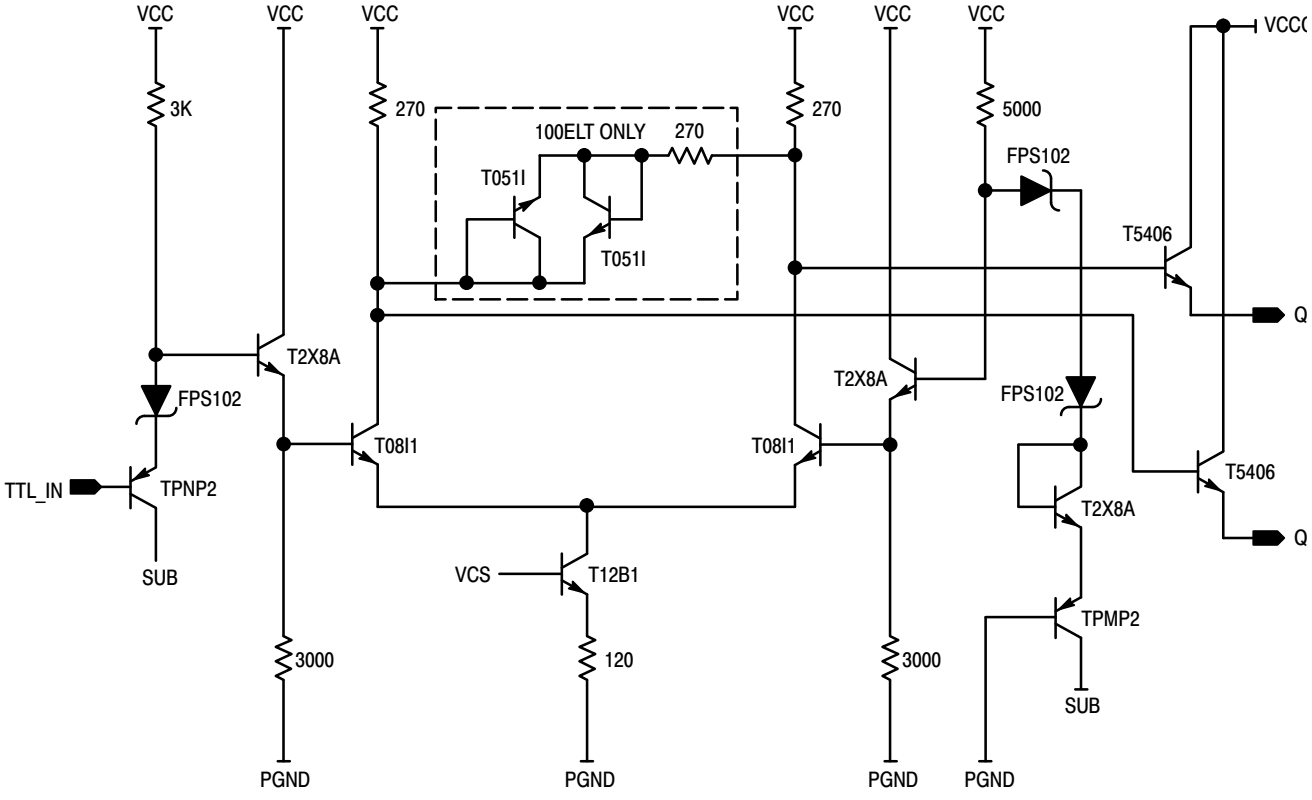

All resistors modeled according to Figure 11.

**2a. BVOHH Generator for the MC10/100ELT25**



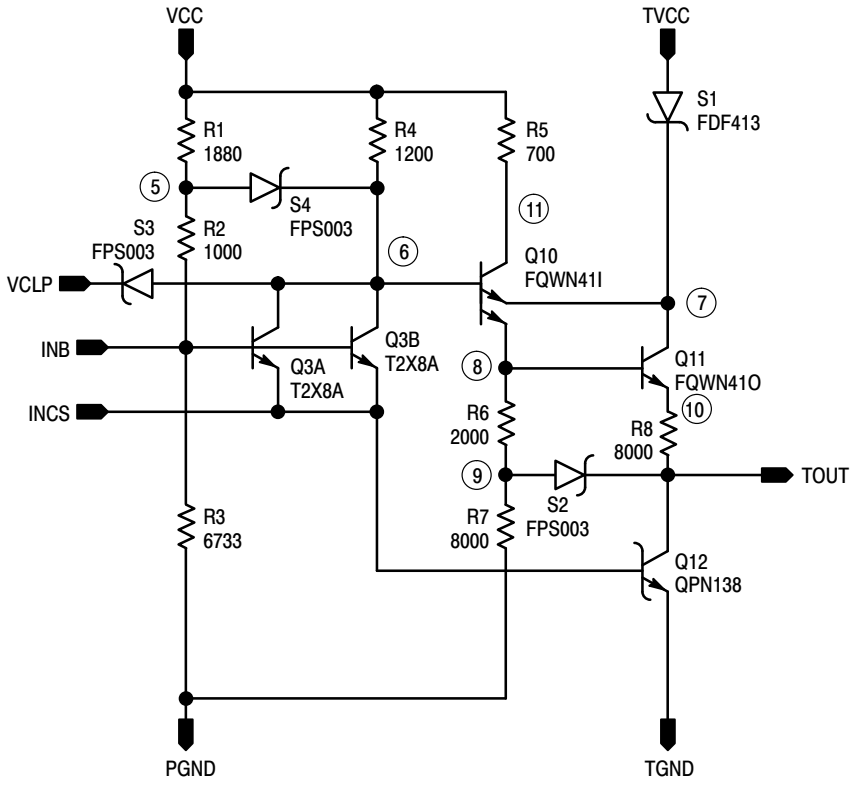

All resistors modeled according to Figure 11.

**Figure 3. . TTL_ECL**



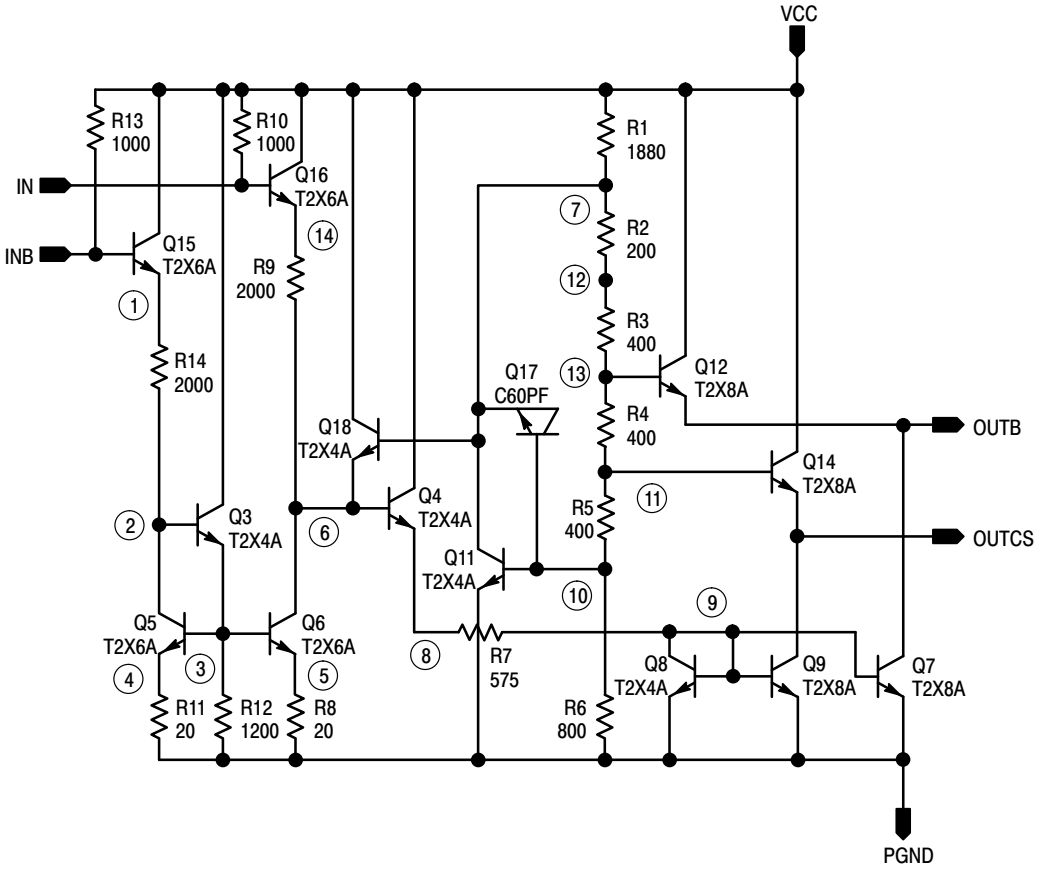

All resistors modeled according to Figure 11.

**Figure 4. . TTL_PECL**



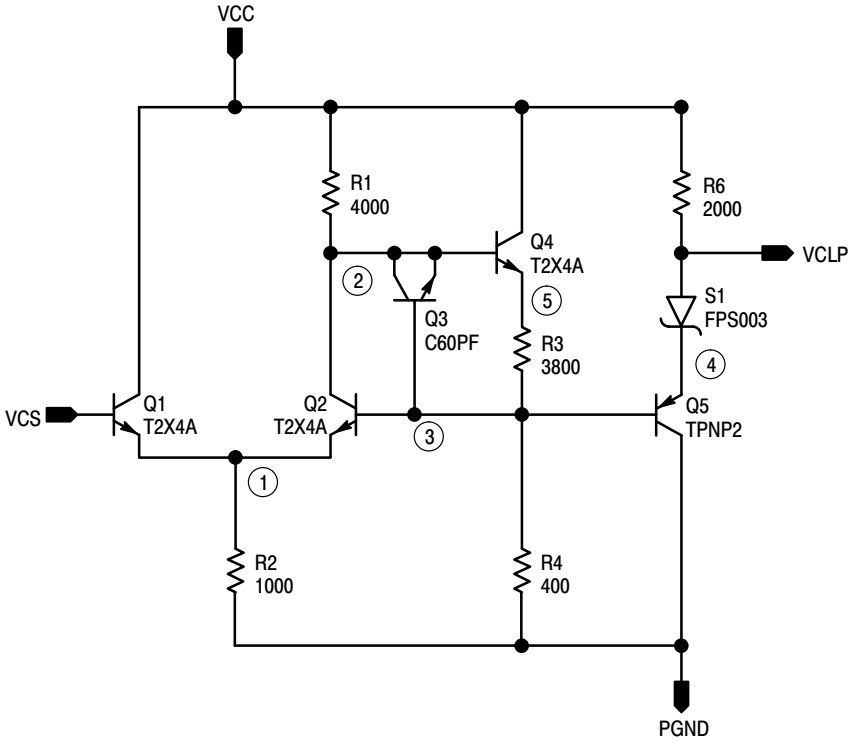

All resistors modeled according to Figure 11.

**Figure 5. . TTL_OUT**




All resistors modeled according to Figure 11.

**Figure 6. . MACRO ETL ETXR**




All resistors modeled according to Figure 11.

**Figure 7. . VCLP**

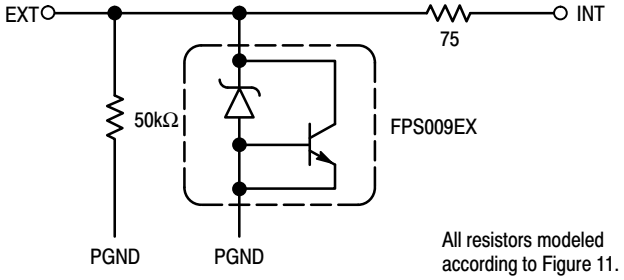



**Figure 8. . ESD Protection ECL/PECL Input**

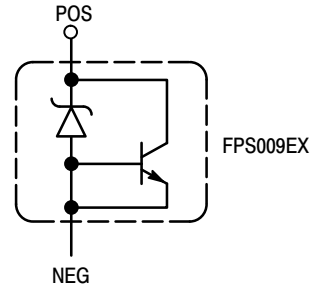



**Figure 9. . ESD Protection for all Outputs and TTL Inputs**

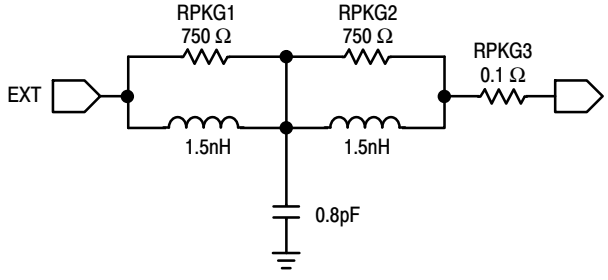



**Figure 10. . Package Pin Model**

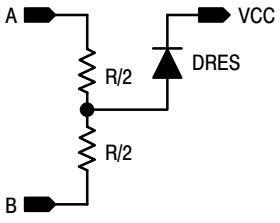



**Figure 11. . Resistor Model**

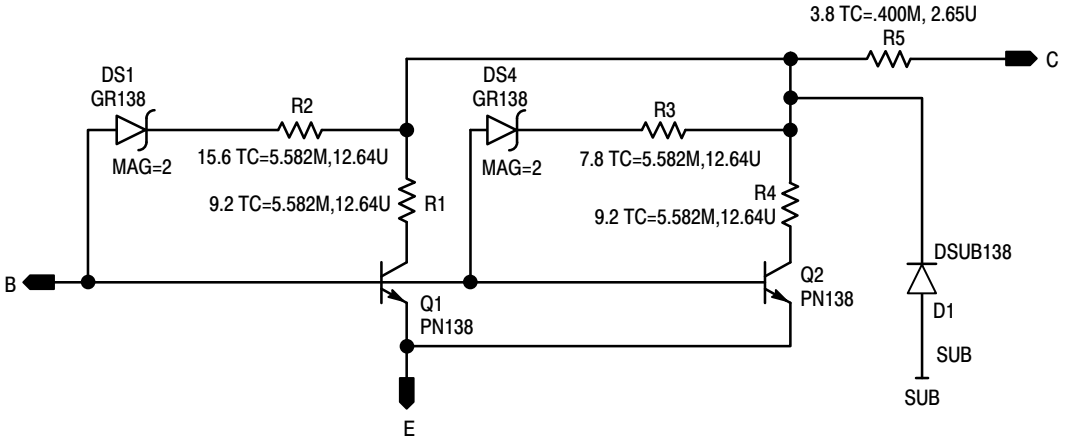



**Figure 12. . QPN138**

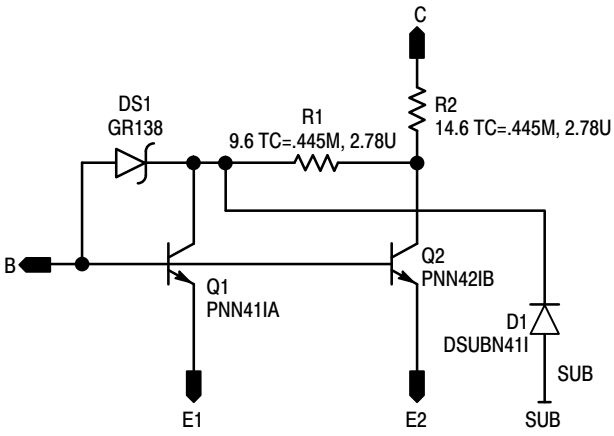



**Figure 13. . QWN410**

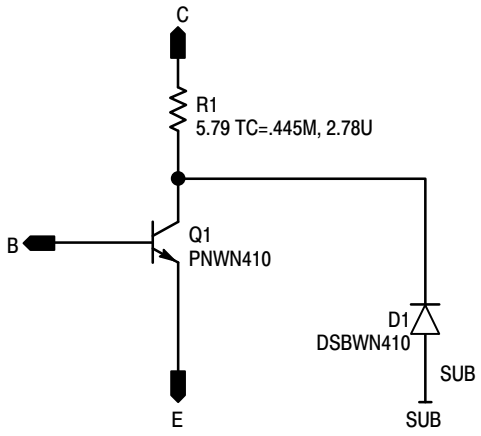



**Figure 14. . QPN410**

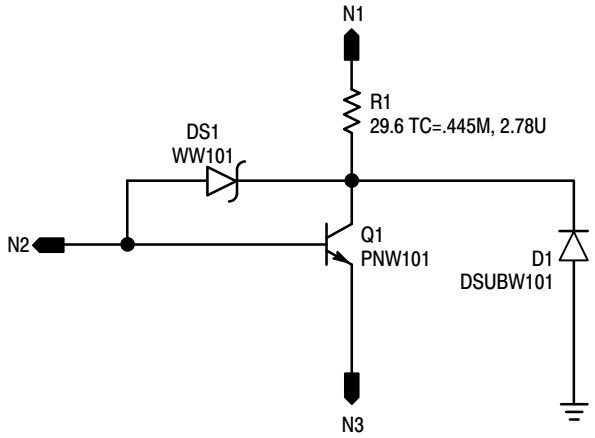



**Figure 15. . FDG003**

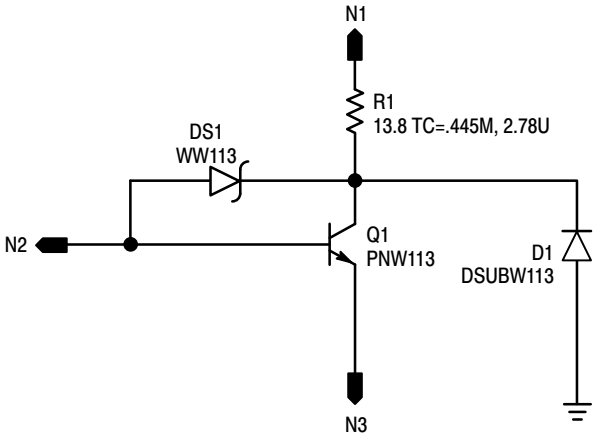



**Figure 16. . FQW113**

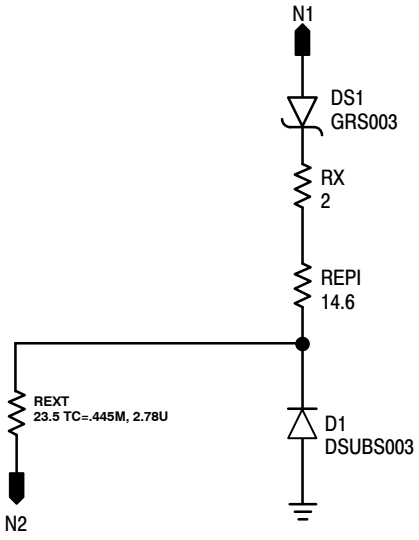



**Figure 17. . FDG003**

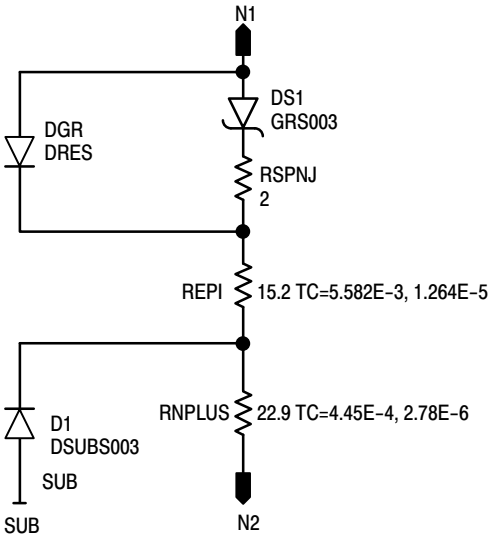



**Figure 18. . FPS003**

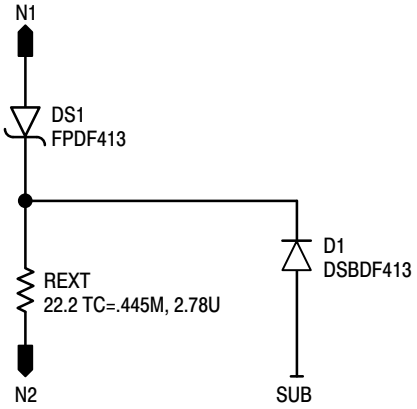



**Figure 19. . FDF413**

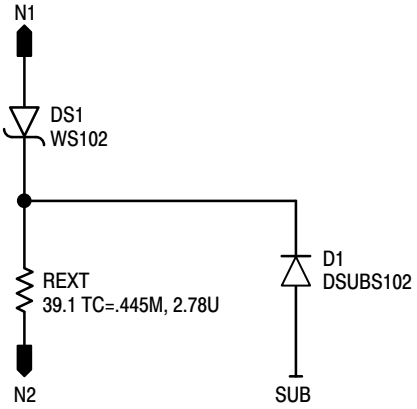



**Figure 20. . FPS102**

**Models**

```
*************************************************************************
* Spice Model Files for the:  MC10ELT20     MC100ELT20                  *
*                             MC10ELT21     MC100ELT21                  *
*                             MC10ELT22     MC100ELT22                  *
*                                           MC100ELT23                  *
*                             MC10ELT24     MC100ELT24                  *
*                             MC10ELT25     MC100ELT25                  *
*                             MC10ELT28     MC100ELT28                  *
*                                                                       *
*************************************************************************
******               ELT Translator SPICE Model                  ******
*************************************************************************
*                                                                       *
* NODES:                                                                *
*                                                                       *
* PGND = (INTERNAL GND)                                                 *
* TGND = (OUTPUT GND FOR TTL OUTPUTS)                                   *
* TVCC = (VCC FOR THE TTL OUTPUTS)                                      *
* VCS  = (CURRENT SOURCE DRIVE FOR THE ECL/PECL GATES=ECL VEE + 1.3V) *
* VBB  = (BIAS FOR SINGLE ENDED ECL/PECL = ECL VCC -1.3V)               *
* SUB  = (SUBSTRATE = MOST NEGATIVE RAIL FOR THE CKT.)                  *
* GND  = 0V                                                             *
* VEE  = -5V (databook spec)                                            *
* V2   = VCS + 0.9V                                                     *
* D..  = Input (ECL or TTL)                                             *
* Q..  = Output(ECL or TTL)                                             *
*                                                                       *
*  VCS and V2 are internal nodes.                                       *
*************************************************************************

******************************************************** ELT20 ****


.SUBCKT ELT20_10H  VCC GND D0 Q0 Q0B


VCS     VCS GND   1.3


   X1   VC GN VCS D Q QB                        TTL_PECL_10H
   X2   Q GN                                    ESD
   X3   QB GN                                   ESD
   X4   D GN                                    ESD
   X12  VCC VC                                  PKG8
   X13  GND GN                                  PKG8
   X15  D0 D                                    PKG8
   X16  Q0 Q                                    PKG8
   X17  Q0B QB                                  PKG8
 .ENDS ELT20_10H


.SUBCKT ELT20_100K  VCC GND D0 Q0 Q0B


VCS     VCS GND   1.3


   X1   VC GN VCS D Q QB                        TTL_PECL_100K
   X2   Q GN                                    ESD
   X3   QB GN                                   ESD
   X4   D GN                                    ESD
```

```
   X12  VCC VC                                  PKG8
   X13  GND GN                                  PKG8
   X15  D0 D                                    PKG8
   X16  Q0 Q                                    PKG8
   X17  Q0B QB                                  PKG8
.ENDS ELT20_100k

********************************************************* ELT21 ****

.SUBCKT ELT21_10H  VCC GND DECL DECLB QTTL

VCS     VCS GND   1.3
V2      V2  GND   2.2

   X1   VC GN VCS VCLP                    VOHCLMP
   X2   VC VC GN GN VCLP INB INCS QTT     TTL_OUT
   X3   VC GN Q QB INB INCS FEED          ETXR
   X4   VC GN VCS PIN PINB V2 Q QB        PECL_IN
   X5   VC GN DEC PIN                     ESDPD
   X6   VC GN DECB PINB                   ESDPD
   X7   QTT GN                            ESD
   X8   VCC VC                            PKG8
   X9   GND GN                            PKG8
   X10  DECL DEC                          PKG8
   X11  DECLB DECB                        PKG8
   X12  QTTL QTT                          PKG8
.ENDS ELT21_10H

.SUBCKT ELT21_100K  VCC GND DECL DECLB QTTL

VCS     VCS GND   1.3
V2      V2  GND   2.2

   X1   VC GN VCS VCLP                    VOHCLMP
   X2   VC VC GN GN VCLP INB INCS QTT     TTL_OUT
   X3   VC GN Q QB INB INCS FEED          ETXR
   X4   VC GN VCS PIN PINB V2 Q QB        PECL_IN
   X5   VC GN DEC PIN                     ESDPD
   X6   VC GN DECB PINB                   ESDPD
   X7   QTT GN                            ESD
   X8   VCC VC                            PKG8
   X9   GND GN                            PKG8
   X10  DECL DEC                          PKG8
   X11  DECLB DECB                        PKG8
   X12  QTTL QTT                          PKG8
.ENDS ELT21_100K

********************************************************* ELT22 ****

.SUBCKT ELT22_10H  VCC GND D0 D1 Q0 Q0B Q1 Q1B

VCS     VCS GND   1.3

   X1   VC GN VCS D0i Q0i Q0iB                TTL_PECL_10H
   X2   VC GN VCS D1i Q1i Q1iB                TTL_PECL_10H
```

```
   XE1  Q0i GN                                ESD
   XE2  Q0iB GN                               ESD
   XE3  Q0i GN                                ESD
   XE4  Q1i GN                                ESD
   XE5  Q1iB GN                               ESD
   XE6  D1i GN                                ESD
   X9   D1 D1i                                PKG8
   X10  Q1 Q1i                                PKG8
   X11  Q1B Q1iB                              PKG8
   X12  VCC VC                                PKG8
   X13  GND GN                                PKG8
   X15  D0 D0i                                PKG8
   X16  Q0 Q0i                                PKG8
   X17  Q0B Q0iB                              PKG8
 .ENDS ELT22_10H


.SUBCKT ELT22_100k  VCC GND D0 D1 Q0 Q0B Q1 Q1B

VCS     VCS GND   1.3

   X1   VC GN VCS D0i Q0i Q0iB                TTL_PECL_10H
   X2   VC GN VCS D1i Q1i Q1iB                TTL_PECL_10H
   XE1  Q0i GN                                ESD
   XE2  Q0iB GN                               ESD
   XE3  D0i GN                                ESD
   XE4  Q1i GN                                ESD
   XE5  Q1iB GN                               ESD
   XE6  D1i GN                                ESD
   X9   D1 D1i                                PKG8
   X10  Q1 Q1i                                PKG8
   X11  Q1B Q1iB                              PKG8
   X12  VCC VC                                PKG8
   X13  GND GN                                PKG8
   X15  D0 D0i                                PKG8
   X16  Q0 Q0i                                PKG8
   X17  Q0B Q0iB                              PKG8
 .ENDS ELT22_100k

******************************************************** ELT23 ****

.SUBCKT ELT23_100K  VCC GND DECL DECLB QTTL

VCS     VCS GND   1.3
V2      V2  GND   2.2

   X1   VC GN VCS VCLP                    VOHCLMP
   X2   VC VC GN GN VCLP INB INCS QTT     TTL_OUT
   X3   VC GN Q QB INB INCS FEED          ETXR
   X4   VC GN VCS PIN PINB V2 Q QB        PECL_IN
   X5   VC GN DEC PIN                     ESDPD
   X6   VC GN DECB PINB                   ESDPD
   X7   QTT GN                            ESD
   X8   VCC VC                            PKG8
   X9   GND GN                            PKG8
   X10  DECL DEC                          PKG8
   X11  DECLB DECB                        PKG8
   X12  QTTL QTT                          PKG8
```

```
.ENDS ELT23_100K

********************************************************* ELT24 ****

.SUBCKT ELT24_10H  VCC GND VEE D Q QB

VCS     VCS VEE   1.3

   X1   VC VE GN GN VCS DI QI QBI         TTL_ECL_10H
   X2   QI VE                             ESD
   X3   QBI VE                            ESD
   X4   DI VE                             ESD
   X5   VCC VC                            PKG8
   X6   GND GN                            PKG8
   X7   D DI                              PKG8
   X8   Q QI                              PKG8
   X9   QB QBI                            PKG8
   X10  VEE VE                            PKG8
.ENDS ELT24_10H

.SUBCKT ELT24_100K  VCC GND VEE D Q QB

VCS     VCS VEE   1.3

   X1   VC VE GN GN VCS DI QI QBI         TTL_ECL_100K
   X2   QI VE                             ESD
   X3   QBI VE                            ESD
   X4   DI VE                             ESD
   X5   VCC VC                            PKG8
   X6   GND GN                            PKG8
   X7   D DI                              PKG8
   X8   Q QI                              PKG8
   X9   QB QBI                            PKG8
   X10  VEE VE                            PKG8
.ENDS ELT24_100K

******************************************************** ELT 25 ****

.SUBCKT ELT25_10H  D DB Q VCC GND VEE

VCLMP   VCLMP VEE    2.1
VCS     VCS   VEE    1.3

   X1   IN INB QT VCCI VCCI VEEI GNDI
+       BVOHH VCLMP VCS                  ECL_TTL_ELT25
   X2   BVOHH VCCI VEEI VCS GNDI VEEI    BVOHH_GEN_ELT25

   XP1  D   IN                            PKG8
   XP2  DB  INB                           PKG8
   XP3  Q   QT                            PKG8
   XP4  VCC VCCI                          PKG8
   XP5  GND GNDI                          PKG8
   XP6  VEE VEEI                          PKG8
.ENDS ELT25_10H
```

```
.SUBCKT ELT25_100K  D DB Q VCC GND VEE

VCLMP   VCLMP VEE    2.1
VCS     VCS   VEE    1.3

   X1   IN INB QT VCCI VCCI VEEI GNDI
+       BVOHH VCLMP VCS                  ECL_TTL_ELT25
   X2   BVOHH VCCI VEEI VCS GNDI VEEI    BVOHH_GEN_ELT25

   XP1  D   IN                          PKG8
   XP2  DB  INB                         PKG8
   XP3  Q   QT                          PKG8
   XP4  VCC VCCI                        PKG8
   XP5  GND GNDI                        PKG8
   XP6  VEE VEEI                        PKG8
.ENDS ELT25_100k

********************************************************* ELT28 ******

.SUBCKT ELT28_10H  VCC GND DECL DECLB QTTL DTTL QECL QECLB

VCS     VCS GND   1.3
V2      V2  GND   2.2

   X1   VC GN VCS VCLP                  VOHCLMP
   X2   VC VC GN GN VCLP INB INCS QTT    TTL_OUT
   X3   VC GN Q QB INB INCS FEED         ETXR
   X4   VC GN VCS PIN PINB V2 Q QB       PECL_IN
   X5   VC GN VCS DTT QEC QECB           TTL_PECL_10H
   X6   VC GN DEC PIN                    ESDPD
   X7   VC GN DECB PINB                  ESDPD
   X8   QTT GN                          ESD
   X9   DTT GN                          ESD
   X10  QEC GN                          ESD
   X11  QECB GN                         ESD
   X12  VCC VC                          PKG8
   X13  GND GN                          PKG8
   X14  DECL DEC                        PKG8
   X15  DECLB DECB                      PKG8
   X16  QTTL QTT                        PKG8
   X17  DTTL DTT                        PKG8
   X18  QECL QEC                        PKG8
   X19  QECLB QECB                      PKG8
.ENDS ELT28_10H

.SUBCKT ELT28_100K  VCC GND DECL DECLB QTTL DTTL QECL QECLB

VCS     VCS GND   1.3
V2      V2  GND   2.2

   X1   VC GN VCS VCLP                  VOHCLMP
   X2   VC VC GN GN VCLP INB INCS QTT    TTL_OUT
   X3   VC GN Q QB INB INCS FEED         ETXR
   X4   VC GN VCS PIN PINB V2 Q QB       PECL_IN
   X5   VC GN VCS DTT QEC QECB           TTL_PECL_100K
   X6   VC GN DEC PIN                    ESDPD
```

```
   X7   VC GN DECB PINB                ESDPD
   X8   QTT GN                         ESD
   X9   DTT GN                         ESD
   X10  QEC GN                         ESD
   X11  QECB GN                        ESD
   X12  VCC VC                         PKG8
   X13  GND GN                         PKG8
   X14  DECL DEC                       PKG8
   X15  DECLB DECB                     PKG8
   X16  QTTL QTT                       PKG8
   X17  DTTL DTT                       PKG8
   X18  QECL QEC                       PKG8
   X19  QECLB QECB                     PKG8
.ENDS ELT28_100K
```

```
**************************************************************************
**************************************************************************
****                          I/O Models                              ****
**************************************************************************
**************************************************************************


**************************************************************************
**** The subcircuit ECL_TTL_ELT25 is a netlist of the differential ****
**** MC10/100ELT25 ECL to TTL translator (ECLinPS Lite)            ****
****    VCLMP = VCS+0.8V                                          ****
****    PVCC  = +5V                                               ****
****    TVCC  = +5V                                               ****
****    SUB   = VEE                                               ****
**************************************************************************


.SUBCKT  ECL_TTL_ELT25 IN INB TTLOUT PVCC TVCC VEE GND BVOHH VCLMP VCS

   XESDIN  PVCC VEE IN DIN   ESDPD
   XESDINB PVCC VEE INB DINB ESDPD
   XESDO   TTLOUT GND        ESD

   Q1      3 1 2 VEE         T2X8A
   Q2      3 VCLMP 2 VEE     T2X8A
   Q3      5 13 2 VEE        T2X8A
   Q4      2 VCS 4 VEE       T2X8A
   Q5      PVCC 6 3 VEE      T2X8A
   Q6      PVCC 6 5 VEE      T2X8A
   Q7      6 7 GND VEE       T2X4A

   XQ1     8 5 9 10 VEE      FQWN41I
   XQ2     9 10 12 VEE       FQWN41O
   XQ3     TTLOUT 3 GND VEE  QPN138

   XR1     PVCC 6 PVCC       RESK params: R=3500
   XR2     PVCC 7 PVCC       RES  params: R=188
   XR3     PVCC 5 PVCC       RES  params: R=1820
   XR4     TVCC 8 TVCC       RES  params: R=700
   XR5     10 11 TVCC        RES  params: R=2000
   XR6     12 TTLOUT TVCC    RES  params: R=8
   XR7     7 GND PVCC        RES  params: R=1555
   XR8     PVCC 3 PVCC       RES  params: R=1820
   XR9     DINB 13 PVCC      RES  params: R=75
   XR10    4 VEE PVCC        RES  params: R=86
   XR11    DIN 1 PVCC        RES  params: R=75
   XR12    11 GND TVCC       RESK params: R=8969

   XD1     5 BVOHH VEE       FDG003
   XD2     11 TTLOUT VEE     FDG003
   XD3     TVCC 9 VEE        FDF413

.ENDS    ECL_TTL_ELT25
```

```
*********************************************************************
**** The subcircuit BVOHH_GEN_ELT25 represents the BVOH           ****
**** generator of the MC10/100ELT25 device                        ****
****      PVCC = +5V                                               ****
****      PGND = 0V                                                ****
****      SUB  = VEE                                               ****
*********************************************************************


.SUBCKT BVOHH_GEN_ELT25  BVOHH PVCC VEE VCS PGND SUB


   Q1    PVCC 4 3 VEE        T2X4A
   Q2    2 VCS 1 VEE         T2X4A
   Q3    4 2 5 VEE           T2X8A
   Q4    PVCC PGND 5 VEE     T2X8A
   Q5    5 VCS 6 VEE         T2X8A
   Q6    SUB 4 7 VEE         TPNP2
   Q7    4 VEE 4 VEE         C60PF


   XQ1   10 PGND 11 VEE      FQW101
   XQ2   9 8 VEE VEE         FQW101
   XQ3   BVOHH 10 PGND VEE   FQW113


   XD1   BVOHH 7 VEE         FDG003


   XR1   3 2 PVCC            RESK params: R=4100
   XR2   PVCC 4 PVCC         RESK params: R=6883
   XR3   6 VEE PVCC          RES  params: R=460
   XR4   PGND 8 PVCC         RESK params: R=7090
   XR5   8 VEE PVCC          RESK params: R=2724
   XR6   11 9 PVCC           RESK params: R=2500
   XR7   1 VEE PVCC          RES  params: R=928
   XR8   PVCC 10 PVCC        RESK params: R=5695
   XR9   PVCC BVOHH PVCC     RESK params: R=4166


.ENDS    BVOHH_GEN_ELT25


*********************************************************************
***** SUBCKT TTL_OUT is the TTL ouput for the                  *****
***** MC10/100ELT21, MC100ELT23, MC10/100ELT28.                *****
*********************************************************************


.SUBCKT TTL_OUT  TVCC VCC TGND PGND VCLP INB INCS OUT
   Q3a   6 INB INCS PGND     t2x8a
   Q3b   6 INB INCS PGND     t2x8a
   XQ10  11 6 7 8 PGND       FQWN41I
   XQ11  7 8 10 PGND         FQWN41O
   XQ12  OUT INCS TGND PGND  QPN138
   XD1   TVCC 7 PGND         FDF413
   XD2   9 OUT PGND          FPS003
   XD3   6 VCLP PGND         FPS003
   XD4   5 6 PGND            FPS003
   XR1   5 INB VCC           RES  params: R=1000
   XR2   VCC 5 VCC           RES  params: R=1880
   XR3   INB PGND VCC        RESK params: R=6733
   XR5   VCC 6 VCC           RES  params: R=1200
   XR6   TVCC 11 TVCC        RES  params: R=700
   XR7   8 9 VCC             RES  params: R=2000
```

```
   XR8   9 PGND VCC          RESK params: R=8000
   XR9   10 OUT VCC          RES  params: R=8
.ENDS    TTL_OUT

*********************************************************************
***** SUBCKT ETXR is necessary to drive the TTL_OUT SUBCKT        *****
***** used in MC10/100ELT21, MC100ELT23, MC10/100ELT28.           *****
*********************************************************************

.SUBCKT ETXR  VCC PGND IN INB OUTB OUTCS TWO5PHI
   Q3    VCC 2 3 PGND       t2x4a
   Q4    VCC 6 8 PGND       t2x4a
   Q5    2 3 4 PGND         t2x6a
   Q6    6 3 5 PGND         t2x6a
   Q7    OUTB 9 PGND PGND   t2x8a
   Q8    9 9 PGND PGND      t2x4a
   Q9    OUTCS 9 PGND PGND  t2x8a
   Q11   7 10 PGND PGND     t2x4a
   Q12   VCC 13 OUTB PGND   t2x8a
   Q14   VCC 11 OUTCS PGND  t2x8a
   Q15   VCC INB 1 PGND     t2x6a
   Q16   VCC IN 14 PGND     t2x6a
   Q17   7 10 7 PGND        c60pf
   Q18   VCC 7 6 PGND       t2x4a
   XR1   VCC INB VCC        RES params:  R=1000
   XR2   VCC IN VCC         RES params:  R=1000
   XR3   3 PGND VCC         RES params:  R=1200
   XR5   VCC 7 VCC          RES params:  R=1800
   XR6A  7 TWO5PHI VCC      RES params:  R=200
   XR6   TWO5PHI 13 VCC     RES params:  R=400
   XR7   13 11 VCC          RES params:  R=400
   XR8   11 10 VCC          RES params:  R=400
   XR9   10 PGND VCC        RES params:  R=800
   XR11  4 PGND VCC         RES params:  R=20
   XR12  5 PGND VCC         RES params:  R=20
   XR14  8 9 VCC            RES params:  R=575
   XR15  1 2 VCC            RES params:  R=2000
   XR17  14 6 VCC           RES params:  R=2000
.ENDS ETXR

*********************************************************************
**** SUBCKT VOHCLMP IS NECESSARY TO GENERAT A PROPER CLAMP VOLTAGE ****
**** FOR TTL_OUT in MC10/100ELT28, MC100ELT23, MC10/100ELT21.      ****
*********************************************************************

.SUBCKT VOHCLMP  VCC PGND VCS VCLP
   Q1    VCC VCS 1 PGND   t2x4a
   Q2    2 3 1 PGND       t2x4a
   Q3    2 3 2 PGND       c60pf
   Q4    VCC 2 5 PGND     t2x4a
   Q5    PGND 5 4 PGND    tpnp2
   XD1   VCLP 4 PGND      FPS003
   XR1   VCC 2 VCC        RESK params: R=4000
   XR2   1 PGND VCC       RES  params: R=1000
   XR3   5 3 VCC          RESK params: R=3800
   XR4   3 PGND VCC       RES  params: R=2600
   XR6   VCC VCLP VCC     RES  params: R=2000
.ENDS VOHCLMP
```

```
*********************************************************************
*** The SUBCKT TTL_PECL_100K represents 100K TTL to PECL          ***
*** translator used in MC100ELT20, MC100ELT22.                    ***
*********************************************************************


.SUBCKT TTL_PECL_100K  VCC PGND VCS TIN POUT PBOUT
   Q1      PGND TIN 1 PGND     tpnp2
   Q2      VCC 2 3 PGND        t2x8a
   Q3      VCC 10 9 PGND       t2x8a
   Q4      12 12 13 PGND       t2x8a
   Q5      PGND PGND 13 PGND   tpnp2
   Q6      4 3 5 PGND          t08i1
   Q7      7 9 5 PGND          t08i1
   Q8      5 VCS 6 PGND        t12b1
   Q9      VCC 4 PBOUT PGND    t5406
   Q10     VCC 7 POUT PGND     t5406
   Q11     4 4 8 PGND          t05i1
   Q12     8 8 4 PGND          t05i1
   XDSTE5  19 VCC PGND         FPS102
   XDSTE6  VCC 19 PGND         FPS102
   XD1     2 1 PGND            FPS102
   XD2     10 11 PGND          FPS102
   XD3     11 12 PGND          FPS102
   XR1     VCC 2 VCC           RESK params: R=3000
   XR2     3 PGND VCC          RESK params: R=3000
   XR3     9 PGND VCC          RESK params: R=3000
   XR4     VCC 10 VCC          RESK params: R=3000
   XR5     VCC 4 VCC           RES  params: R=270
   XR6     VCC 7 VCC           RES  params: R=270
   XR7     6 PGND VCC          RES  params: R=120
   XR8     7 8 VCC             RES  params: R=270
.ENDS  TTL_PECL_100K

*********************************************************************
*** The SUBCKT TTL_PECL_10H represents 10H TTL to PECL            ***
*** translator used in MC10ELT20,MC10ELT22.                       ***
*********************************************************************


.SUBCKT TTL_PECL_10H  VCC PGND VCS TIN POUT PBOUT
   Q1      PGND TIN 1 PGND     tpnp2
   Q2      VCC 2 3 PGND        t2x8a
   Q3      VCC 10 9 PGND       t2x8a
   Q4      12 12 13 PGND       t2x8a
   Q5      PGND PGND 13 PGND   tpnp2
   Q6      4 3 5 PGND          t08i1
   Q7      7 9 5 PGND          t08i1
   Q8      5 VCS 6 PGND        t12b1
   Q9      VCC 4 PBOUT PGND    t5406
   Q10     VCC 7 POUT PGND     t5406
   XDSTE5  19 VCC PGND         FPS102
   XDSTE6  VCC 19 PGND         FPS102
   XD1     2 1 PGND            FPS102
   XD2     10 11 PGND          FPS102
   XD3     11 12 PGND          FPS102
   XR1     VCC 2 VCC           RESK params: R=3000
   XR2     3 PGND VCC          RESK params: R=3000
   XR3     9 PGND VCC          RESK params: R=3000
   XR4     VCC 10 VCC          RESK params: R=3000
   XR5     VCC 4 VCC           RES  params: R=270
   XR6     VCC 7 VCC           RES  params: R=270
```

```
   XR7     6 PGND VCC          RES  params: R=120
.ENDS  TTL_PECL_10H

*********************************************************************
*** The SUBCKT TTL_ECL_100K is used in the 100K TTL to ECL          ***
*** translator MC100ELT24.                                          ***
*********************************************************************

.SUBCKT TTL_ECL_100K  VCC VEE EGND PGND VCS TTL_IN Q QB
   XRTE1   VCC 1 VCC           RESK params: R=3000
   XRTE2   VCC 2 VCC           RESK params: R=3000
   XRTE3   7 VEE PGND          RESK params: R=5100
   XRTE4   12 VEE PGND         RESK params: R=5100
   XRTE5   8 VEE PGND          RESK params: R=3000
   XRTE6   13 VEE PGND         RESK params: R=3000
   XREO1   PGND 16 PGND        RES  params: R=270
   XREO2   PGND 14 PGND        RES  params: R=270
   XREO3   19 VEE PGND         RES  params: R=120
   XREO4   14 18 PGND          RES  params: R=270
   XDSTE1  4 5 VEE             FPS102
   XDSTE2  5 6 VEE             FPS102
   XDSTE3  1 2 VEE             FPS102
   XDSTE4  2 9 VEE             FPS102
   XDSTE5  11 12 VEE           FPS102
   XDSTE6  PGND 11 VEE         FPS102
   XDSTE7  6 7 VEE             FPS102
   QTE1    VEE TTL_IN 1 VEE    tpnp2
   QTE2    VCC 1 3 VEE         t2x8a
   QTE3    3 3 4 VEE           t2x8a
   QTE4    9 9 10 VEE          t2x8a
   QTE5    VEE PGND 10 VEE     tpnp2
   QTE6    VCC 7 8 VEE         t2x8a
   QTE7    VCC 12 13 VEE       t2x8a
   QEO2    16 8 15 VEE         t08i1
   QEO3    14 13 15 VEE        t08i1
   QEO4    15 VCS 19 VEE       t12b1
   QEO5    EGND 14 Q VEE       t5406
   QEO6    EGND 16 QB VEE      t5406
   QEO7    18 18 16 VEE        t05i1
   QEO8    16 16 18 VEE        t05i1
.ENDS      TTL_ECL_100K

*********************************************************************
*** The SUBCKT TTL_ECL_10H is used in the 10H TTL to ECL            ***
*** translator MC10ELT24.                                           ***
*********************************************************************

.SUBCKT TTL_ECL_10H  VCC VEE EGND PGND VCS TTL_IN Q QB

   XRTE1   VCC 1 VCC           RESK params: R=3000
   XRTE2   VCC 2 VCC           RESK params: R=3000
   XRTE3   7 VEE PGND          RESK params: R=5100
   XRTE4   12 VEE PGND         RESK params: R=5100
   XRTE5   8 VEE PGND          RESK params: R=3000
   XRTE6   13 VEE PGND         RESK params: R=3000
   XREO1   PGND 16 PGND        RES  params: R=270
   XREO2   PGND 14 PGND        RES  params: R=270
   XREO3A  19 VEE PGND         RES  params: R=120
   XDSTE1  4 5 VEE             FPS102
```

```
   XDSTE2  5 6 VEE             FPS102
   XDSTE3  1 2 VEE             FPS102
   XDSTE4  2 9 VEE             FPS102
   XDSTE5  11 12 VEE           FPS102
   XDSTE6  PGND 11 VEE         FPS102
   XDSTE7  6 7 VEE             FPS102
   QTE1    VEE TTL_IN 1 VEE    tpnp2
   QTE2    VCC 1 3 VEE         t2x8a
   QTE3    3 3 4 VEE           t2x8a
   QTE4    9 9 10 VEE          t2x8a
   QTE5    VEE PGND 10 VEE     tpnp2
   QTE6    VCC 7 8 VEE         t2x8a
   QTE7    VCC 12 13 VEE       t2x8a
   QEO2    16 8 15 VEE         t08i1
   QEO3    14 13 15 VEE        t08i1
   QEO4    15 VCS 19 VEE       t12b1
   QEO5    EGND 14 Q VEE       t5406
   QEO6    EGND 16 QB VEE      t5406
.ENDS  TTL_ECL_10H

*********************************************************************
*** The SUBCKT PECL_IN represents the PECL input in PECL-TTL        ***
*** translators in MC10/100ELT21, MC10/100ELT23, MC10/100ELT28.     ***
*********************************************************************

.SUBCKT PECL_IN  VCC PGND VCS PIN PINB V2 OUT OUTB
   Q5   OUTB PIN 1 PGND t2x6a
   Q6   OUT PINB 1 PGND t2x6a
   Q7   1 VCS 2 PGND    t2x6a
   Q9   VCC V2 1 PGND   t2x6a
   XR1  2 pgnd VCC      RES params: R=820
.ENDS PECL_IN

*********************************************************************
*** The SUBCKT PKG8 is the model for the 8-ld SOIC-package. It can  ***
*** be used for all pins.                                           ***
*********************************************************************

.SUBCKT PKG8  EXT INT
   CPKG   82 0    0.8p
   RPKG1  EXT 82  750
   RPKG2  82 83   750
   RPKG3  83 INT  0.1
   LPKG1  EXT 82  1.5n
   LPKG2  82 83   1.5n
.ENDS  PKG8

*********************************************************************
*** The SUBCKT ESD represents the ESD-protection circuitry for the  ***
*** TTL-I/O-Pins and (P)ECL Outputs.                                ***
*********************************************************************

.SUBCKT ESD  POS NEG
   X  POS NEG NEG  FPS009EX
.ENDS ESD

*********************************************************************
```

```
*** The SUBCKT ESDPD represents the ESD-protection circuitry for    ***
*** the (P)ECL-Inputs.                                              ***
**********************************************************************


.SUBCKT ESDPD  VCCE PGND IN OUT
   XFP  IN PGND PGND  FPS009EX
   XRB  IN OUT VCCE   RES params: R=75
   XRP  IN PGND VCCE  RPD params: R=50K
.ENDS   ESDPD
```

```
**********************************************************************
**********************************************************************
****** Most Subcircuits that represents transistor circuitry,     *****
****** built with several primitives                              *****
**********************************************************************
**********************************************************************


.SUBCKT FPS009EX  N1 N2 SUB
   R1   N1 1         4.97 TC=0.445m,2.78u
   Q1   1 N2 N2 SUB  pn009e
   D1   SUB 1        dsub009e
   DS1  N2 1         gr009e
.ENDS   FPS009EX

**********************************************************************

.SUBCKT QPN138  C B E SUB
   Q1   3 B E SUB  pn138
   Q2   5 B E SUB  pn138
   DS1  B 1     gr138
   DS4  B 4     gr138
   D1   SUB 2   dsub138
   R1   2 3     9.2  TC=5.582m,12.64u
   R2   1 2     15.6 TC=5.582m,12.64u
   R3   4 2     7.8  TC=5.582m,12.64u
   R4   2 5     9.2  TC=5.582m,12.64u
   R5   2 C     3.8  TC=5.582m,12.64u
.ENDS   QPN138

**********************************************************************

.SUBCKT FQWN41I  C B E1 E2 SUB
   Q1   1 B E1 SUB  pnn41ia
   Q2   2 B E2 SUB  pnn42ib
   DS1  b 1         gr138
   D1   SUB 1       dsubn41i
   R1   1 2         9.6  TC=0.445m,2.78u
   R2   C 2         14.6 TC=0.445m,2.78u
.ENDS   FQWN41I

**********************************************************************

.SUBCKT FQWN41O  C B E SUB
   Q1   1 B E SUB   pnwn41o
   D1   SUB 1       dsbwn41o
   R1   C 1         5.79 TC=0.445m,2.78u
.ENDS   FQWN41O

**********************************************************************

.SUBCKT FQW101  C B E SUB
   QPNW101 1 B E   PNW101
   DS1     B 1     WW101
   D1      SUB 1   DSUBW101
   R1      C 1     29.6     TC=0.445M,2.78U
.ENDS   FQW101
```

```
**********************************************************************

.SUBCKT FQW113  C B E SUB
   Q1   1 B E    PNW113
   DS1  B 1      WW113
   D1   SUB 1    DSUBW113
   R1   C 1      13.8       TC=0.445M,2.78U
.ENDS   FQW113

**********************************************************************

.SUBCKT FDG003  N1 N2 SUB
   D1   SUB 3    DSUBS003
   DS1  N1  1    GRS003
   REXT N2  3    23.5       TC=0.445M,2.78U
   RX   1   2    2.0
   REPI 2   3    14.6
.ENDS   FDG003

**********************************************************************

.SUBCKT FPS003  N1 N2 SUB
   DS1  N1 1    grs003
   DGR  N1 2    dres
   D1   SUB 3   dsubs003
   R1   1 2     2
   R2   2 3     15.2 TC=5.582m,12.64u
   R3   3 N2    22.9 TC=0.445m, 2.78u
.ENDS   FPS003

**********************************************************************

.SUBCKT FDF413  N1 N2 SUB
   DS1  N1 1    fpdf413
   D1   SUB 1   dsbdf413
   R1   1 N2    22.2 TC=0.445m,2.78u
.ENDS   FDF413

**********************************************************************

.SUBCKT FPS102  N1 N2 SUB
   DS1  N1 1    ws102
   D1   SUB 1   dsubs102
   R1   1 N2    39.1 TC=0.455m,2.78u
.ENDS   FPS102

**********************************************************************

.SUBCKT RES  A B VCC   params: R=50
    *   Assumes Sheet Rho=100OHM, Resistor Width=10U, and Cap in Farads.
    *   Use for Resistors up to 2500OHM
    Ra  A 1    {R/2} TC=900U
    Rb  1 B    {R/2} TC=900U
    D1  1 VCC  DRES
    .MODEL DRES D
```

```
      + (IS=3.7E-16
      +  CJO=4.72E-16*R+58E-16)
.ENDS RES

*********************************************************************

.SUBCKT RESK  A B VCC  params: R=3000
    *   Assumes Sheet Rho=500OHM, Resistor Width=10U, and Cap in Farads.
    *   Use for Resistors > 2500OHM
    Ra  A 1    {R/2} TC=900U
    Rb  1 B    {R/2} TC=900U
    D1  1 VCC  DRES
    .MODEL DRES D
      + (IS=3.7E-16
      +  CJO=0.265E-16*R+29E-16)
.ENDS RESK

*********************************************************************

.SUBCKT RPD  A B VCC   params: R=50K
    Ra  A 1   {R/2} TC=900U
    Rb  1 B   {R/2} TC=900U
    D1  1 VCC  DRPD
    .MODEL DRPD D
      + (IS=3.7E-16
      +  CJO=0.1149P)
.ENDS RPD

*********************************************************************
**********************    MODEL-PARAMETER    **********************
*********************************************************************

*********************************************************************
.MODEL t2x4a          NPN
     + (is=0.01288f  bf=100       br=1.5        re=2          ikf=14.3m
     +  vaf=46       ise=0.2394f  rb=400        rbm=200       irb=850u
     +  ikr=0.364    var=3.58     isc=0.06404f  rc=35.4       nc=1.045
     +  nr=0.9972    cje=44.5f    vje=1.037     mje=0.572     nf=1.000
     +  xti=4.7      cjc=61f      vjc=0.75      mjc=0.266     ne=2.000
     +  xtb=1.15     cjs=109.4f   vjs=0.5815    mjs=0.5273    tr=9.92n
     +  ptf=30       tf=35p       xtf=2.6       vtf=1.67      itf=8.08m
     +  xcjc=59m     fc=0.8       eg=1.11)
*********************************************************************
.MODEL t2x6a          NPN
     + (is=0.01973f  bf=100       br=1.5        re=1.66       ikf=0.0195
     +  vaf=46       ise=0.358f   rb=678        rbm=50        irb=12u
     +  ikr=0.3655   var=3.58     isc=0.04519f  rc=27.24      nc=1.045
     +  nr=1.027     cje=60.17f   vje=0.92      mje=0.413     nf=1.000
     +  xti=4.7      cjc=70.8f    vjc=0.75      mjc=0.2665    ne=2.000
     +  xtb=1.15     cjs=120.2f   vjs=581.5m    mjs=0.5273    tr=9.92n
     +  ptf=50       tf=35p       xtf=2.6       vtf=1.578     itf=11.66m
     +  xcjc=74.1m   fc=0.8       eg=1.11)
```

```
*********************************************************************
.MODEL t2x8a          NPN
     + (is=0.02532f  bf=100       br=1.5        re=1.50      ikf=27.3m
     +  vaf=46       ise=0.478f   rb=222        rbm=111      irb=1.7m
     +  ikr=365.5m   var=3.58     isc=0.080f    rc=22.67     nc=1.045
     +  nr=0.9972    cje=79.6f    vje=1.037     mje=0.572    nf=1
     +  xti=4.7      cjc=88.7f    vjc=0.75      mjc=0.266    ne=2
     +  xtb=1.15     cjs=130.9f   vjs=581.5m    mjs=527.3m   tr=9.92n
     +  ptf=50       tf=35E-12    xtf=2.6       vtf=1.578    itf=16m
     +  xcjc=0.085   fc=0.8       eg=1.11)
*********************************************************************
.MODEL pn138          NPN
     + (is=0.163f    bf=100        br=1.5        re=0         ikf=0.179
     +  vaf=46       ise=0         rb=75.9       rbm=31.1
     +  ikr=6.975m   var=3.58      isc=0.193f    rc=5.29      nc=1.045
     +  nr=1         cje=773f      vje=0.9       mje=0.4      nf=1.008
     +  xti=5        cjc=378f      vjc=0.53      mjc=0.37     ne=1
     +  xtb=1.15     eg=1.11       tr=9.92n
     +  ptf=0        tf=35p        xtf=2.6       vtf=100      itf=10
     +  xcjc=0.1     fc=0.5)
*********************************************************************
.MODEL gr138          D
     + (is=0.138p    rs=5.6        n=1.044       tt=10p       cjo=174.2f
     +  vj=0.4       m=0.33        eg=0.69       xti=2        bv=30)
*********************************************************************
.MODEL dsub138        D
     + (cjo=1.87P    eg=1.15       vj=0.51     m=0.24)
*********************************************************************
.MODEL dsub009e       D
     + (cjo=106f     eg=1.15       vj=0.51     m=0.24)
*********************************************************************
.MODEL pn009e         NPN
     + (is=0.392f    bf=100        br=1.5        re=0         ikf=431m
     +  vaf=46       ise=0         rb=185        rbm=39
     +  ikr=0.3m     var=3.58      isc=4.25f     rc=3.9       nc=1.045
     +  nr=1         cje=1.37p     vje=0.9       mje=0.4      nf=1.008
     +  xti=5        cjc=609f      vjc=0.53      mjc=0.37     ne=1
     +  xtb=1.15     eg=1.11       tr=9.92n
     +  ptf=0        tf=35p        xtf=2.6       vtf=100      itf=1.64m
     +  xcjc=0.1     fc=0.5)
*********************************************************************
.MODEL gr009e         D
     + (is=0.54p     rs=9.57       n=1.044       tt=10p       cjo=683f
     +  vj=0.4       m=0.33        eg=0.69       xti=2        bv=30)
*********************************************************************
.MODEL dsubn41i       D
     + (cjo=303.3f   eg=1.15       vj=0.51     m=0.24)
*********************************************************************
.MODEL pnn41ia        NPN
     + (is=0.02625f  bf=100        br=1.5        re=0         ikf=0.029
     +  vaf=46       ise=0         rb=467        rbm=189.2
     +  ikr=1.125m   var=3.58      isc=0.0311f   rc=58        nc=1.045
     +  nr=1         cje=131.6f    vje=0.9       mje=0.4      nf=1.008
     +  xti=5        cjc=60.4f     vjc=0.53      mjc=0.37     ne=1
     +  xtb=1.15     eg=1.11       tr=9.92n
     +  ptf=0        tf=35p        xtf=2.6       vtf=100      itf=10
     +  xcjc=0.1     fc=0.5)
```

```
*********************************************************************
.MODEL pnn42ib       NPN
     + (is=0.02625f  bf=100        br=1.5        re=0        ikf=0.029
     +  vaf=46       ise=0         rb=744.7      rbm=189.2
     +  ikr=1.125m   var=3.58      isc=0.0311f   rc=58       nc=1.045
     +  nr=1         cje=131.6f    vje=0.9       mje=0.4     nf=1.008
     +  xti=5        cjc=60.4f     vjc=0.53      mjc=0.37    ne=1
     +  xtb=1.15     eg=1.11       tr=9.92n
     +  ptf=0        tf=35p        xtf=2.6       vtf=100     itf=10
     +  xcjc=0.1     fc=0.5)
*********************************************************************
.MODEL dsbwn41o      D
     + (cjo=789.8f   eg=1.15       vj=0.51     m=0.24)
*********************************************************************
.MODEL pnwn41o       NPN
     + (is=0.164f    bf=100        br=1.5        re=0        ikf=0.180
     +  vaf=46       ise=0         rb=83.2       rbm=38.7
     +  ikr=7.01m    var=3.58      isc=0.194f    rc=9.31     nc=1.045
     +  nr=1         cje=776.3f    vje=0.9       mje=0.4     nf=1.008
     +  xti=5        cjc=417.9f    vjc=0.53      mjc=0.37    ne=1
     +  xtb=1.15     eg=1.11       tr=9.92n
     +  ptf=0        tf=35p        xtf=2.6       vtf=100     itf=10
     +  xcjc=0.1     fc=0.5)
*********************************************************************
.MODEL grs003        D
     + (is=0.0427p   rs=53         n=1.044       tt=10p      cjo=54f
     +  vj=0.4       m=0.33        eg=0.69       xti=2       bv=30)
*********************************************************************
.MODEL dsubs003      D
     + (is=0.1f      rs=0          n=1           tt=500p     cjo=127f
     +  eg=1.15      vj=0.51       m=0.24        xti=3
     +  bv=35)
*********************************************************************
.MODEL ws102         D
     + (is=0.1p      rs=77         n=1.044       tt=10p      cjo=62.2f
     +  vj=0.4       m=0.33        eg=0.69       xti=2       bv=30)
*********************************************************************
.MODEL dsubs102      D
     + (is=0.1f      rs=0          n=1           tt=500p     cjo=85f
     +  eg=1.15      vj=0.51       m=0.24        xti=3
     +  bv=35)
*********************************************************************
.MODEL fpdf413       D
     + (is=0.902p    rs=3.78       n=1.044       tt=10p      cjo=755.1f
     +  vj=0.4       m=0.33        eg=0.69       xti=2       bv=30)
*********************************************************************
.MODEL dsbdf413      D
     + (is=0.1f      rs=0          n=1           tt=500p     cjo=780f
     +  eg=1.15      vj=0.51       m=0.24        xti=3
     +  bv=35)
*********************************************************************
.MODEL t05i1         NPN
     + (is=0.02118f  bf=100        br=1.5        re=1.533    ikf=21.3m
     +  vaf=46       ise=0.250f    rb=52.7       rbm=0       irb=0
     +  ikr=530u     var=3.58      isc=0.09562f  rc=26.33    nc=1.045
     +  nr=0.997     cje=67.7f     vje=1.037     mje=571.8m  nf=1
     +  xti=4.7      cjc=99.5f     vjc=0.603     mjc=0.266   ne=2
     +  xtb=1.15     cjs=152f      vjs=0.5052    mjs=0.3465  tr=9.92n
     +  ptf=20       tf=35p        xtf=2.6       vtf=1.67    itf=8.08m
     +  xcjc=69m     fc=0.8        eg=1.11)
```

```
*********************************************************************
.MODEL t08i1          NPN
     + (is=0.03333f  bf=100        br=1.5        re=1.333    ikf=33.6m
     +  vaf=46       ise=1.0f      rb=56.6       rbm=0       irb=0
     +  ikr=115m     var=3.58      isc=0.1847f   rc=22.86    nc=1.045
     +  nr=995m      cje=99.3f     vje=1.037     mje=571.8m  nf=1
     +  xti=4.7      cjc=124.4f    vjc=603m      mjc=266m    ne=2
     +  xtb=1.15     cjs=170.4f    vjs=505.2m    mjs=346.5m  tr=9.92n
     +  ptf=40       tf=35p        xtf=2.6       vtf=1.67    itf=8.08m
     +  xcjc=89m     fc=0.8        eg=1.11)
*********************************************************************
.MODEL t12b1          NPN
     + (is=0.057f    bf=100        br=1.5        re=1.25     ikf=82.8m
     +  vaf=46       ise=2.4f      rb=170        rbm=170     irb=1.7m
     +  ikr=0.27     var=3.58      isc=0.101f    rc=13.3     nc=1.045
     +  nr=1.019     cje=15f       vje=658m      mje=273m    nf=1
     +  xti=3        cjc=27f       vjc=603m      mjc=369m    ne=2
     +  xtb=1.15     cjs=101f      vjs=429m      mjs=259m    tr=9.92n
     +  tf=35p        xtf=2.6      vtf=1.4       itf=8m
     +  xcjc=620m    fc=5m         eg=1.11)
*********************************************************************
.MODEL t5406          NPN
     + (is=0.33f     bf=100        br=1.5        re=833m     ikf=0.48
     +  vaf=46       rb=86.6       var=3.58      rc=23.6     nc=1.045
     +  cje=.495p    cjc=722f      xtb=1.15      cjs=576f    tr=9.92n
     +  tf=35p       xtf=2.6       eg=1.11)
*********************************************************************
.MODEL tpnp2          PNP
     + (is=0.0769f   bf=70         br=1          rb=164      rc=56
     +  cje=86f      cjc=1.4p      tf=1n)
*********************************************************************
.MODEL c60pf          NPN
     + (is=0.88224f  bf=100        br=1.5        rb=141      rc=16
     +  re=0.3       cje=3.657p    cjc=2.927p    cjs=1.029p  nc=1.045
     +  eg=1.11)
*********************************************************************
.MODEL dres           D
     + (is=0.37f     cjo=414f)
*********************************************************************
.MODEL DSUBW113 D   (CJO=179.8FF eg=1.15   vj=.51 m=.24)
*********************************************************************
.MODEL PNW113 npn   (IS=2.45E-17 bf=100 NF=1.008 vaf=30.0 IKF=.0270
+  ISE=0 NE=1 br=1.5 NR=1 XCJC=.1 var=8.4
+  IKR=1.05MA ISC=2.9E-17 nc=1.045 RB=497.6 RBM=200
+  RE=0 RC=62.2
+  CJE=123.4FF vje=0.92 mje=0.413
+  CJC=68.3FF vjc=0.75 mjc=0.266
+  tf=35E-12 xtf=2.6 VTF=100 ITF=10A PTF=0
+  tr=9.92E-9 xtb=1.15 XTI=5 FC=.5
+  eg=1.11)
*********************************************************************
.MODEL WW113 D      (IS=4.6E-13 RS=60.1 N=1.044 TT=10PS
+  CJO=61.6FF VJ=.4 M=.33
+  EG=.69 XTI=2 FC=.5 BV=30)
```

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*********************************************************************
.MODEL DSUBW101 D   (CJO=109.4FF eg=1.15   vj=.51 m=.24)
.MODEL PNW101 npn   (IS=7E-18 bf=100 NF=1.008 vaf=30.0 IKF=.0077
+  ISE=0 NE=1 br=1.5 NR=1 XCJC=.1 var=8.4
+  IKR=.3MA ISC=8.28E-18 nc=1.045 RB=1508.3 RBM=466.7
+  RE=0 RC=217.6
+  CJE=41.3FF vje=0.92 mje=0.413
+  CJC=32FF vjc=0.75 mjc=0.266
+  tf=35E-12 xtf=2.6 VTF=100 ITF=10A PTF=0
+  tr=9.92E-9 xtb=1.15 XTI=5 FC=.5
+  eg=1.11)
*********************************************************************
.MODEL WW101 D      (IS=2.15E-13 RS=125.3 N=1.044 TT=10PS
+  CJO=28.8FF VJ=.4 M=.33
+  EG=.69 XTI=2 FC=.5 BV=30)
*********************************************************************
*********************************************************************

.END
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