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AN1504/D

Metastability and the ECLinPS™ Family

Prepared by: Applications Engineering

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APPLICATION NOTE

This application note examines the concept of metastability and provides a theoretical discussion of how it occurs, including examples of the metastable condition. An equation characterizing metastability and a test circuit derived from that equation are presented. Metastability results are then applied to the ECLinPS family.

Introduction

Metastability is a central issue anytime a designer wishes to synchronize two or more asynchronous signals. A popular method for accomplishing this task is to employ a D flip−flop as the synchronizing element (Figure 1).

As shown in Figure 1, synchronization can be accomplished using a single D flip−flop; more typically, several D flip−flops are cascaded to provide synchronization while reducing the probability of a metastable or "anomalous" state occurring at the input of System 2. Unfortunately the information at the data and clock inputs of flip−flops used as synchronizing elements is asynchronous by nature, thus the manufacturer specifications for set−up and hold times may not be observed. A series of timing diagrams is shown in Figure 2 demonstrating three possible timing relationships between the data and clock signals; to the right of each data trace is the corresponding output waveform. In the first case the data adheres to the specified set−up and hold times, hence the output attains the proper state. In case 2 the set−up time is violated such that the output of the D flip−flop does not change state. Case 3 represents a violation of the set−up and hold times whereby the D flip−flop enters a metastable state. The resolving time for a flip−flop in this metastable state is indeterminate. Further, the final settling state of the flip−flop having been in this metastable condition cannot be guaranteed.

Metastability Theory

A bistable device such as a flip−flop has two stable output states: the "1" or high state and the "0" or low state. When the manufacturers specified set−up and hold times are observed the flip−flop will achieve the proper output state (Figure 3). However if the set−up and hold times are violated the device may enter a metastable state, thereby increasing the propagation delay, as indicated by the output response shown in Figure 4.

To better understand flip−flop metastability, the operation of a typical ECLinPS D flip−flop is reviewed. The schematic of a D flip−flop is shown in Figure 5.

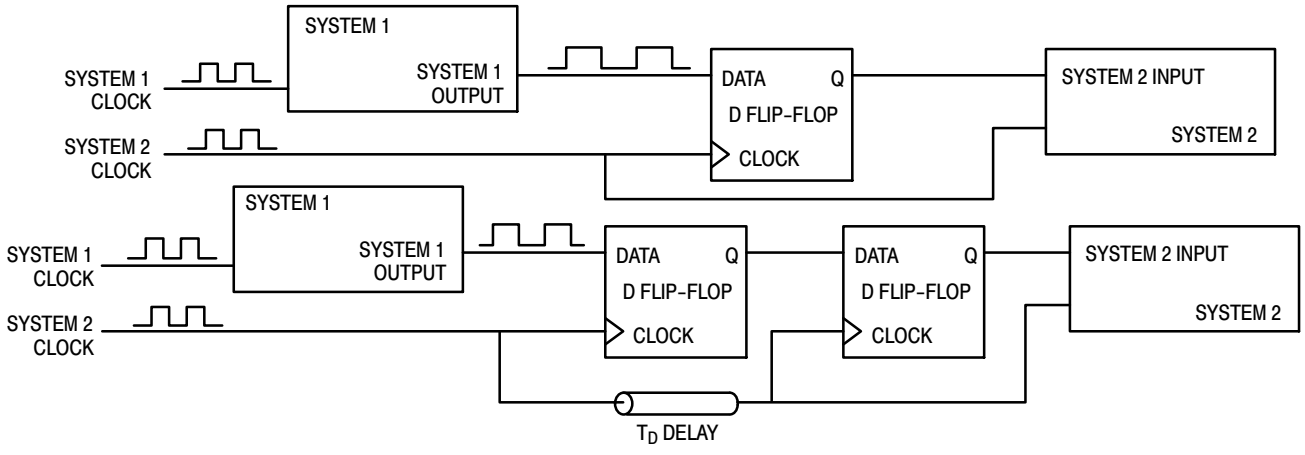

Figure 1. Clock Synchronization Schemes

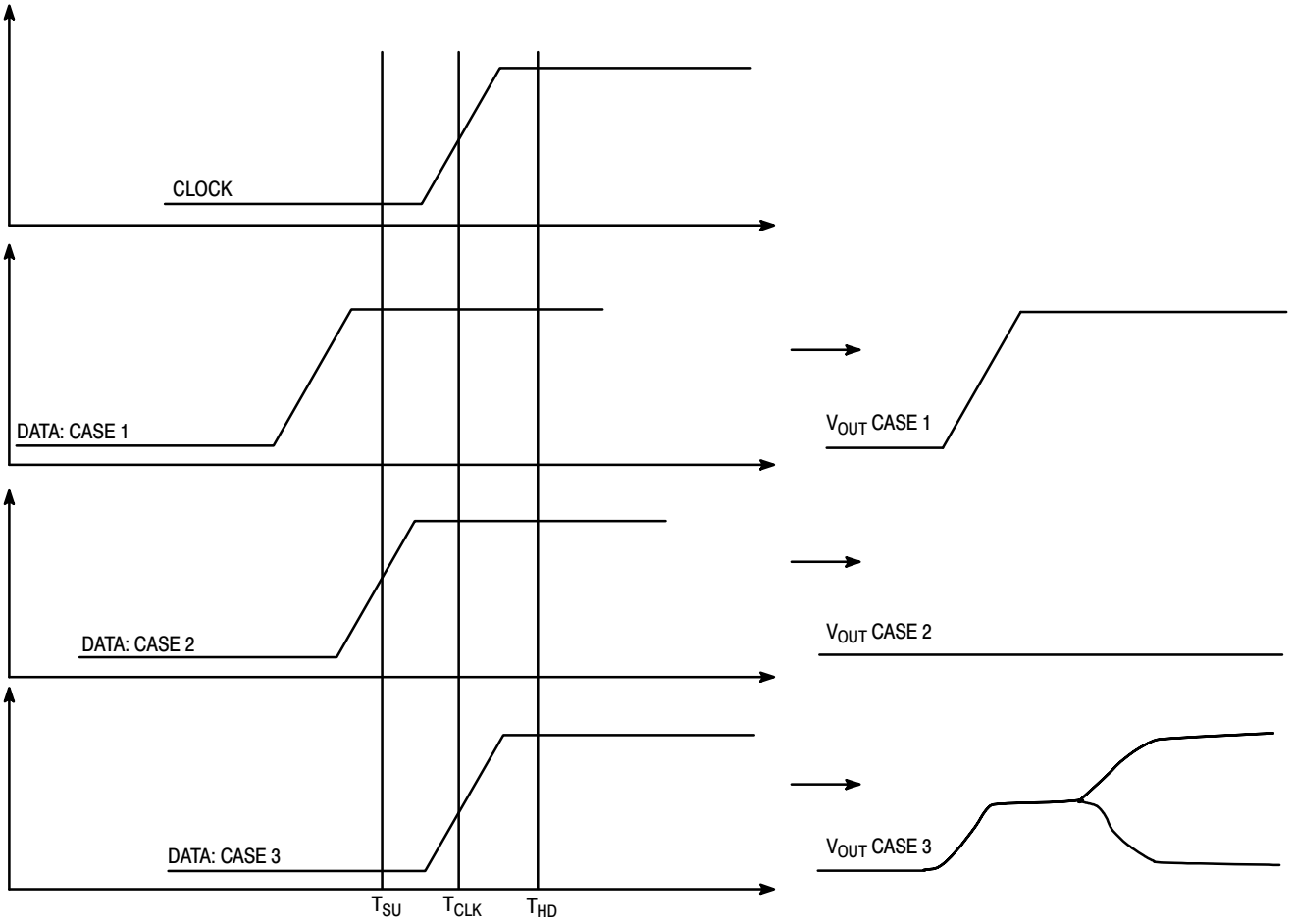

Figure 2. Timing Relationships Between Data and Clock Signals for a D Flip−Flop

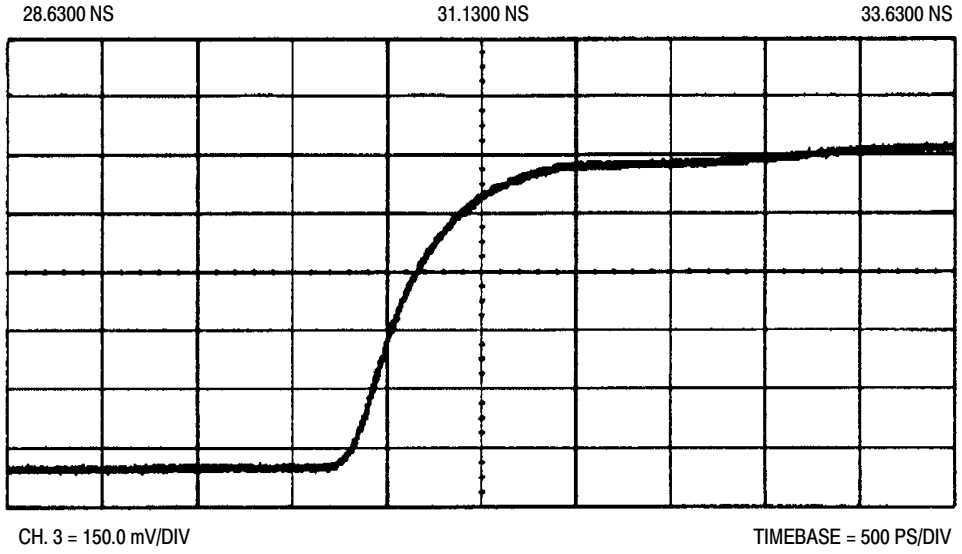

Figure 3. Typical Flip−Flop Output Response

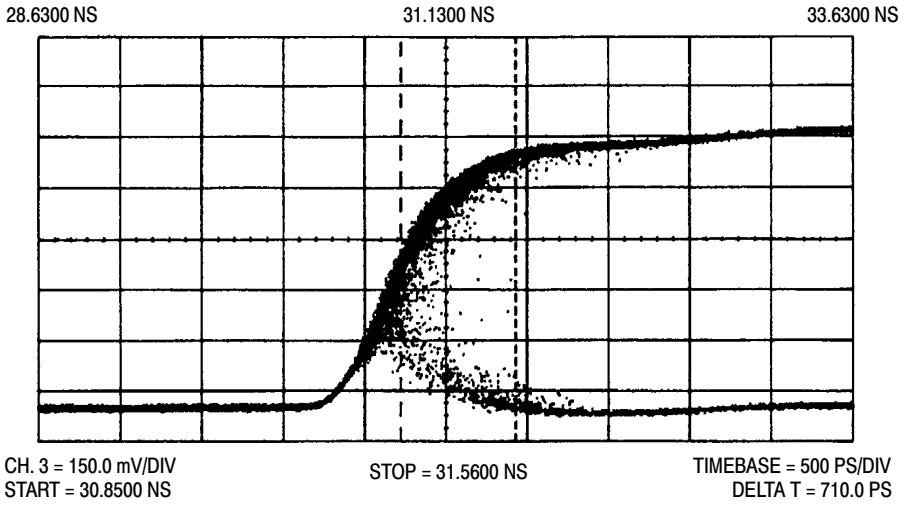

Figure 4. Metastable Flip−Flop Output Response

The flip−flop shown in Figure 5 can be divided into two functional blocks: Master latch and Slave latch. Under optimal operating conditions the clock is low when data arrives at the input to the master latch; after the specified set−up time the clock input is raised to a high level, and the data is latched. When the clock signal goes to the low state, the slave portion of the circuit becomes transparent and transfers the latched data to the output. Changes at the input will have no affect on the output when the "slave latch" is transparent.

The master and slave latches each consist of two subsections: Data and Regenerative (Figure 5). Since the master latch accepts signals from external sources it is the section most susceptible to metastability problems. When the clock signal goes to a high state the current in the master latch clock differential pair switches from the regenerative to the data side. If the set−up and hold times are observed the circuit will function properly. However, if the data and clock signals change such that the set−up and hold times are violated, the data differential pair, the regenerative differential pair and the clock differential pair for the master will share the same switch current. In addition there will not be enough current to charge and discharge the transistor parasitic capacitances, creating an RC feedback loop via the collector nodes of the data and regenerative differential pairs. Thus the master latch enters a metastable state which appears at the output since the slave latch is transparent under these conditions. Theoretically, there is no upper bound on the length of time this metastable state can last, although in practice circuits eventually do leave the metastable region.

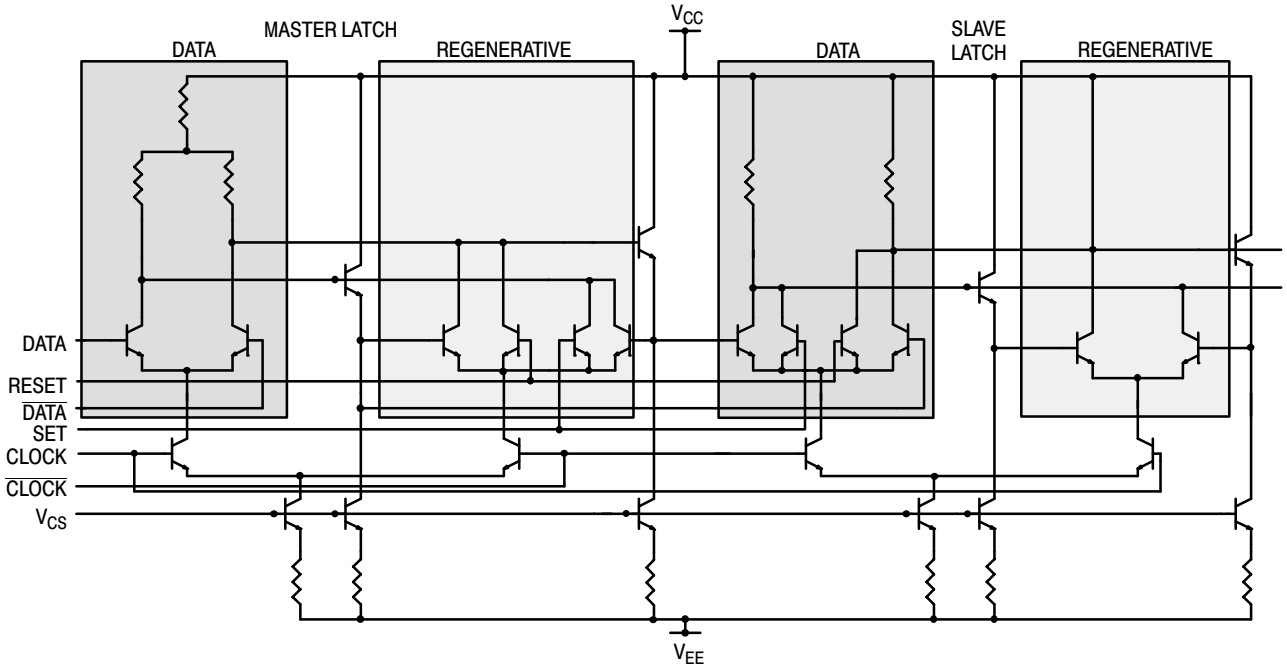

Figure 5. ECLinPS D Flip−Flop

Metastable Equations

Flip−flop propagation delay as a function of the input signal is represented in Figure 6.

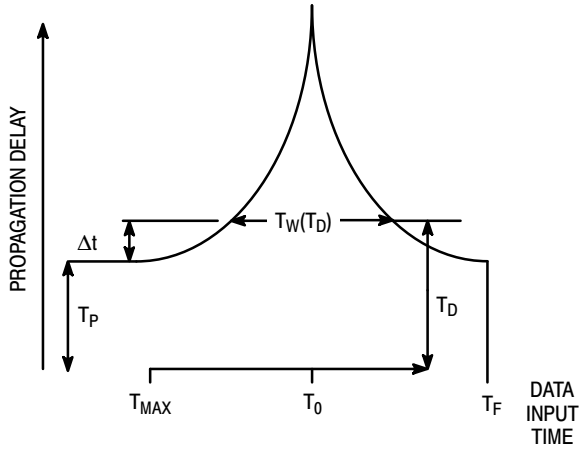

Figure 6. Flip−Flop Response Time Plot

The ordinate is the flip−flop propagation delay time, and the abscissa is the time that data arrives at the flip−flop input relative to reference time, T_0. For devices with positive set−up times T_0 represents the clock transition time with the difference between T_0 and T_{MAX} being the minimum allowable set−up time. Thus data arriving before time T_{MAX} will elicit a nominal propagation delay, T_P, when clocked. For data appearing between times T_{MAX} and T_F the propagation delay will be longer than T_P because the set−up and/or hold times have been violated; and the device enters the metastable state. Data occurring at the input after time T_F will have no affect on the output, hence the output does not change and the propagation delay is defined as zero.

For devices with zero or negative set−up times the same response plot applies, however the abscissa is shifted such that the value of T0 is no longer the clock transition time. The same concepts are valid for derivation of metastability equations for each case: positive, negative or zero set−up and hold times. To clarify the flip−flop response plot, Figure 7 illustrates a case in which the propagation delay is T_P. Data arrives at time T_A, allowing the proper set−up time prior to a clock transition and is maintained at this level for the specified hold time. Figure 8 is an example in which the propagation delay is longer than T_P since the data arrives at time T_A, violating the set−up time.

Using the response plot in Figure 6, Stoll[1] developed the concept of a failure window to facilitate the characterization of metastability. The value of $T_W(T_D)$ is the width of the window for which a propagation delay of time duration T_D occurs, and is the range of data input times relative to the clock input for which a failure will occur. The value of T_D is the maximum allowable propagation delay; delays longer than T_D constitute a failure. The failure window is described mathematically as:

$$T_W(T_D) = T_P \times 10^{(\Delta t)/t} \qquad \text{(eq. 1)}$$

Where:

$T_W(T_D)$	Failure Window Width
T_P	Nominal Propagation Delay
T_D	Delay After Clock That Constitutes a Failure
τ	Flip−Flop Resolution Time Constant
Δt	Excess Delay ($T_D - T_P$)

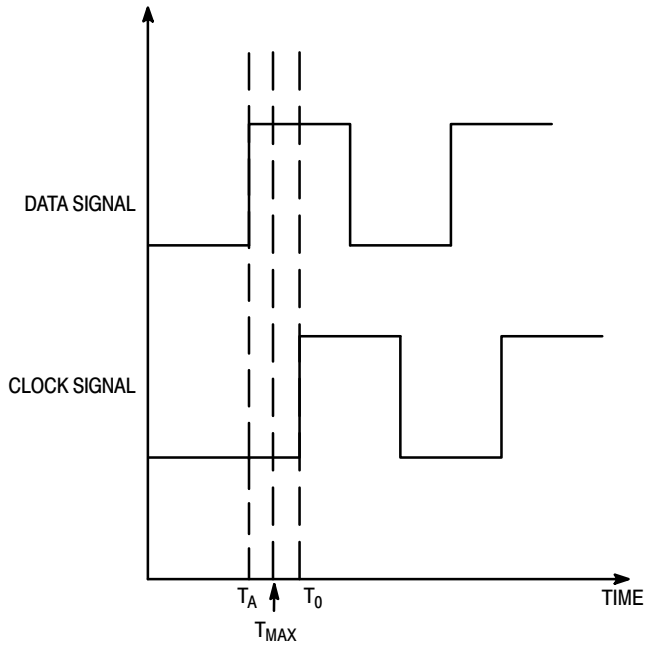

Figure 7. Proper Set−Up and Hold Times

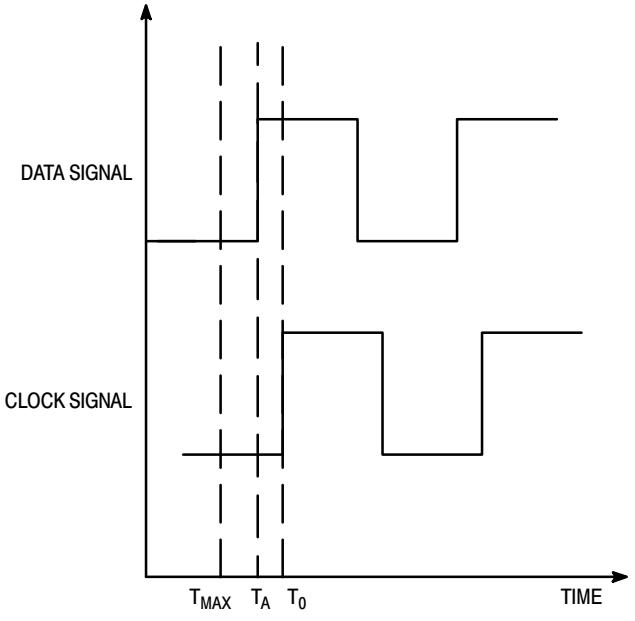

Figure 8. Violation of Set−Up and Hold Times

This equation only applies for narrow window widths, i.e., those times well up on the response plot of Figure 6.

To summarize, when the set−up and hold times are obeyed the flip−flop will have a nominal propagation delay, T_P. If the data and clock signals arrive such that the set−up and hold times are violated there will be an excess delay as indicated in the response plot of Figure 6. This excess delay is caused by the flip−flop entering the metastable region. For data signals arriving much later than the clock signal the flip−flop will not change state, thus the propagation delay is zero by definition. The window width is the range of input arrival times relative to the clock for which the output response does not attain a defined value within the time period T_D. Since T_D represents the maximum allowable delay, the window width represents the relative range of input times for which a failure will occur.

Equation 1 can be combined with the industry accepted definition for system level Mean Time Between Failures (Equation 2)[2] to derive an equation yielding Mean Time Between Failures as a function of system design and semiconductor device parameters.

$$MTBF = 1/(2 * f_C * f_D * T_W(T_D)) \quad \text{(eq. 2)}$$

Where:

f_C Clock Frequency

f_D Data Frequency

$$MTBF = 1/(2 * f_C * f_D * T_P * 10 - (\Delta t)/\tau) \quad \text{(eq. 3)}$$

The System Designer can use Equation 3 to address the issue of metastability. Device τ values are provided in Table 2, " τ Values for Several Flip−Flops" and T_P (Nominal Propagation Delay) value is provided in the device datasheet. MTBF, f_c and f_d are system design parameters. Thus the designer can use this equation to determine the value of T_D.

Test Circuitry For Metastable Evaluation

Equation 3 provides the impetus for the design of a metastability test circuit capable of providing a value of τ, the flip−flop resolution time constant. Transforming this equation into a "linear" form by taking the logarithm of both sides yields Equation 4:

$$\log MTBF = -\log \cdot (2 * f_C * f_D * T_P) + \Delta t/\tau \quad \text{(eq. 4)}$$

Plotting log MTBF versus Δt yields a line with slope $1/\tau$, and log MTBF intercept of $-\log(2*f_c*f_d*T_P)$. Thus, the test circuit must accept the clock and data input frequencies as a function of Δt and yield MTBF as an output. The circuit configuration shown in Figure 9 fulfills these criteria.

The test circuitry can be categorized into five functional blocks: DUT, adjustable delay portion, comparator section, counter−set circuitry, and the counter. Starting with the comparator portion of the circuit, the output of the DUT is fed into the comparator; if the DUT output falls in the range $V_{BB} - 0.15\ V < V_{BB} < V_{BB} + 0.15\ V$, the DUT is defined as being in a metastable condition (Figure 10).

For DUT output states in the metastable region the comparator output attains a logic high level. When the DUT output does not fall within this range it is in a "defined high or low level," and the output of the comparator will be at a logic low level. If the comparator output is at a logic high level, indicating metastability, the counter−set section sends out a periodic waveform which increments the counter. If the DUT is not metastable the output of the "counter−set" circuitry is constant and the counter (HP−8335A) is not incremented. The total number of counts over a specified time period is a measure of MTBF.

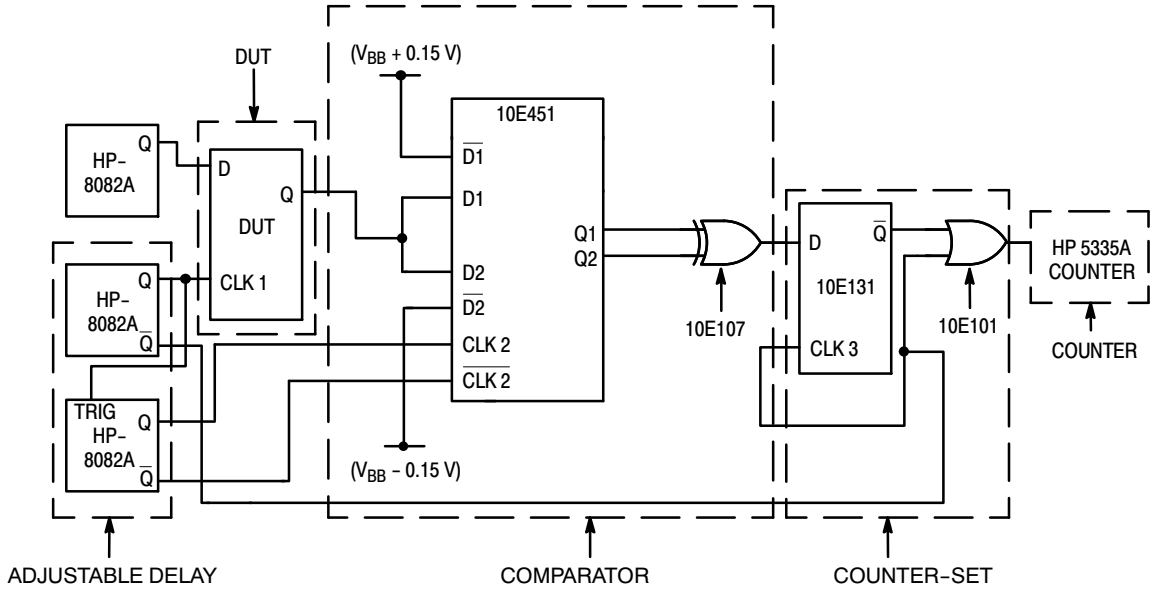

Figure 9. Metastability Test Circuit

Pulse generator #1 (PG1) supplies the data signal to the DUT. To ensure asynchronous signals between the DUT data and clock signals, a separate pulse generator, PG2, provides the clock signal to the DUT. Generator PG2 also provides the clocking signal to the comparator circuitry via its inverting output terminal. Pulse generator PG3 supplies the clock signals to the E451 portion of the comparator section. To increase the probability of the DUT entering the metastable state the DUT data frequency is set at 1.33 times the DUT clock frequency. The value of Δt is the delay between the noninverting clock signals for the DUT and the E451. Finally, the inverting terminal of PG2 supplies the clock signal for the counter−set circuitry.

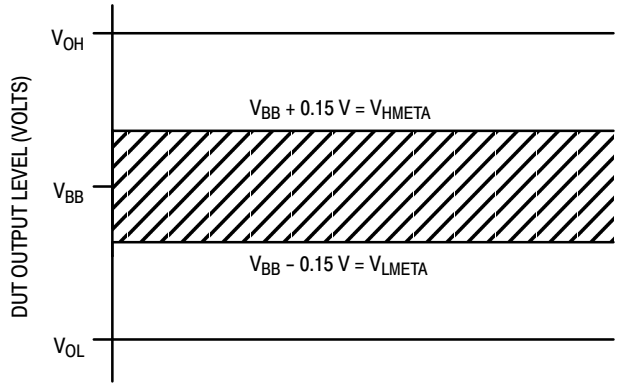

Figure 10. Output Response Defining the Metastable Region

To take advantage of the precision 50 Ω input impedance of the test measurement equipment, the circuit power supplies are shifted by +2.0 V. Thus all input signals, bias voltages, and comparator values have been shifted by +2.0 V as shown in Table 1.

Table 1. ECL LEVELS AFTER TRANSLATING BY +2.0 V

Parameter	Typical (V)		Shifted (V)	
	10E	100E	10E	100E
V_{IL}	−1.75	−1.70	+0.25	+0.30
V_{IH}	−0.90	−0.95	+1.10	+1.05
V_{BB}	−1.30	−1.30	+0.70	+0.70
V_{CC}	0.00	0.00	+2.00	+2.00
V_{EE}	−5.20	−4.50	−3.20	−2.50
V_{Hmeta}	−1.15	−1.15	+0.85	+0.85
V_{Lmeta}	−1.45	−1.45	+0.55	+0.85

Results

An example of using a log MTBF versus Δt plot to determine τ is shown in Figure 11.

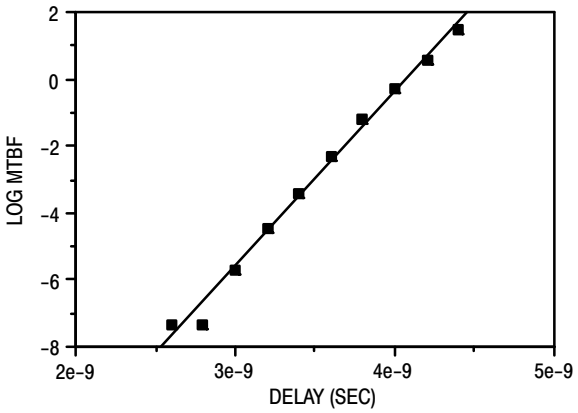

Figure 11. Plot of Log MTBF versus Delay

From Equation 4 the slope of the line is the reciprocal of τ. Measurements similar to these were performed to characterize the ECLinPS family as well as D flip−flops from various vendors. The results are shown in Table 2:

Table 2. τ Values for Several Flip−Flops

Device Type	Resolution Time Constant (τ)
ON Semiconductor NBSG53A	80 psec
ON Semiconductor MC10EP31	100 psec
ON Semiconductor MC10E431	125 psec
ON Semiconductor MC10E151	185 psec
ON Semiconductor MC10E131	200 psec
ON Semiconductor MC10H131	718 psec
Signetics 100131	890 psec
Signetics 100151	1172 psec
National 100131	1594 psec

Having determined the value of τ, the system designer can use this information in conjunction with Equation 3 to aid in optimizing the system design.

Example

As an example, assume the system configuration shown in Figure 12, in which the output from System 1 is to be synchronized to System 2 using a 10E151 D flip−flop.

Further, the equivalent output signal for System 1 is 75 MHz whereas the clock frequency for System 2, as well as the synchronizing element, is 100 MHz. Under these conditions the data and clock inputs to the D flip−flop are asynchronous and the system designer must consider the possibility of the D flip−flop entering the metastable state. Therefore the system designer must determine how long the flip−flop will remain in the metastable region in order to

decide when the data at the output of the flip−flop will attain a defined state and can be clocked into System 2.

The solution to this dilemma is found with Equation 3:

$$MTBF = 1/(2 * f_C * f_D * T_P * 10 - (\Delta t)/\tau) \quad \text{(eq. 5)}$$

The values for f_C and f_D were specified as 100 MHz and 75 MHz, respectively. Assuming the D flip−flop is an ON Semiconductor 10E151, a worse case value of propagation delay (Tp) of 800 psec is obtained from the ECLinPS Device Data Book. The value of t is given in Table 2 as 185 psec. Substituting these values into Equation 3 yields:

$$MTBF = 1/(2 * f_C * f_D * T_P * 10 - (\Delta t/185\ \text{psec})) \quad \text{(eq. 6)}$$

At this point the system designer must specify an acceptable MTBF. For this example an MTBF of 5 years is assumed. Therefore the value of Δt is calculated to be

$\Delta t = 2.83$ nsec

From the relationship

$\Delta t = T_D - T_P$

the value of T_D is calculated to be

$T_D = 3.63$ nsec

Thus for an MTBF of 5 years the designer should delay the clocking of the data from the output of the flip−flop into System 2 by 3.63 nsec.

Conclusion

Metastability has become a critical issue with system designers. In order to better serve our customers, ON Semiconductor has characterized the ECLinPS family for metastability using the concept of a failure window. The nominal flip−flop resolution time constant for the ECLinPS family, excluding the E131 and E431 devices as these flip−flops use alternative architectures, has been determined to be 185 psec. The resolution time constant for the E131 and E431 devices is 200 psec and 125 psec, respectively. Thus the system designer can use the value of τ in conjunction with Equation 3 to determine the metastable induced excess delay for a specified MTBF. Although this application note does not present a method for avoiding metastability, it does provide a means for the designer to quantitatively incorporate metastability in their designs.

References

1. Stoll, P. “How to Avoid Synchronization Problems” VLSI Design, November/December 1982. pp. 56−59.
2. Nootbaar, K. “Design, Testing, and Application of a Metastable−Hardened flip−flop,” Wescon/87, Section 16−2 pp. 1−9.

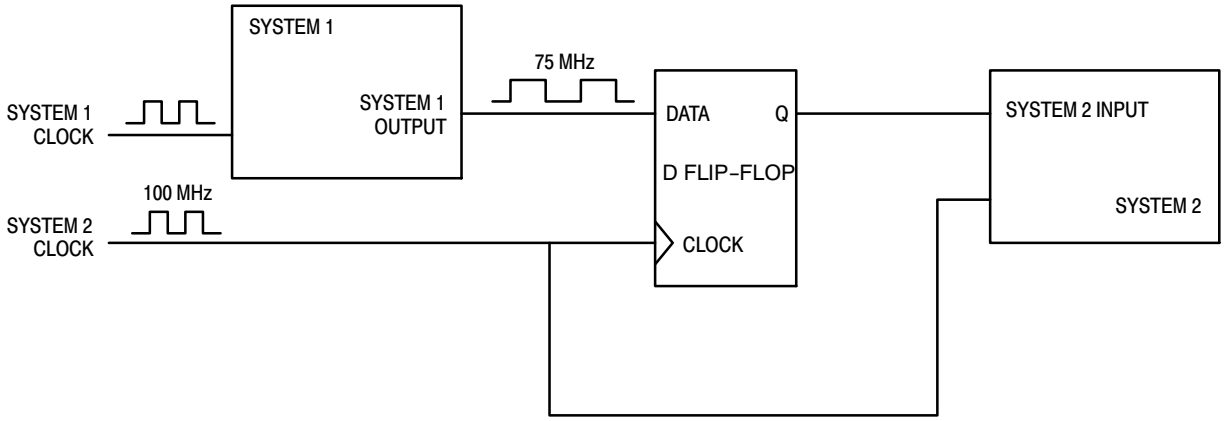

Figure 12. System Example

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