AN1403/D

FACT™ I/O Model Kit

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ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

OBJECTIVE

The objective of providing a spice modelling kit is to allow the customer to perform system level interconnect modelling for the ON Semiconductor FACT logic family. It is not intended for the purpose of performing extensive device modelling.

Schematic Information

The kit contains representative circuit schematics of the different I/O structures and a worst case package model schematic used in the FACT family.

Input Structures

There are three basic variations of the input structures (Figures 1. , 2. , and 3.). In all of the schematics, the clamping diodes are shown and the appropriate PMOS:NMOS ratios of the inverter stage. Actual MOS gate sizes may vary, but the ratio will be maintained. The variation of size is the result of custom designing each functional device for speed, which may require different build−up ratios (BUR). For 74ACxxx devices, both ON Semiconductor and Fairchild (second source) use the identical Input buffer structures. However, the for 74ACTxxx devices (TTL input buffer) will vary depending on the source of the design. Once again, the appropriate P:N ratios are depicted in the figures.

Output Structure

There are two represented output structures (Figures 4. and 5.); one is the standard output buffer and the other is with tri-state. The size range of this standard output buffer is listed in the figure as:

P-channel (1570 – 1900)

N-channel (780 – 900)

Typically, ON Semiconductor designs use a 1600/800 size output buffer.

Transistor Parameters for Typical FACT Output Buffers

1600/800 FACT Output Buffer

PMOS L=2U W=1599U AD=5192.8P AS=4504.1P PD=1690.4U PS=1874.7U+NRD=9.375E−4 NRS=9.375E−4

NMOS L=2U W=799U AD=2596.4P AS=2502.3P PD=845.2U PS=1041.5U +NRD=1.875E−3 NRS=1.875E−3

1900/900 FACT Output Buffer

PMOS L=2U W=1899U AD=6163.6P AS=5227.3P PD=2013.0U PS=2181.3U +NRD=7.895E−4 NRS=7.895E−4

NMOS L=2U W=899U AD=2918.0P AS=2699.7P PD=956.5U PS=1129.8U +NRD=1.667E−3 NRS=1.667E−3

Package Model

The package model represents the parasitics as they are seen on a corner pin GND & V_{CC} for a 20-pin plastic DIP type package (Figure 6.). For 14-pin and 16-pin plastic DIP packages, reduce inductance by 20% from the 20 pin model. To simulate an SOIC type package, reduce the inductance of the appropriate DIP model by 50%.

Spice Parameter Information

In addition to the schematics, a listing of the spice parameters for the transistors are referenced and included (Page 4). These parameters can be used for best, typical, and worst case simulations.

Summary

The information included in this kit should provide the basic information necessary to do Spice level interconnect modelling. If any clarification or additional information is necessary, the user is encouraged to contact the FACT Applications or Design personnel for assistance.

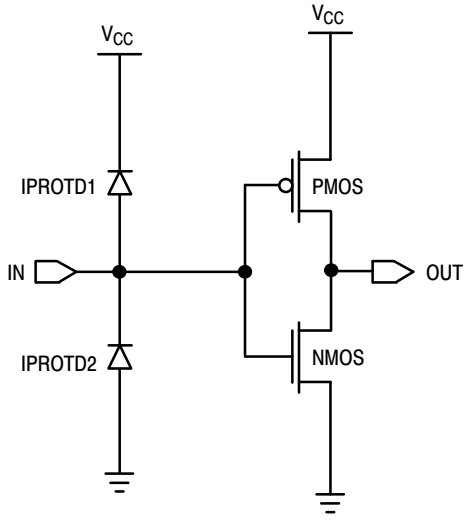

Figure 1. Fairchild/ON Semiconductor 74ACxxx Input Buffer P/N Ratio = 'P:N = 2.5:1'

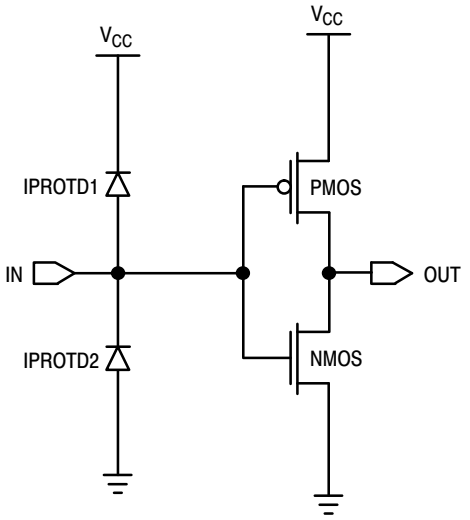

Figure 2. Fairchild 74ACTxxx TTL Input Buffer P/N Ratio = 'P:N = 1:4'

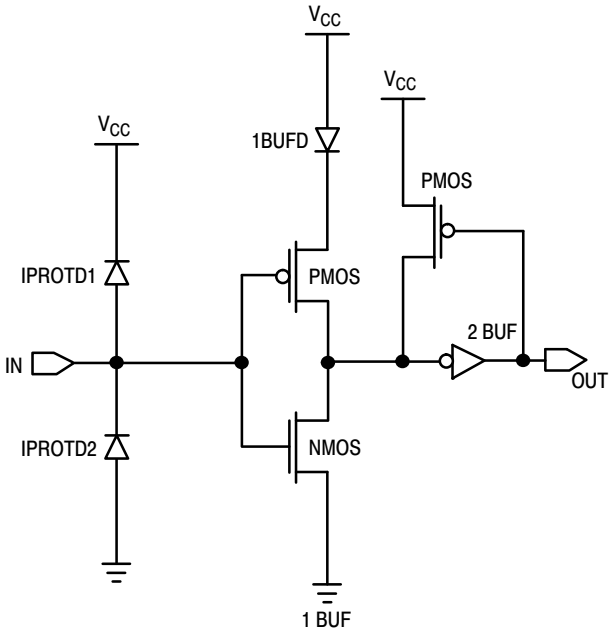

Figure 3. ON Semiconductor 74ACTxxx TTL Input Buffer 1 BUF P/N Ratio = 'P:N = 1:2.5' 2 BUF P/N Ratio = 'P:N = 1:1'

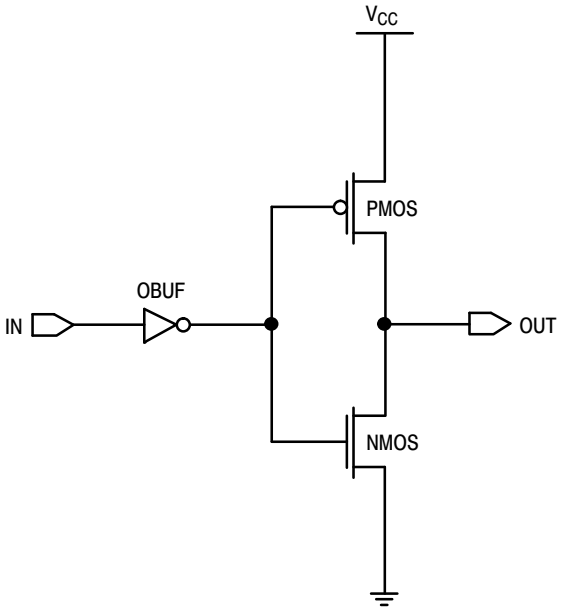

Figure 4. Standard Output Buffer P-Channel Device Size Range (1570→1900) N-Channel Device Size Range (780→900)

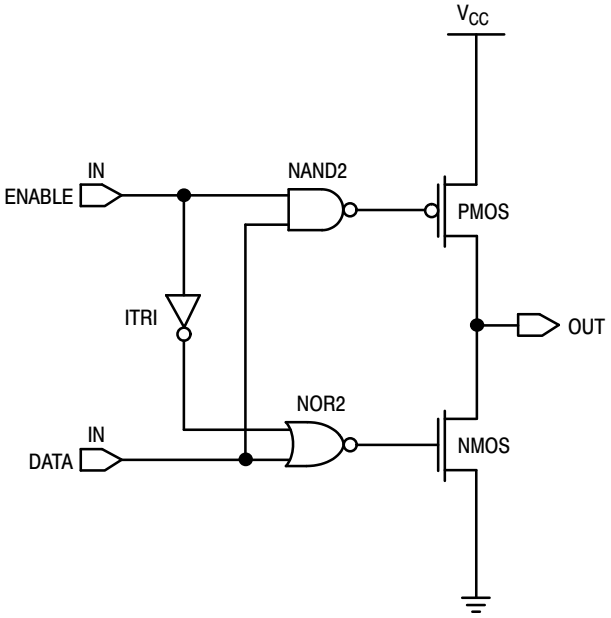

Figure 5. Standard Tri-State Output Buffer P-Channel Device Size Range (1570→1900) N-Channel Device Size Range (780→900)

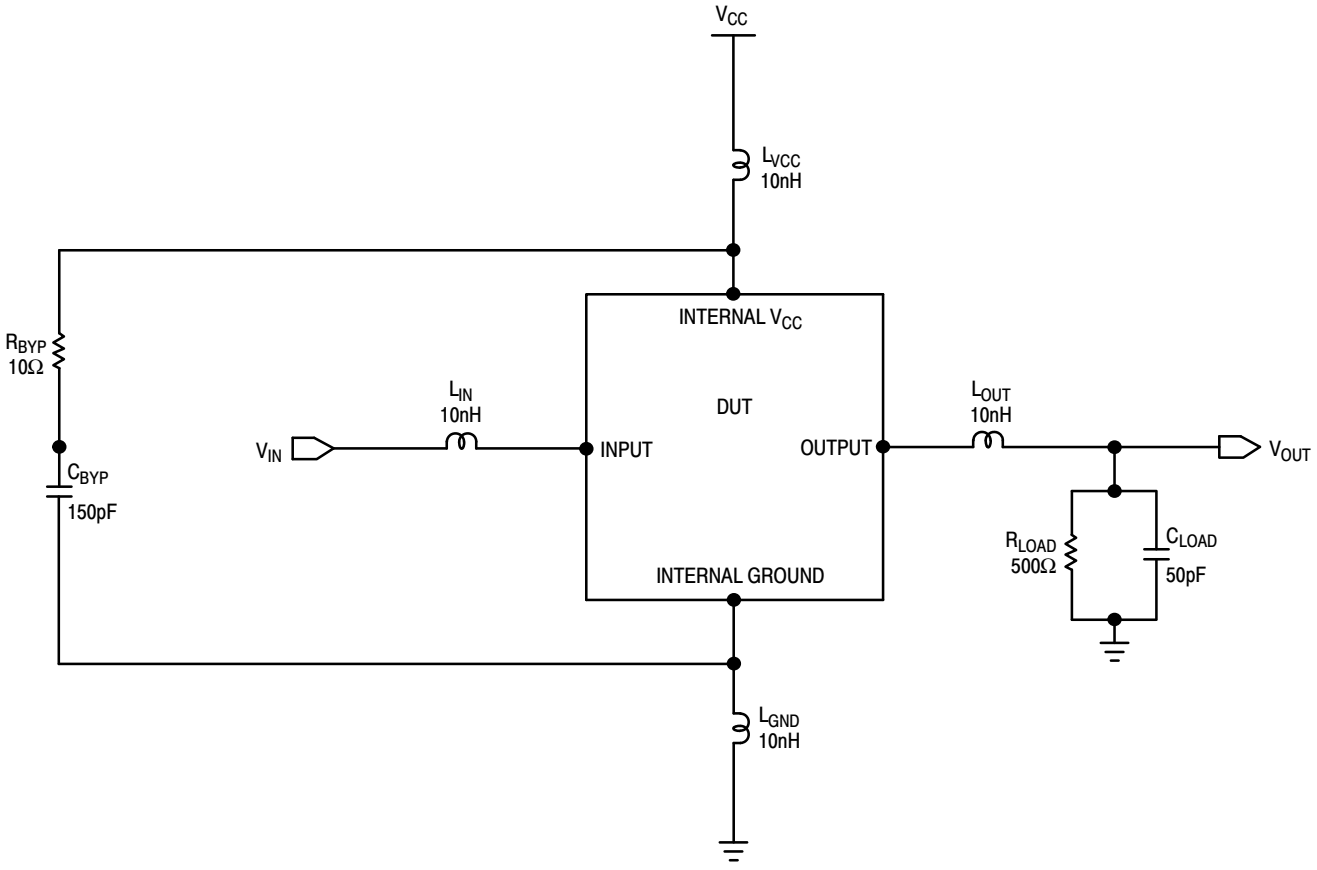

Figure 6. Package Model for FACT Circuits

MSPICE SIMULATION CARDS

Note:
$BPBN − Best PMOS, Best NMOS
$BPWN − Best PMOS, Worst NMOS
$TPTN − Typical PMOS, Typical NMOS
$WPBN − Worst PMOS, Best NMOS
$WPWN − Worst PMOS, Worst NMOS

```
$BPBN
.MODEL NMOS NMOS LEVEL=3   VTO=0.525 TOX=2.3E−8 NSUB=2.9E16
+                          XJ=2.5E−7 LD=4.75E−7 UO=537.8 VMAX=1.45E5 DELTA=1.4
+                          THETA=0.038 ETA=0.12 KAPPA=0.06 RSH=40 NFS=2.4E11
+                          CGSO=3.5E−10 CGDO=3.5E−10 PB=0.95 CJ=5.8E−4
+                          MJ=0.4 CJSW=1.1E−9 MJSW=0.36 TPG=1 XQC=0.4

.MODEL PMOS PMOS LEVEL=3   VTO=−0.55 TOX=2.3E−8 NSUB=1E16
+                          XJ=3E−7 LD=4.75E−7 UO=199.7 VMAX=1.4E5 DELTA=0.75
+                          THETA=0.08 ETA=0.09 KAPPA=2.5 RSH=120 NFS=1.68E11
+                          CGSO=6.2E−10 CGDO=6.2E−10 PB=0.87 CJ=2.42E−4
+                          MJ=0.4 CJSW=4.66E−10 MJSW=0.36 TPG=−1 XQC=0.4
#
$BPWN
#
.MODEL PMOS PMOS LEVEL=3   VTO=−0.55 TOX=2.3E−8 NSUB=1E16
+                          XJ=3E−7 LD=4.75E−7 UO=199.7 VMAX=1.4E5 DELTA=0.75
+                          THETA=0.08 ETA=0.09 KAPPA=2.5 RSH=120 NFS=1.68E11
+                          CGSO=6.2E−10 CGDO=6.2E−10 PB=0.87 CJ=2.42E−4
+                          MJ=0.4 CJSW=4.66E−10 MJSW=0.36 TPG=−1 XQC=0.4

.MODEL NMOS NMOS LEVEL=3   VTO=0.865 TOX=2.8E−8 NSUB=2.9E16
+                          XJ=2.5E−7 LD=2.25E−7 UO=537.8 VMAX=1.45E5 DELTA=1.4
+                          THETA=0.038 ETA=0.12 KAPPA=0.06 RSH=60 NFS=2.4E11
+                          CGSO=3.5E−10 CGDO=3.5E−10 PB=0.95 CJ=5.8E−4
+                          MJ=0.4 CJSW=1.1E−9 MJSW=0.36 TPG=1 XQC=0.4
#
$TPTN
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+                          XJ=2.5E−7 LD=3.5E−7 UO=537.8 VMAX=1.45E5 DELTA=1.4
+                          THETA=0.038 ETA=0.12 KAPPA=0.06 RSH=41 NFS=2.4E11
+                          CGSO=3.5E−10 CGDO=3.5E−10 PB=0.95 CJ=5.8E−4
+                          MJ=0.4 CJSW=1.1E−9 MJSW=0.36 TPG=1 XQC=0.4

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+                          XJ=3E−7 LD=3.5E−7 UO=199.7 VMAX=1.4E5 DELTA=0.75
+                          THETA=0.08 ETA=0.09 KAPPA=2.5 RSH=146 NFS=1.68E11
+                          CGSO=6.2E−10 CGDO=6.2E−10 PB=0.87 CJ=2.42E−4
+                          MJ=0.4 CJSW=4.66E−10 MJSW=0.36 TPG=−1 XQC=0.4
#
$WPBN
#
.MODEL NMOS NMOS LEVEL=3   VTO=0.525 TOX=2.3E−8 NSUB=2.9E16
+                          XJ=2.5E−7 LD=4.75E−7 UO=537.8 VMAX=1.45E5 DELTA=1.4
+                          THETA=0.038 ETA=0.12 KAPPA=0.06 RSH=40 NFS=2.4E11
+                          CGSO=3.5E−10 CGDO=3.5E−10 PB=0.95 CJ=5.8E−4
+                          MJ=0.4 CJSW=1.1E−9 MJSW=0.36 TPG=1 XQC=0.4
```

```
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+                           THETA=0.08 ETA=0.09 KAPPA=2.5 RSH=160 NFS=1.68E11
+                           CGSO=6.2E−10 CGDO=6.2E−10 PB=0.87 CJ=2.42E−4
+                           MJ=0.4 CJSW=4.66E−10 MJSW=0.36 TPG=−1 XQC=0.4
#
$WPWN
#
.MODEL NMOS NMOS LEVEL=3    VTO=0.865 TOX=2.8E−8 NSUB=2.9E16
+                           XJ=2.5E−7 LD=2.25E−7 UO=537.8 VMAX=1.45E5 DELTA=1.4
+                           THETA=0.038 ETA=0.12 KAPPA=0.06 RSH=60 NFS=2.4E11
+                           CGSO=3.5E−10 CGDO=3.5E−10 PB=0.95 CJ=5.8E−4
+                           MJ=0.4 CJSW=1.1E−9 MJSW=0.36 TPG=1 XQC=0.4

.MODEL PMOS PMOS LEVEL=3    VTO=−0.89 TOX=2.8E−8 NSUB=1E16
+                           XJ=3E−7 LD=2.25E−7 UO=199.7 VMAX=1.4E5 DELTA=0.75
+                           THETA=0.08 ETA=0.09 KAPPA=2.5 RSH=160 NFS=1.68E11
+                           CGSO=6.2E−10 CGDO=6.2E−10 PB=0.87 CJ=2.42E−4
+                           MJ=0.4 CJSW=4.66E−10 MJSW=0.36 TPG=−1 XQC=0.4
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