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AN-9738

Design Guideline on 150W Power Supply for LED Street Lighting Design Using FL7930B and FAN7621S

Introduction

This application note describes a 150W rating design guideline for LED street lighting. The application design consists of CRM PFC and LLC SRC with high power factor and high power conversion efficiency using FL7930B and FAN7621S. To verify the validity of the application board and scheme, a demonstration board 150W (103V/1.46A) AC-DC converter was implemented and its results are presented in this application note. In CRM active PFC, the most popular topology is a boost converter. This is because boost converters can have continuous input current that can be manipulated with peak current mode control techniques to force peak current to track changes in line voltage. The FAN7930B is an active Power Factor Correction (PFC) controller for boost PFC applications that operate in critical conduction mode (CRM). Since it was first introduced in early 1990s, LLC-SRC (series resonant converter) has became a most popular topology because of its outstanding performance in areas such as the output regulation of switching frequency, ZVS capability for entire load range, low turn-off current, small resonant components using the integrated transformer, zero current switching (ZCS), and no reverse recovery loss on secondary rectifier. Figure 1 shows the typical application circuit, with the CRM PFC converter in the front end and the LLC SRC DC-DC converter in the back end. FL7930B and FAN7621S achieve high efficiency with medium power for 150W rating applications where CRM and LLC SRC operation with a two-stage shows best performance. CRM boost PFC converters can achieve better efficiency with light and medium power rating than Continuous Conduction Mode (CCM) boost PFC converters. These benefits result from the elimination of the reverse-recovery losses of the boost diode and Zero-Current Switching (ZCS). The LLC SRC DC-DC converter achieves higher efficiency than the conventional hard switching converter. The FL7930B provides a controlled on-time to regulate the output DC voltage and achieves natural power factor correction. The FAN7621S includes a high-side gate driver circuit, accurate current-controlled oscillator, frequency -limit circuit, soft-start, and built-in protections. The high-side gate drive circuit has a common-mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. Using Zero Voltage Switching (ZVS) dramatically reduces switching losses and significantly improves efficiency. ZVS also reduces switching noise noticeably, which allows a small-sized Electromagnetic Interference (EMI) filter.

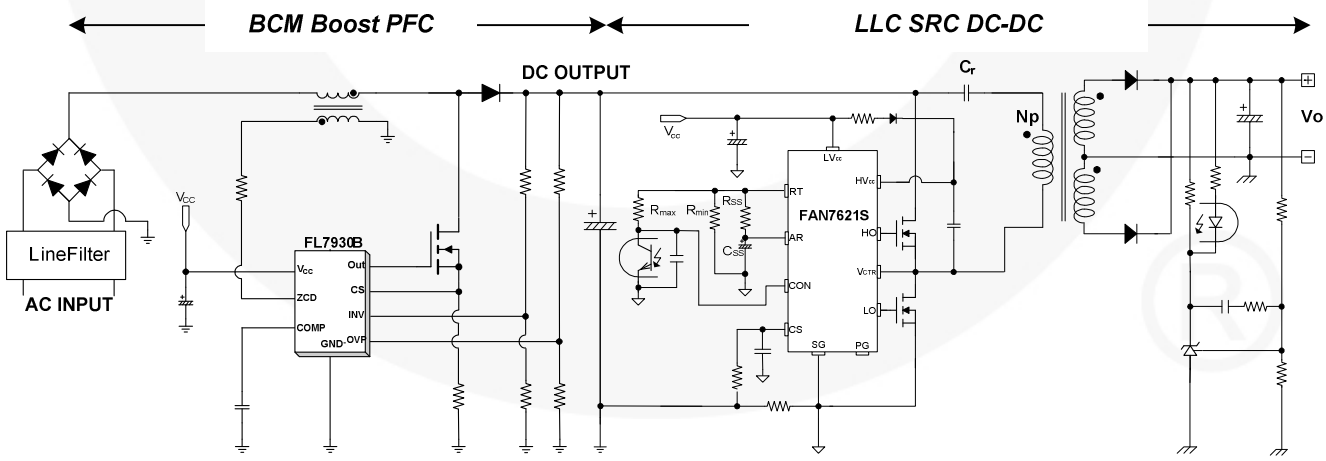


Figure 1. Typical Application Circuit

1. Basic Operation of BCM PFC Pre-Regulator

The most widely used operation modes for the boost converter are Continuous Conduction Mode (CCM) and Boundary Conduction Mode (BCM). These two descriptive names refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. As the names indicate, the inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. Even though the BCM operation has higher RMS current in the inductor and switching devices, it allows better switching condition for the MOSFET and the diode. As shown in Figure 2, the diode reverse recovery is eliminated and a fast-recovery diode is not needed. The MOSFET is also turned on with zero current, which reduces the switching loss.

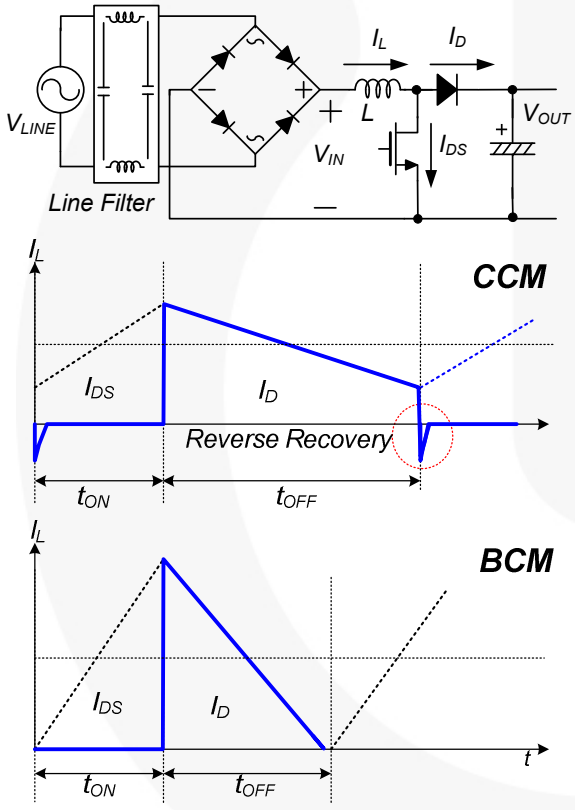


Figure 2. CCM vs. BCM Control

The fundamental idea of BCM PFC is that the inductor current starts from zero in each switching period, as shown in Figure 3. When the power transistor of the boost converter is turned on for a fixed time, the peak inductor current is proportional to the input voltage. Since the current waveform is triangular; the average value in each switching period is proportional to the input voltage. In a sinusoidal input voltage, the input current of the converter follows the input voltage waveform with very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation an ideal candidate for power factor correction.

A side effect of BCM is that the boost converter runs with variable switching frequency that depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input current follows the sinusoidal input voltage waveform, as shown in Figure 3. The lowest frequency occurs at the peak of sinusoidal line voltage.

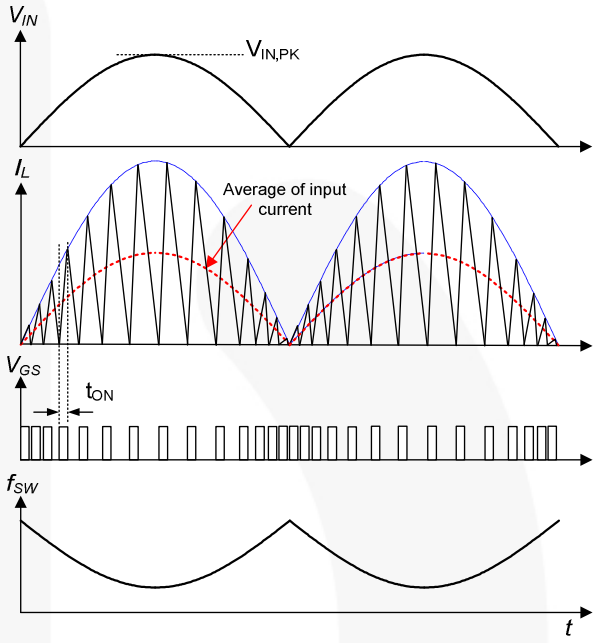


Figure 3. Operation Waveforms of BCM PFC

The voltage-second balance equation for the inductor is:

$$V_{IN}(t)\cdot t_{ON} = \left(V_{OUT} - V_{IN}(t)\right)\cdot t_{OFF} \quad (1)$$

where $V_{IN(t)}$ is the rectified line voltage and V_{OUT} is the output voltage.

The switching frequency of BCM boost PFC converter is:

$$f_{SW} = \frac{1}{t_{ON}+t_{OFF}} = \frac{1}{t_{ON}}\cdot\frac{V_{OUT}-V_{IN}(t)}{V_{OUT}} = \frac{1}{t_{ON}}\cdot\frac{V_{OUT}-V_{IN,PK}\cdot\left|\sin\left(2\pi\cdot f_{LINE}\cdot t\right)\right|}{V_{OUT}} \quad (2)$$

where $V_{IN,PK}$ is the amplitude of the line voltage and f_{LINE} is the line frequency.

Figure 4 shows how the MOSFET on-time and switching frequency change as output power decreases. When the load decreases, as shown in the right side of Figure 4, the peak inductor current diminishes with reduced MOSFET on-time and, therefore, the switching frequency increases. Since this can cause severe switching losses at light-load condition and too-high switching frequency operation may occur at startup, the maximum switching frequency of FL7930B is limited to 300kHz.

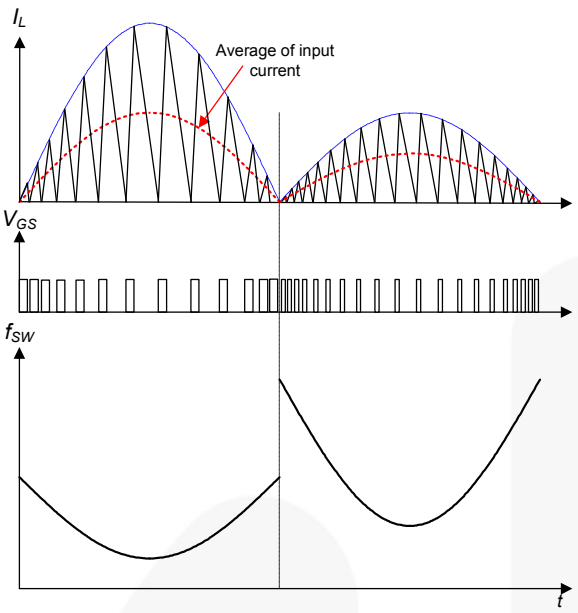


Figure 4. Frequency Variation of BCM PFC

Since the design of the filter and inductor for a BCM PFC converter with variable switching frequency should be at minimum frequency condition, it is worthwhile to examine how the minimum frequency of BCM PFC converter changes with operating conditions.

2. Consideration of LLC Resonant Converter

The attempt to obtain ever-increasing power density in switched-mode power supplies has been limited by the size of passive components. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters; however, switching losses have been an obstacle to high-frequency operation. To reduce switching losses and allow high-frequency operation, resonant switching techniques have been developed. These techniques process power in a sinusoidal manner and the switching devices are softly commutated. Therefore, the switching losses and noise can be dramatically reduced.

Among various kinds of resonant converters, the simplest and most popular is the LC series resonant converter, where the rectifier-load network is placed in series with the LC resonant network, as depicted in Figure 5. In this configuration, the resonant network and the load act as a voltage divider. By changing the frequency of driving voltage V_d, the impedance of the resonant network changes. The input voltage is split between this impedance and the reflected load. Since it is a voltage divider, the DC gain of a LC series resonant converter is always <1. At light-load condition, the impedance of the load is large compared to the impedance of the resonant network; all the input voltage is imposed on the load. This makes it difficult to regulate the output at light load. Theoretically, frequency should be infinite to regulate the output at no load.

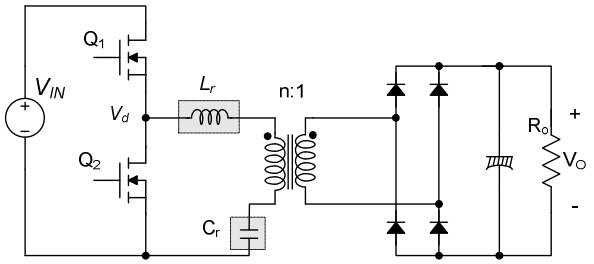


Figure 5. Half-Bridge, LC Series Resonant Converter

To overcome the limitation of series resonant converters, the LLC resonant converter has been proposed. The LLC resonant converter is a modified LC series resonant converter implemented by placing a shunt inductor across the transformer primary winding, as depicted in Figure 6. When this topology was first presented, it did not receive much attention due to the counterintuitive concept that increasing the circulating current in the primary side with a shunt inductor can be beneficial to circuit operation. However, it can be very effective in improving efficiency for high-input voltage applications where the switching loss is more dominant than the conduction loss.

In most practical designs, this shunt inductor is realized using the magnetizing inductance of the transformer. The circuit diagram of LLC resonant converter looks much the same as the LC series resonant converter: the only difference is the value of the magnetizing inductor. While the series resonant converter has a magnetizing inductance larger than the LC series resonant inductor (L_r), the magnetizing inductance in an LLC resonant converter is just 3~8 times L_r, which is usually implemented by introducing an air gap in the transformer.

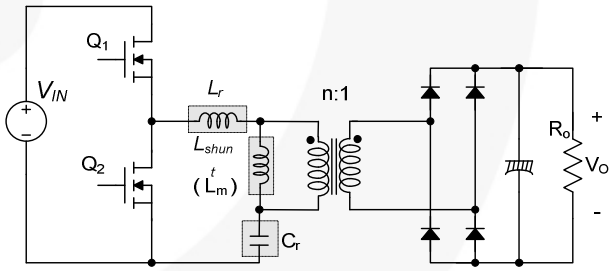


Figure 6. Half-Bridge LLC Resonant Converter

An LLC resonant converter has many advantages over a series resonant converter. It can regulate the output over wide line and load variations with a relatively small variation of switching frequency. It can achieve zero voltage switching (ZVS) over the entire operating range. All essential parasitic elements; including the junction capacitances of all semiconductor devices, the leakage inductance, and magnetizing inductance of the transformer; are utilized to achieve soft switching.

This application note presents design considerations for an LLC resonant half-bridge converter employing Fairchild's FAN7621S. It includes explanation of the LLC resonant converter operation principles, designing the transformer and resonant network, and selecting the components. The step-by-step design procedure, explained with a design example, helps design the LLC resonant converter. 0 shows a simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor. Figure 8 illustrates the typical waveforms of the LLC resonant converter. It is assumed that the operation frequency is the same as the resonance frequency, determined by the resonance between L_r and C_r. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current (I_m) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current (I_p) is the sum of the magnetizing current and the secondary-side current referred to the primary.

In general, the LLC resonant topology consists of the three stages shown in 0; square-wave generator, resonant network, and rectifier network.

- The square-wave generator produces a square-wave voltage, V_d, by driving switches Q_1 and Q_2 alternately with 50% duty cycle for each switch. A small dead time is usually introduced between the consecutive transitions. The square-wave generator stage can be built as a full-bridge or half-bridge type.
- The resonant network consists of a capacitor, leakage inductances, and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Essentially, only sinusoidal current is allowed to flow through the resonant network even though a square-wave voltage is applied. The current (I_p) lags the voltage applied to the resonant network (that is, the fundamental component of the square-wave voltage (V_d) applied to the half-bridge totem pole), which allows the MOSFETs to be turned on with zero voltage. As shown in Figure 8, the MOSFET turns on while the voltage across the MOSFET is zero by flowing current through the anti-parallel diode.
- The rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and a capacitor. The rectifier network can be implemented as a full-wave bridge or a center-tapped configuration with capacitive output filter.

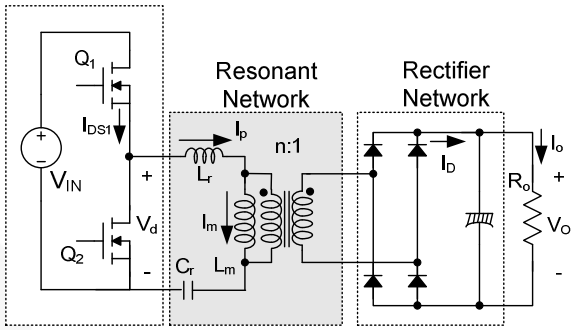


Figure 7. Schematic of Half-Bridge LLC Resonant Converter

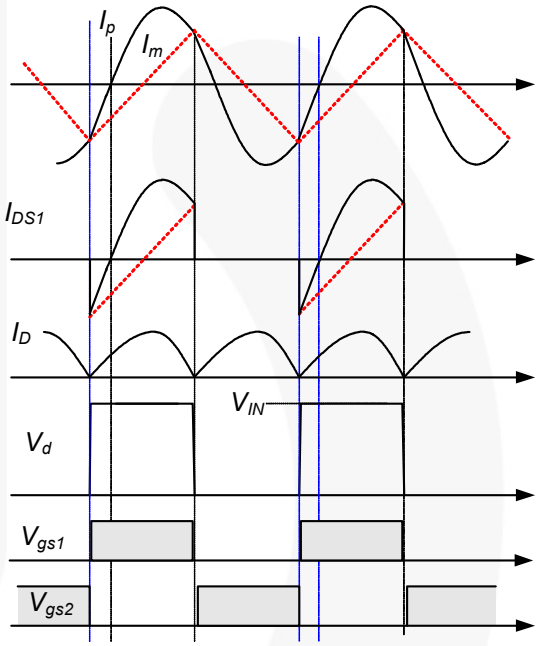


Figure 8. Typical Waveforms of Half-Bridge LLC Resonant Converter

The filtering action of the resonant network allows the use of the fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Figure 9 shows how this equivalent load resistance is derived. The primary-side circuit is replaced by a sinusoidal current source, I_{ac}, and a square wave of voltage, V_{RI}, appears at the input to the rectifier. Since the average of $|I_{ac}|$ is the output current, I_o, I_{ac}, is obtained as:

$$I_{ac} = \frac{\pi \cdot I_o}{2} \sin(\omega t) \quad (3)$$

and V_{RI} is given as:

$$V_{RI} = +V_o \quad if \sin(\omega t) > 0$$
$$V_{RI} = -V_o \quad if \sin(\omega t) < 0 \tag{4}$$

where V_o is the output voltage.

The fundamental component of V_{RI} is given as:

$$V_{RI}^{\ F} = \frac{4V_o}{\pi}\sin(\omega t) \tag{5}$$

Since harmonic components of V_{RI} are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing $V_{RI}^{\ F}$ by I_{ac} as:

$$R_{ac} = \frac{V_{RI}^{\ F}}{I_{ac}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2}R_o \tag{6}$$

Considering the transformer turns ratio ($n=N_p/N_s$), the equivalent load resistance shown in the primary side is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2}R_o \tag{7}$$

By using the equivalent load resistance, the AC equivalent circuit is obtained, as illustrated in Figure 10, where $V_d^{\ F}$ and $V_{RO}^{\ F}$ are the fundamental components of the driving voltage, V_d and reflected output voltage, V_{RO} (nV_{RI}), respectively.

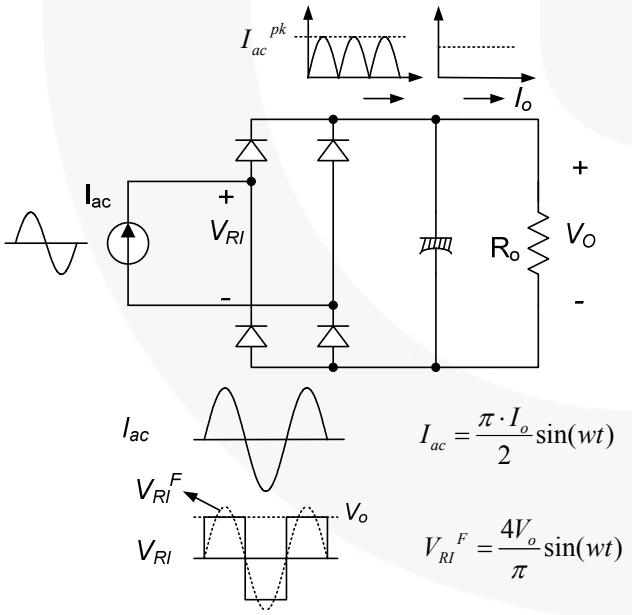


Figure 9. Derivation of Equivalent Load Resistance R_{ac}

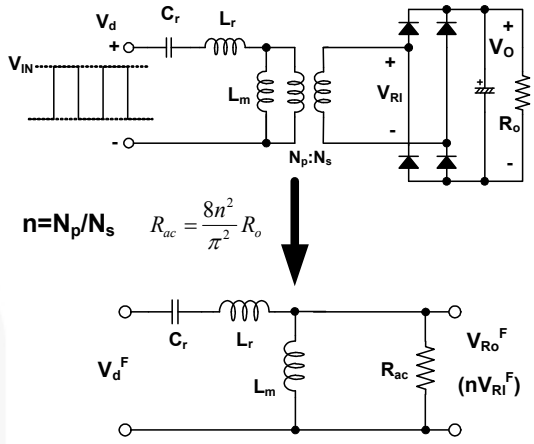


Figure 10. AC Equivalent Circuit for LLC Resonant Converter

With the equivalent load resistance obtained in Equation 7, the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Figure 10, the voltage gain, M, is obtained as:

$$M = \frac{V_{RO}^{\ F}}{V_d^{\ F}} = \frac{n \cdot V_{RI}^{\ F}}{V_d^{\ F}} = \frac{\frac{4n \cdot V_o}{\pi}\sin(\omega t)}{\frac{4}{\pi}\frac{V_{in}}{2}\sin(\omega t)} = \frac{2n \cdot V_o}{V_{in}}$$
$$= \left| \frac{(\frac{\omega}{\omega_o})^2 (m-1)}{(\frac{\omega^2}{\omega_p^{\ 2}} - 1) + j\frac{\omega}{\omega_o}(\frac{\omega^2}{\omega_o^{\ 2}} - 1)(m-1)Q} \right| \tag{8}$$

where:

$$L_p = L_m + L_r \ , \ R_{ac} = \frac{8n^2}{\pi^2}R_o \ , \ m = \frac{L_p}{L_r}$$
$$Q = \sqrt{\frac{L_r}{C_r}}\frac{1}{R_{ac}} \ , \ \omega_o = \frac{1}{\sqrt{L_r C_r}} \ , \ \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

As can be seen in Equation (8), there are two resonant frequencies. One is determined by L_r and C_r, while the other is determined by L_p and C_r.

Equation (8) shows the gain is unity at resonant frequency (ω_o), regardless of the load variation, which is given as:

$$M = \frac{2n \cdot V_o}{V_{in}} = \frac{(m-1)\cdot \omega_p^{\ 2}}{\omega_o^{\ 2} - \omega_p^{\ 2}} = 1 \quad at\ \omega = \omega_o \tag{9}$$

The gain of Equation (8) is plotted in Figure 11 for different Q values with m=3, f_o=100kHz, and f_p=57kHz. As observed in Figure 11, the LLC resonant converter shows gain characteristics that are almost independent of the load when the switching frequency is around the resonant frequency, f_o. This is a distinct advantage of LLC-type resonant converter over the conventional series resonant converter. Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation.

The operating range of the LLC resonant converter is limited by the peak gain (attainable maximum gain), which is indicated with 'Q' in Figure 11. Note that the peak voltage gain does not occur at f_o or f_p. The peak gain frequency, where the peak gain is obtained, exists between f_p and f_o, as shown in Figure 11. As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to f_o and the peak gain drops; the full-load condition should be worst case for the resonant network design.

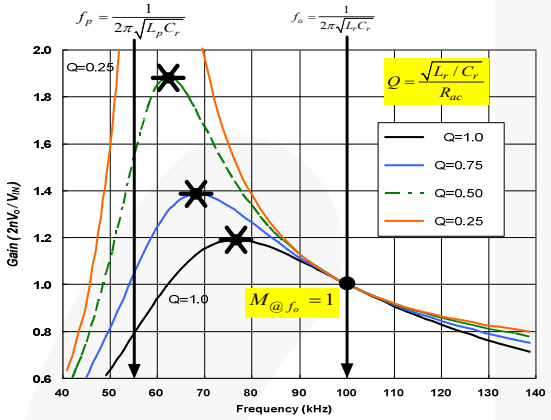


Figure 11. Typical Gain Curves of LLC Resonant Converter (*m*=3)

3. Design Considerations

This design procedure uses the schematic in Figure 1 as a reference. A 150W street lighting application with universal input range is selected as a design example. The design specifications are:

- Line Voltage Range: $85V_A$~$277V_{AC}$ (50Hz)
- Output of Converter: 103V/1.46A (150W)
- PFC Output Voltage: 430V
- Overall Efficiency: 90% (PFC: 95%, LLC: 95%)

3.1 PFC Section

[STEP-1] Define System Specification

- Line Frequency Range ($V_{LINE,MIN}$ and $V_{LINE,MAX}$)
- Line Frequency (f_{LINE})
- Output-Voltage (V_{OUT})
- Output Load Current (I_{OUT})
- Output Power ($P_{OUT} = V_{OUT} \times I_{OUT}$)
- Estimated Efficiency (η)

To calculate the maximum input power, it is necessary to estimate the power conversion efficiency. At universal input range, efficiency is recommended at 0.9; 0.93~0.95 is recommended when input voltage is high. When input voltage is set at the minimum, input current becomes the maximum to deliver the same power compared at high line. Maximum boost inductor current can be detected at the minimum line voltage and at its peak. Inductor current can be divided into two categories; rising current when the MOSFET is on and output diode current when the MOSFET is off, as shown in Figure 12.

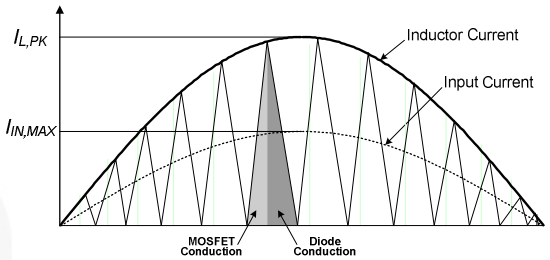


Figure 12. Inductor and Input Current

Because switching frequency is much higher than line frequency, input current can be assumed to be constant during a switching period, as shown in Figure 133.

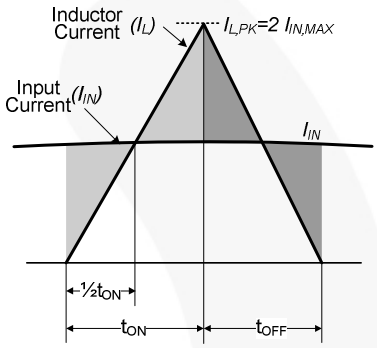


Figure 13. Inductor and Input Current

With the estimated efficiency, Figure 12 and Figure 13, inductor current peak *($I_{L,PK}$)*, maximum input current *($I_{IN,MAX}$)*, and input Root Mean Square (RMS) current *($I_{IN,MAXRMS}$)* are given as:

$$I_{L,PK} = \frac{4 \cdot P_{OUT}}{\eta \cdot \sqrt{2} \cdot V_{LINE,MIN}} \ [A] \quad (10)$$

$$I_{IN,MAX} = I_{L,PK} / 2 \ [A] \quad (11)$$

$$I_{IN,MAXRMS} = I_{IN,MAX} / \sqrt{2} \ [A] \quad (12)$$

(Design Example) Input voltage range is universal input, output load is 465mA, and estimated efficiency is selected as 0.9.

$V_{LINE,MIN} = 85V_{AC}$, $V_{LINE,MAX} = 277V_{AC}$

$f_{LINE} = 50Hz$

$V_{OUT} = 430V$, $I_{OUT} = 465mA$

$\eta = 0.9$

$$I_{L,PK} = \frac{4 \cdot P_{OUT}}{\eta \cdot \sqrt{2} \cdot V_{LINE,MIN}} = \frac{4 \cdot 430V \cdot 0.465A}{0.9 \cdot \sqrt{2} \cdot 85} = 7.392A$$

$$I_{IN,MAX} = \frac{I_{L,PK}}{2} = \frac{7.392A}{2} = 3.696A$$

$$I_{IN,MAXRMS} = \frac{I_{IN,MAX}}{\sqrt{2}} = \frac{3.696A}{\sqrt{2}} = 2.613A$$

[STEP-2] Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. The minimum switching frequency must be higher than the maximum audible frequency band of 20kHz. Minimum frequency near 20kHz can decrease switching loss with the cost of increased inductor size and line filter size. Too-high minimum frequency may increase the switching loss and make the system respond to noise. Selecting in the range of about 30~60kHz is a common choice; 40~50kHz is recommended with FL7930B.

The minimum switching frequency may appear at minimum input voltage or maximum input voltage, depending on the output voltage level. When PFC output voltage is less than 430V, minimum switching appears at the maximum input voltage *(see Fairchild application note AN-6086)*. Inductance is obtained using the minimum switching frequency:

$$L = \frac{\eta \cdot \left(\sqrt{2}V_{LINE}\right)^2}{4 \cdot f_{SW,MIN} \cdot P_{OUT} \cdot \left(1 + \frac{\sqrt{2}V_{LINE}}{V_{OUT} - \sqrt{2}V_{LINE}}\right)} \ [H] \quad (13)$$

where L is boost inductance and $f_{SW,MIN}$ is the minimum switching frequency.

The maximum on-time needed to carry peak inductor current is calculated as:

$$t_{ON,MAX} = L \cdot \frac{I_{L,PK}}{\sqrt{2} \cdot V_{LINE,MIN}} \ [s] \quad (14)$$

Once inductance and the maximum inductor current are calculated, the turn number of the boost inductor should be determined considering the core saturation. The minimum number of turns is given as:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L[\mu H]}{A_e[mm^2] \cdot \Delta B} \ [Turns] \quad (15)$$

where A_e is the cross-sectional area of the core and ΔB is the maximum flux swing of the core in Tesla. ΔB should be set below the saturation flux density.

Figure 14 shows the typical B-H characteristics of a ferrite core from TDK (PC45). Since the saturation flux density (Δ*B*) decreases as the temperature increases, the high-temperature characteristics should be considered.

RMS inductor current *($I_{L,RMS}$)* and current density of the coil *($I_{L,DENSITY}$)* can be given as:

$$I_{L,RMS} = \frac{I_{L,PK}}{\sqrt{6}} \ [A] \quad (16)$$

$$I_{L,DENSITY} = \frac{I_{L,RMS}}{\pi \cdot \left(d_{wire}/2\right)^2 \cdot N_{wire}} \ [A/mm^2] \quad (17)$$

where d_{WIRE} is the diameter of winding wire and N_{WIRE} is the number of strands of winding wire.

When selecting wire diameter and strands; current density, window area *(A_W, refer to Figure 14)* of the selected core, and fill factor need to be considered. The winding sequence of the boost inductor is relatively simple compared to a DC-DC converter, so fill factor can be assumed about 0.2~0.3.

Layers cause the skin effect and proximity effect in the coil, so real current density may be higher than expected.

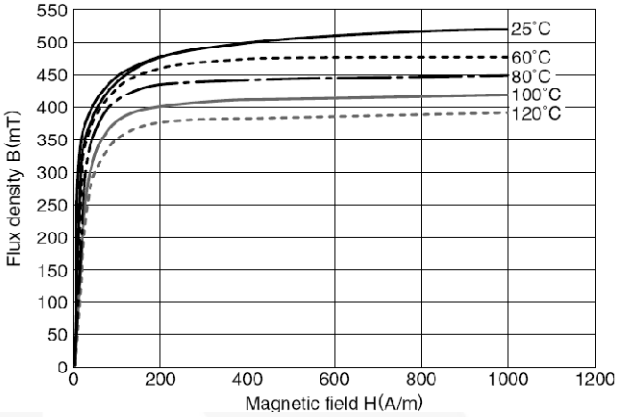


Figure 14. Typical B-H Curves of Ferrite Core

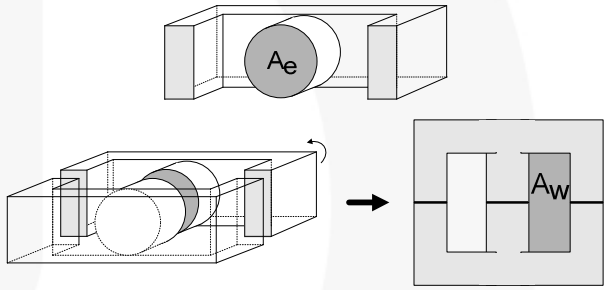


Figure 15. A_e and A_W

(Design Example) Since the output voltage is 430V, the minimum frequency occurs at high-line ($277V_{AC}$) and full-load condition. Assuming the efficiency is 90% and selecting the minimum frequency as 50kHz, the inductor value is obtained as:

$$L = \frac{\eta \cdot \left(\sqrt{2}V_{LINE}\right)^2}{4 \cdot f_{SW,MIN} \cdot P_{OUT} \cdot \left(1 + \frac{\sqrt{2}V_{LINE}}{V_{OUT} - \sqrt{2}V_{LINE}}\right)}$$

$$= \frac{0.9 \cdot \left(\sqrt{2} \times 277\right)^2}{4 \cdot 50 \cdot 10^3 \cdot 200 \cdot \left(1 + \frac{\sqrt{2} \cdot 277}{430 - \sqrt{2} \cdot 277}\right)} = 307.2[\mu H]$$

Assuming EER3019N core (PL-7, A_e=137mm^2) is used and setting ΔB as 0.3T, the primary winding should be:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L[\mu H]}{A_e[mm^2] \cdot \Delta B} = \frac{7.392 \cdot 307}{137 \cdot 0.3} = 55[T]$$

The number of turns (N_{BOOST}) of the boost inductor is determined as 55 turns.

When 0.10mm diameter and 50-strand wire is used, RMS current of inductor coil and current density are:

$$I_{L,RMS} = \frac{I_{L,PK}}{\sqrt{6}} = \frac{7.392}{\sqrt{6}} = 3.017\,[A]$$

$$I_{L,DENSITY} = \frac{I_{L,RMS}}{\pi \cdot \left(d_{wire}/2\right)^2 \cdot N_{wire}} = \frac{3.017}{\pi \cdot (0.1/2)^2 \cdot 50} = 7.68\,[A/mm^2]$$

[STEP-3] Inductor Auxiliary Winding Design

Figure 16 shows the application circuit of the nearby ZCD pin from auxiliary winding.

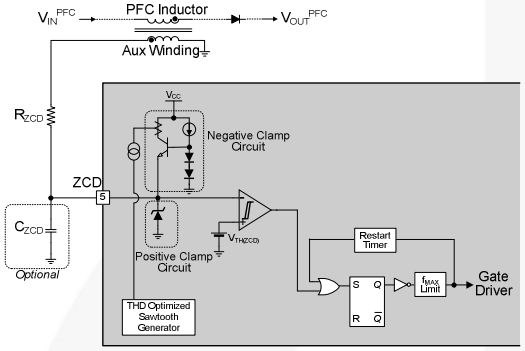


Figure 16. Application Circuit of ZCD Pin

The first role of ZCD winding is detecting the zero-current point of the boost inductor. Once the boost inductor current becomes zero, the effective capacitance *(C_{eff})* at the MOSFET drain pin and the boost inductor resonate together. To minimize the constant turn-on time deterioration and turn-on loss, the gate is turned on again when the drain source voltage of the MOSFET *(V_{DS})* reaches the valley point shown in Figure 17. When input voltage is lower than half of the boosted output voltage, Zero Voltage Switching (ZVS) is possible if MOSFET turn-on is triggered at valley point.

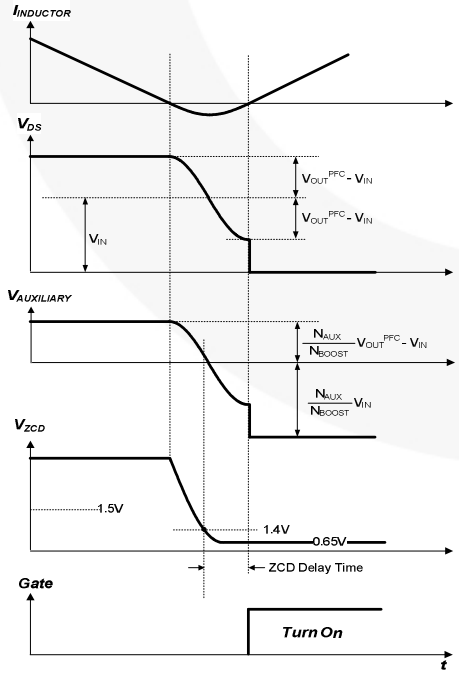


Figure 17. ZCD Detection Waveforms

Auxiliary winding must give enough energy to trigger ZCD threshold to detect zero current. Minimum auxiliary winding turns are given as:

$$N_{AUX} \geq \frac{1.5V \cdot N_{BOOST}}{V_{OUT} - \sqrt{2}V_{LINE,MAX}}\ [Turns] \quad (18)$$

where 1.5V is the positive threshold of the ZCD pin.

To guarantee stable operation, it is recommended to add 2~3 turns to the auxiliary winding turns calculated in Equation (18). However, too many auxiliary winding turns raise the negative clamping loss at high line and positive clamping loss at low line.

(Design Example) 55 turns are selected as boost inductor turns and auxiliary winding turns are calculated as:

$$N_{AUX} \geq \frac{1.5V \cdot N_{BOOST}}{V_{OUT} - \sqrt{2}V_{LINE,MAX}} = \frac{1.5 \cdot 55}{430 - \sqrt{2} \cdot 277} = 2.15[Turns]$$

Choice should be around 4~5 turns after adding 2~3 turns.

[STEP-4] ZCD Circuit Design

If a transition time when $V_{AUXILIARY}$ drops from 1.4V to 0V is ignored from Figure 17, the necessary additional delay by the external resistor and capacitor is one quarter of the resonant period. The time constant made by ZCD resistor and capacitor should be the same as one quarter of the resonant period:

$$R_{ZCD} \cdot C_{ZCD} = \frac{2\pi\sqrt{C_{eff} \cdot L}}{4} \quad (19)$$

where C_{eff} is the effective capacitance at the MOSFET drain pin; C_{ZCD} is the external capacitance at the ZCD pin; and R_{ZCD} is the external resistance at the ZCD pin.

The second role of R_{ZCD} is the current limit of the internal negative clamp circuit when auxiliary voltage drops to negative due to MOSFET turn on. ZCD voltage is clamped 0.65V and minimum R_{ZCD} can be given as:

$$R_{ZCD} \geq \frac{\left(\frac{N_{AUX}}{N_{BOOST}}\sqrt{2}V_{LINE,MAX} - 0.65V\right)}{3mA}\ [\Omega] \quad (20)$$

where 3mA is the clamping capability of the ZCD pin.

The calculation result of Equation (20) is normally higher than 15kΩ. If 20kΩ is assumed as R_{ZCD}, calculated C_{ZCD} from Equation (19) is around 10pF when the other components are assumed as conventional values used in the field. Because most IC pins have several pF of parasitic capacitance, C_{ZCD} can be eliminated when R_{ZCD} is higher than 30kΩ. However, a small capacitor would be helpful when auxiliary winding suffers from operating noise.

The PFC control loop has two conflicting goals: output voltage regulation and making the input current shape the same as input voltage. If the control loop reacts to regulate output voltage smoothly, as shown in Figure 18, control

voltage varies widely with the input voltage variation. Input current acts to the control loop and sinusoidal input current shape cannot be attained. This is the reason control response of most PFC topologies is very slow and turn-on time over AC period is kept constant. This is also the reason output voltage ripple is made by input and output power relationship, not by control-loop performance.

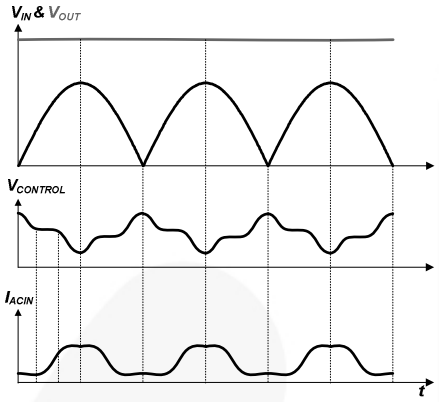


Figure 18. Input Current Deterioration by Fast Control

If on-time is controlled constantly over one AC period, the inductor current peak follows AC input voltage shape and achieves good power factor. Off-time is basically inductor current reset time due to Boundary Mode and is determined by the input and output voltage difference. When input voltage is at its peak, the voltage difference between input and output voltage is small and long turn-off time is necessary. When input voltage is near zero, turn-off time is short, as shown in Figure 19 and Figure 20. Though inductor current drops to zero, the minor delay is explained above. The delay can be assumed as fixed when AC is at line peak and zero. Near AC line peak, the inductor current decreasing slope is slow and inductor current slope is also slow during the ZCD delay. The amount of negative current is not much higher than the inductor current peak. Near the AC line zero, inductor current decreasing slope is very high and the amount of negative current is higher than positive inductor current peak because input voltage is almost zero.

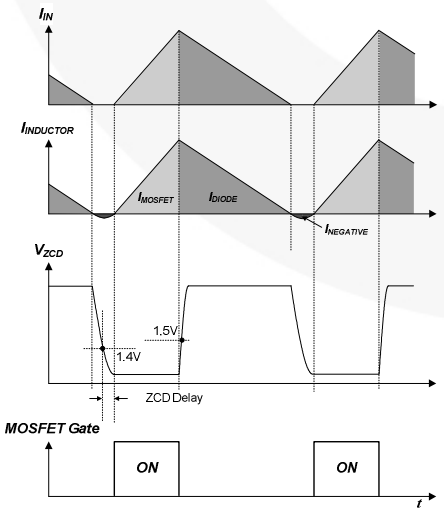


Figure 19. Inductor Current at AC Voltage Peak

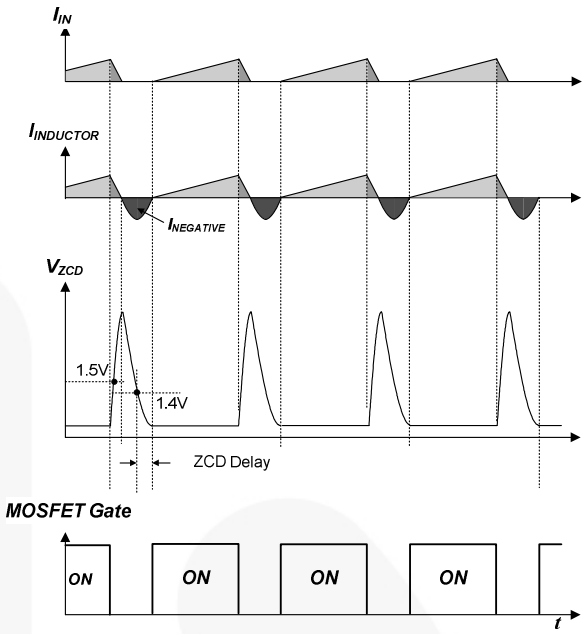


Figure 20. Inductor Current at AC Voltage Zero

Negative inductor current creates zero-current distortion and degrades the power factor. Improve this by extending turn-on time at the AC line input near the zero cross.

Negative auxiliary winding voltage, when the MOSFET is turned on, is linearly proportional to the input voltage. Sourcing current generated by the internal negative clamping circuit is also proportional to sinusoidal input voltage. That current is detected internally and added to the internal sawtooth generator, as shown in Figure 21.

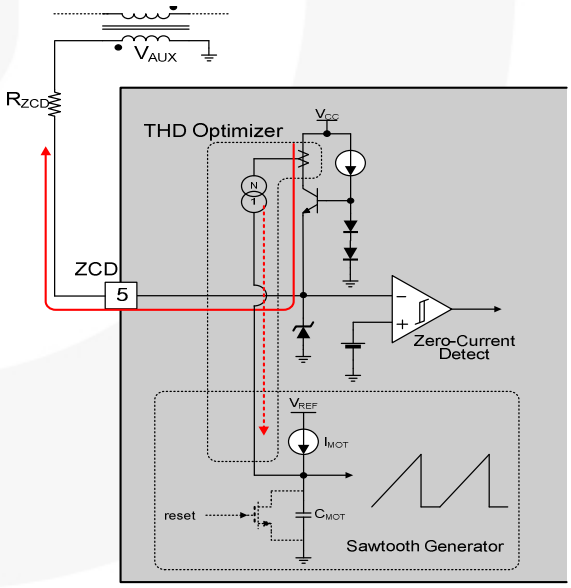


Figure 21. ZCD Current and Sawtooth Generator

When the AC input voltage is almost zero, no negative current is generated from inside, but sourcing current when input voltage is high is used to raise the sawtooth generator slope and turn-on time is shorter. As a result, turn-on time when AC voltage is zero is longer compared to AC voltage, in peaks shown in Figure 22.

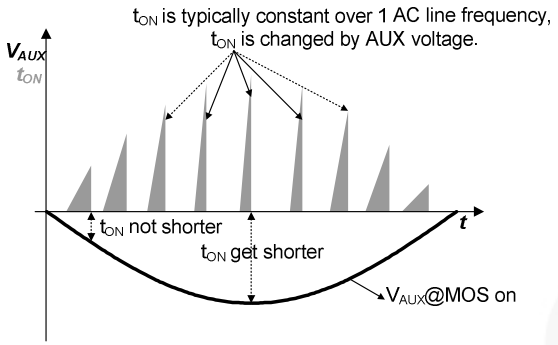


Figure 22. THD Improvement

The current that comes from the ZCD pin, when auxiliary voltage is negative, depends on R_{ZCD}. The second role of R_{ZCD} is also related to improving the Total Harmonic Distortion (THD).

The third role of R_{ZCD} is making the maximum turn-on time adjustment. Depending on sourcing current from the ZCD pin, the maximum on-time varies as in Figure 23.

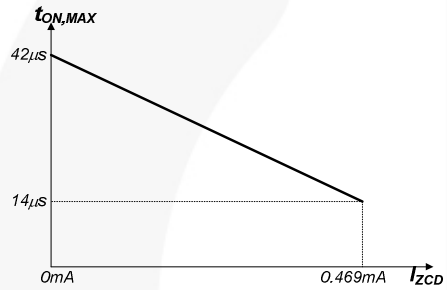


Figure 23. Maximum On-Time Variation vs. I_{ZCD}

With the aid of I_{ZCD}, an internal sawtooth generator slope is changed and turn-on time varies as shown in Figure 24.

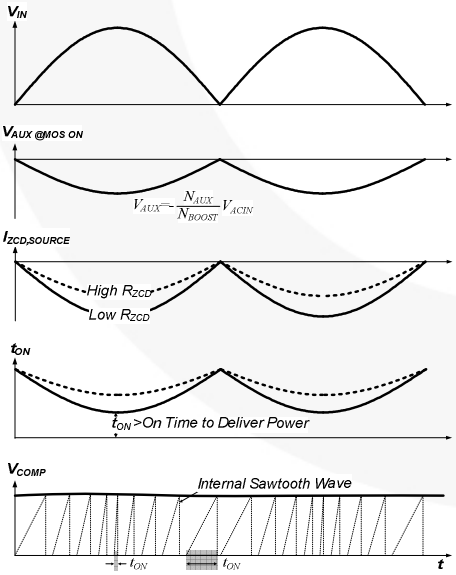


Figure 24. Internal Sawtooth Wave Slope Variation

R_{ZCD} also influences control range. Because FL7930B doesn't detect input voltage, voltage-mode control value is determined by the turn-on time to deliver the needed current to boost output voltage. When input voltage increases, control voltage decreases rapidly. For example, if input voltage doubles, control voltage drops to one quarter. Making control voltage maximum when input voltage is low and at full load is necessary to use the whole control range for the rest of the input voltage conditions. Matching maximum turn-on time needed at low line is calculated in Equation (14) and turn-on time adjustment by R_{ZCD} guarantees use of the full control range. R_{ZCD} for control range optimization is obtained as:

$$R_{ZCD} \geq \frac{28\mu s}{t_{ON,MAX1} - t_{ON,MAX}} \cdot \frac{\sqrt{2} \cdot V_{LINE,MIN} \cdot N_{AUX}}{0.469mA \cdot N_{BOOST}} \ [\Omega] \quad (21)$$

where:
$t_{ON,MAX}$ is calculated by Equation (14);
$t_{ON,MAX1}$ is maximum on-time programming 1;
N_{BOOST} is the winding turns of boost inductor; and
N_{AUX} is the auxiliary winding turns.

R_{ZCD} calculated by Equation (20) is normally lower than the value calculated in Equation (21). To guarantee the needed turn on-time for the boost inductor to deliver rated power, the R_{ZCD} from Equation (20) is normally not suitable. R_{ZCD} should be higher than the result of Equation (21) when output voltage drops as a result of low line voltage.

When input voltage is high and load is light, not much input current is needed and control voltage of V_{COMP} touches switching stop level, such as if FL7930B is 1V. However, in some applications, a PFC block is needed to operate normally at light load. To compensate control range correctly, input voltage sensing is necessary, such as with Fairchild's interleaved PFC controller FAN9612, or special care on sawtooth generator is necessary. To guarantee enough control range at high line, clamping output voltage lower than rated on the minimum input condition can help.

(Design Example) Minimum R_{ZCD} for clamping capability is calculated as:

$$R_{ZCD} \geq \frac{\left(\frac{N_{AUX}}{N_{BOOST}}\sqrt{2}V_{LINE,MAX} - 0.65V\right)}{3mA}$$

$$= \frac{\left(\frac{5}{34}\sqrt{2} \cdot 277 - 0.65V\right)}{3mA} = 18.9k\Omega$$

Minimum R_{ZCD} for control range is calculated as:

$$R_{ZCD} \geq \frac{28\mu s}{t_{ON,MAX1} - t_{ON,MAX}} \cdot \frac{\sqrt{2} \cdot V_{LINE,MIN} \cdot N_{AUX}}{0.469mA \cdot N_{BOOST}}$$

$$= \frac{28\mu s}{42\mu s - 10.9\mu s} \cdot \frac{\sqrt{2} \cdot 85 \cdot 5}{0.469mA \cdot 55} = 20.97k\Omega$$

A choice close to the value calculated by the control range is recommended. 39kΩ is chosen in this case.

[STEP-5] Output Capacitor Selection

The output voltage ripple should be considered when selecting the output capacitor. Figure 25 shows the line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

$$C_{OUT} \geq \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot \Delta V_{OUT,RIPPLE}} \ [f] \quad (22)$$

where $V_{OUT,RIPPLE}$ is the peak-to-peak output voltage ripple specification.

The output voltage ripple caused by the ESR of the electrolytic capacitor is not as serious as other power converters because output voltage is high and load current is small. Since too much ripple on the output voltage may cause premature OVP during normal operation, the peak-to-peak ripple specification should be smaller than 15% of the nominal output voltage.

The hold-up time should also be considered when determining the output capacitor as:

$$C_{OUT} \geq \frac{2 \cdot P_{OUT} \cdot t_{HOLD}}{\left(V_{OUT} - 0.5 \cdot \Delta V_{OUT,RIPPLE}\right)^2 - V_{OUT,MIN}^2} \ [f] \quad (23)$$

where t_{HOLD} is the required hold-up time and $V_{OUT,MIN}$ is the minimum output voltage during hold-up time.

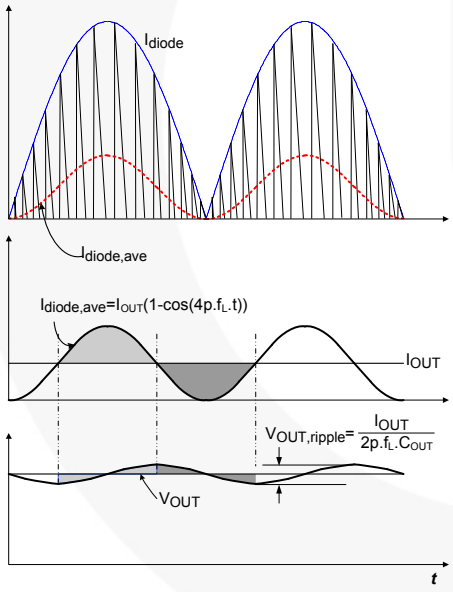


Figure 25. Output Voltage Ripple

The voltage rating of capacitor can be obtained as:

$$V_{ST,COUT} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT} \ [V] \quad (24)$$

where $V_{OVP,MAX}$ and V_{REF} are the maximum tolerance specifications of over-voltage protection triggering voltage and reference voltage at error amplifier, respectively.

(Design Example) With the ripple specification of $8V_{p-p}$, the capacitor should be:

$$C_O \geq \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot \Delta V_{OUT,ripple}} = \frac{0.465}{2\pi \cdot 50 \cdot 8} = 185 [\mu F]$$

Since minimum allowable output voltage during one cycle line (20ms) drop-outs is 330V, the capacitor should be:

$$C_O \geq \frac{2 \times P_{OUT} \cdot t_{HOLD}}{\left(V_{OUT} - 0.5 \cdot \Delta V_{OUT,ripple}\right)^2 - V_{OUT,MIN}^2}$$

$$= \frac{2 \cdot 200 \cdot 20 \times 10^{-3}}{\left(430 - 0.5 \cdot 8\right)^2 - 330^2} = 110 [\mu F]$$

To meet both conditions, the output capacitor must be larger than 140µF. A 240µF capacitor is selected for the output capacitor.

The voltage stress of selected capacitor is calculated as:

$$V_{ST,COUT} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT} = \frac{2.730}{2.500} \cdot 430 = 469.5 [V]$$

[STEP-6] MOSFET and DIODE Selection

Selecting the MOSFET and diode requires extensive knowledge and calculation regarding loss mechanisms and gets more complicated if proper selection of a heatsink is added. Sometimes the loss calculation itself is based on assumptions that may be far from reality. Refer to industry resources regarding these topics. This note shows the voltage rating and switching loss calculations based on a linear approximation.

The voltage stress of the MOSFET is obtained as:

$$V_{ST,Q} = \frac{V_{OVP,MAX}}{V_{REF}} \cdot V_{OUT} + V_{DROP,DOUT} \ [V] \quad (25)$$

where $V_{DROP,DOUT}$ is the maximum forward-voltage drop of output diode.

After the MOSFET is turned off, the output diode turns on and a large output electrolytic capacitance is shown at the drain pin; thus a drain voltage clamping circuit that is necessary on other topologies is not necessary in PFC. During the turn-off transient, boost inductor current changes the path from MOSFET to output diode. Before the output diode turns on; a minor voltage peak can be shown at drain pin, which is proportional to MOSFET turn-off speed.

MOSFET loss can be divided into three parts: conduction loss, turn-off loss, and discharge loss. Boundary mode guarantees Zero Current Switching (ZCS) of the MOSFET when turned on, so turn-on loss is negligible.

The MOSFET RMS current and conduction loss are obtained as:

$$I_{Q,RMS} = I_{L,PK} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot V_{LINE}}{9\pi \cdot V_{OUT}}} \ [A] \quad (26)$$

$$P_{Q,CON} = \left(I_{Q,RMS}\right)^2 \cdot R_{DS,ON} \ [W] \quad (27)$$

where $I_{Q,RMS}$ is the RMS value of MOSFET current, $P_{Q,CON}$ is the conduction loss caused by MOSFET current, and $R_{DS,ON}$ is the ON resistance of the MOSFET.

On resistance is described as "static on resistance" and varies depending on junction temperature. That variation information is normally supplied as a graph in the datasheet and may vary by manufacturer. When calculating conduction loss, generally multiply three by the $R_{DS,ON}$ for more accurate estimation.

The precise turn-off loss calculation is difficult because of the nonlinear characteristics of MOSFET turn-off. When piecewise linear current and voltage of MOSFET during turn-off and inductive load are assumed, MOSFET turn-off loss is obtained as:

$$P_{Q,SWOFF}=\frac{1}{2}\cdot V_{OUT}\cdot I_L\cdot t_{OFF}\cdot f_{SW}\ [W] \quad (28)$$

where t_{OFF} is the turn-off time and f_{SW} is the switching frequency.

Boundary Mode PFC inductor current and switching frequency vary at every switching moment. RMS inductor current and average switching frequency over one AC period can be used instead of instantaneous values.

Individual loss portions are changed according to the input voltage; maximum conduction loss appears at low line because of high input current; and maximum switching off loss appears at high line because of the high switching frequency. The resulting loss is always lower than the summation of the two losses calculated above.

Capacitive discharge loss made by effective capacitance shown at drain and source, which includes MOSFET C_{OSS}, an externally added capacitor to reduce dv/dt and parasitic capacitance shown at drain pin, is also dissipated at MOSFET. That loss is calculated as:

$$P_{Q,DISCHG}=\frac{1}{2}(C_{OSS}+C_{EXT}+C_{PAR})\cdot V_{OUT}^2\cdot f_{SW}\ [W] \quad (29)$$

where:
C_{OSS} is the output capacitance of MOSFET;
C_{EXT} is an externally added capacitance at drain and source of MOSFET; and
C_{PAR} is the parasitic capacitance shown at drain pin.

Because the C_{OSS} is a function of the drain and source voltage, it is necessary to refer to graph data showing the relationship between C_{OSS} and voltage.

Estimate the total power dissipation of MOSFET as the sum of three losses:

$$P_Q=P_{Q,CON}+P_{Q,SWOFF}+P_{Q,DISCHG}[W] \quad (30)$$

Diode voltage stress is the same as the output capacitor stress calculated in Equation (24).

The average diode current and power loss are obtained as:

$$I_{DOUT,AVE}=\frac{I_{OUT}}{\eta}\ [A] \quad (31)$$

$$P_{DOUT}=V_{DROP,DOUT}\cdot I_{DOUT,AVE}\ [W] \quad (32)$$

where $V_{DROP,DOUT}$ is the forward voltage drop of diode.

(Design Example) Internal reference at the feedback pin is 2.5V and maximum tolerance of OVP trigger voltage is 2.730V. If Fairchild's FDPF17N60NT MOSFET and FFPF08H60S diode are selected, $V_{D,FOR}$ is 2.1V at 8A, 25°C, maximum $R_{DS,ON}$ is 0.34Ω at drain current is 17A, and maximum C_{OSS} is 32pF at drain-source voltage is 480V.

$$V_{ST,Q}=\frac{V_{OVP,MAX}}{V_{REF}}\cdot V_{OUT}+V_{DROP,DIODE}$$
$$=\frac{2.73}{2.50}\cdot 430+2.1=471.6\ [V]$$

$$P_{Q,CON}=\left(I_{L,PK}\cdot\sqrt{\frac{1}{6}-\frac{4\sqrt{2}\cdot V_{LINE}}{9\pi\cdot V_{OUT}}}\right)^2\cdot(R_{DS,ON})$$
$$=\left(7.392\cdot\sqrt{\frac{1}{6}-\frac{4\sqrt{2}\cdot 85}{9\pi\cdot 430}}\right)^2\cdot(0.34)=2.23[W]$$

$$P_{Q,SWOFF}=\frac{1}{2}\cdot V_{OUT}\cdot I_L\cdot t_{OFF}\cdot f_{SW}$$
$$=\frac{1}{2}\cdot 430\cdot 2.613\cdot 50ns\cdot(50k/0.8)=1.755\ [W]$$

$$P_{Q,DISCHG}=\frac{1}{2}\cdot(C_{OSS}+C_{EXT}+C_{PAR})\cdot V_{OUT}^2\cdot f_{SW}$$
$$=\frac{1}{2}\cdot 32p\cdot 430^2\cdot(50k/0.8)=0.184[W]$$

Diode average current and forward-voltage drop loss as:

$$I_{DOUT,AVE}=\frac{I_{OUT}}{\eta}=\frac{0.5}{0.9}=0.56[A]$$

$$P_{DOUT,LOSS}=V_{DOUT,FOR}\cdot I_{DOUT,AVE}=2.1\cdot 0.56=1.46[W]$$

[STEP-7] Determine Current-Sense Resistor

It is typical to set pulse-by-pulse current limit level a little higher than the maximum inductor current calculated by Equation (10). For 10% margin, the current-sensing resistor is selected as:

$$R_{CS}=\frac{V_{CS,LIM}}{I_{L,PK}\cdot 1.1}\ [\Omega] \quad (33)$$

Once resistance is calculated, its power loss at low line is calculated as:

$$P_{RCS}=I_{Q,RMS}^2\cdot R_{CS}\ [W] \quad (34)$$

Power rating of the sensing resistor is recommended a twice the power rating calculated in Equation (34).

(Design Example) Maximum inductor current is 4.889A and sensing resistor is calculated as:

$$R_{CS} = \frac{V_{CS,LIM}}{I_{ind}^{pk} \cdot 1.1} = \frac{0.8}{7.392 \cdot 1.1} = 0.098[\Omega]$$

Choosing 0.1Ω as R_{CS}, power loss is calculated as:

$$P_{RCS,LOSS} = I_{Q,RMS}^2 \cdot R_{CS} = 2.436^2 \cdot 0.098 = 0.58[W]$$

Recommended power rating of sensing resistor is 1.19W.

[STEP-8] Design Compensation Network

The boost PFC power stage can be modeled as shown in Figure 26 MOSFET and diode can be changed to loss-free resistor model and then modeled as a voltage-controlled current source supplying RC network.

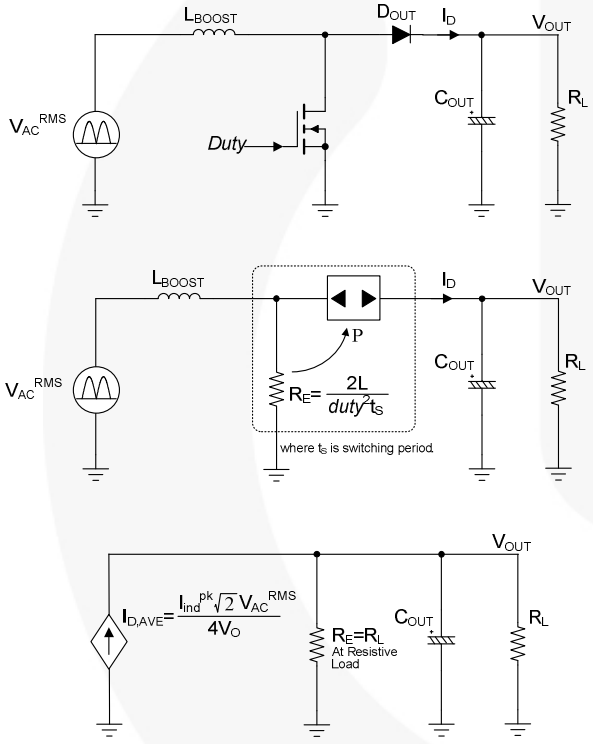


Figure 26. Small Signal Modeling of the Power Stage

By averaging the diode current during the half line cycle, the low-frequency behavior of the voltage controlled current source of Figure 26 is obtained as:

$$I_{DOUT,AVE} = K_{SAW} \cdot \frac{\sqrt{2}V_{LINE}}{4V_{OUT}} \cdot \frac{\sqrt{2}V_{LINE}}{L} \ [A] \quad (35)$$

where:
L is the boost inductance;
V_{OUT} is the output voltage; and
K_{SAW} is the internal gain of sawtooth generator (that of FL7930B is 8.496×10^{-6}).

Then the low-frequency, small-signal, control-to-output transfer function is obtained as:

$$\frac{\hat{v}_{OUT}}{\hat{v}_{COMP}} = K_{SAW} \cdot \frac{(V_{LINE})^2 R_L}{4V_{OUT} \cdot L} \cdot \frac{1}{1 + \frac{s}{2\pi f_p}} \quad (36)$$

where $f_p = \frac{2}{2\pi \cdot R_L C_{OUT}}$ and R_L is the output load resistance in a given load condition.

Figure 27 and Figure 28 show the variation of the control-to-output transfer function for different input voltages and different loads. Since DC gain and crossover frequency increase as input voltage increases, and DC gain increases as load decreases, high input voltage and light load is the worst condition for feedback loop design.

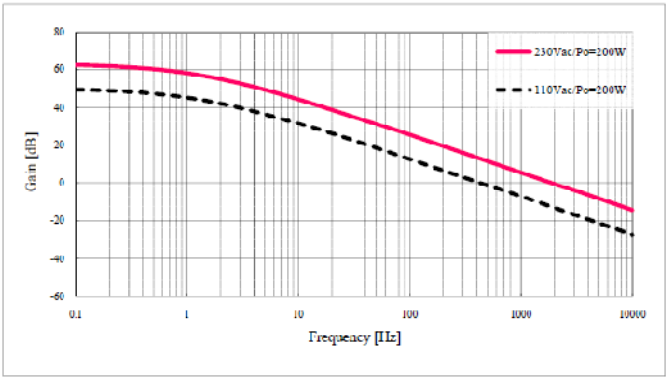


Figure 27. Control-to-Output Transfer Function for Different Input Voltages

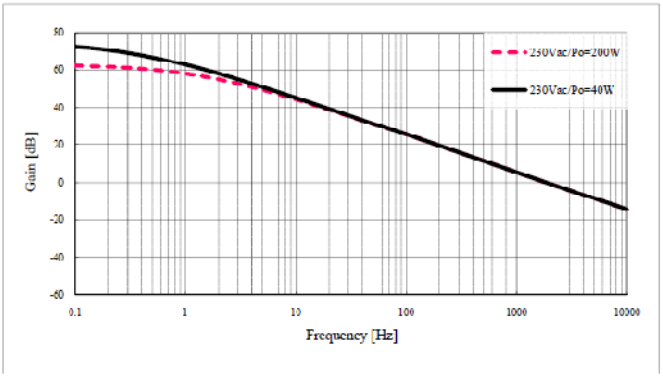


Figure 28. Control-to-Output Transfer Function for Different Loads

Proportional and integration (PI) control with high-frequency pole is typically used for compensation, as shown in Figure 29. The compensation zero (f_{CZ}) introduces phase boost, while the high-frequency compensation pole (f_{CP}) attenuates the switching ripple.

The transfer function of the compensation network is obtained as:

$$\frac{\hat{v}_{COMP}}{\hat{v}_{OUT}} = \frac{2\pi f_I}{s} \cdot \frac{1 + \frac{s}{2\pi f_{CZ}}}{1 + \frac{s}{2\pi f_{CP}}} \quad (37)$$

$$f_I = \frac{2.5}{V_{OUT}} \cdot \frac{115\mu mho}{2\pi \cdot (C_{COMP,LF} + C_{COMP,HF})}$$

where $f_{CZ} = \frac{1}{2\pi \cdot R_{COMP} \cdot C_{COMP,LF}}$

$$f_{CP} = \frac{1}{2\pi \cdot R_{COMP} \cdot \left(\frac{C_{COMP,LF} \cdot C_{COMP,HF}}{C_{COMP,LF} + C_{COMP,HF}} \right)}$$

If $C_{COMP,LF}$ is much larger than $C_{COMP,HF}$, f_I and f_{CP} can be simplified as:

$$f_I \cong \frac{2.5}{V_{OUT}} \cdot \frac{115\mu mho}{2\pi \cdot C_{COMP,LF}} \ [Hz]$$
$$f_{CP} \cong \frac{1}{2\pi \cdot R_{COMP} \cdot C_{COMP,HF}} \ [Hz] \quad (38)$$

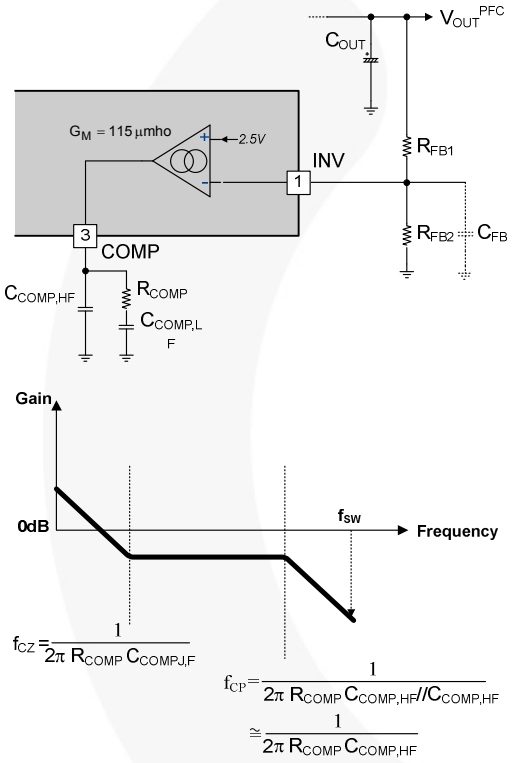


Figure 29. Compensation Network

The feedback resistor is chosen to scale down the output voltage to meet the internal reference voltage:

$$\frac{R_{FB1}}{R_{FB1} + R_{FB2}} \cdot V_{OUT} = 2.5V \quad (39)$$

Typically, high R_{FB1} is used to reduce power consumption and C_{FB} can be added to raise the noise immunity. The maximum C_{FB} currently used is several nano farads. Adding a capacitor at the feedback loop introduces a pole as:

$$f_{FP} = \frac{1}{2\pi \cdot (R_{FB1} // R_{FB2}) \cdot C_{FB}} \cong \frac{1}{2\pi \cdot R_{FB2} \cdot C_{FB}} \ [Hz] \quad (40)$$

where $(R_{FB1} // R_{FB2}) = \frac{R_{FB1} \cdot R_{FB2}}{R_{FB1} + R_{FB2}}$.

Though R_{FB1} is high, pole frequency made by the synthesized total resistance and several nano farads is several kilo hertz and rarely affects control-loop response

The procedure to design the feedback loop is:

a. Determine the crossover frequency (f_C) around 1/10 ~ 1/5 of line frequency. Since the control-to-output transfer function of the power stage has -20dB/dec slope and -90° phase at the crossover frequency; it is required to place the zero of the compensation network (f_{CZ}) around the crossover frequency so 45° phase margin is obtained. The capacitor $C_{COMP,LF}$ is determined as:

$$C_{COMP,LF} \cong \frac{K_{SAW}(V_{LINE})^2 \ 2.5 \cdot 115\mu mho}{2 \cdot V_{OUT}^2 \cdot L \cdot C_{OUT}(2\pi f_C)^2} [f] \quad (41)$$

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

$$R_{COMP} = \frac{1}{2\pi \cdot f_C \cdot C_{COMP,LF}} \ [\Omega] \quad (42)$$

b. Place this compensator high-frequency pole (f_{CP}) at least a decade higher than f_C to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter for noise to be effectively attenuated. The capacitor $C_{COMP,HF}$ is determined as:

$$C_{COMP,HF} = \frac{1}{2\pi \cdot f_{CP} \cdot R_{COMP}} \ [\Omega] \quad (43)$$

(Design Example) If R_{FB1} is 11.7MΩ, then R_{FB2} is:

$$R_{FB2} = \frac{2.5V}{V_{OUT} - 2.5V} R_{FB1} = \frac{2.5}{430 - 2.5} 11.7 \times 10^6 = 68k\Omega$$

Choosing the crossover frequency (control bandwidth) at 15Hz, $C_{COMP,LF}$ is obtained as:

$$C_{COMP,\,LF} \cong \frac{K_{SAW} (V_{LINE})^2 2.5 \cdot 115 \mu mho}{2 \cdot V_{OUT}{}^2 \cdot L \cdot C_{OUT} (2\pi f_C)^2}$$

$$= \frac{8.496 \times 10^{-6} (230)^2 2.5 \cdot 115 \times 10^{-6}}{2 \cdot 430^2 \cdot 199 \times 10^{-6} \cdot 240 \times 10^{-6} (2\pi 15)^2} = 823nF$$

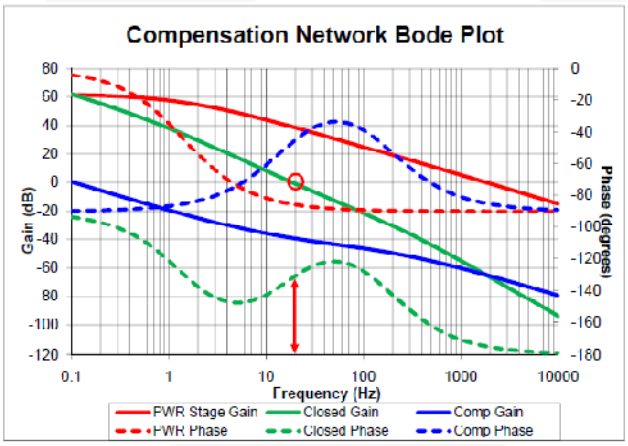
Actual $C_{COMP,LF}$ is determined as 1000nF since it is the closest value among the off-the-shelf capacitors. R_{COMP} is obtained as:

$$R_{COMP} = \frac{1}{2\pi \cdot f_C \cdot C_{COMP,LF}} = \frac{1}{2\pi \cdot 15 \cdot 823 \times 10^{-9}} = 12.8k\Omega$$

Selecting the high-frequency pole as 150Hz, $C_{COMP,HF}$ is obtained as:

$$C_{COMP,HF} = \frac{1}{2\pi \cdot f_{CP} \cdot R_{COMP}} = \frac{1}{2\pi \cdot 150 \cdot 12.8 \times 10^3} = 82nF$$

These components result in a control loop with a bandwidth of 19.5Hz and phase margin of 45.6°. The actual bandwidth is a little larger than the asymptotic design.



[STEP-9] Line Filter Capacitor Selection

It is typical to use small bypass capacitors across the bridge rectifier output stage to filter the switching current ripple, as shown in Figure 30. Since the impedance of the line filter inductor at line frequency is negligible compared to the impedance of the capacitors, the line frequency behavior of the line filter stage can be modeled, as shown in Figure 30. Even though the bypass capacitors absorb switching ripple current, they also generate circulating capacitor current, which leads the line voltage by 90°, as shown in Figure 31. The circulating current through the capacitor is added to the load current and generates displacement between line voltage and current.

The displacement angle is given by:

$$\theta = tan^{-1}\left(\frac{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE} \cdot C_{EQ}}{P_{OUT}}\right) \quad (44)$$

where C_{EQ} is the equivalent capacitance that appears across the AC line ($C_{EQ}=C_{F1}+C_{F2}+C_{HF}$).

The resultant displacement factor is:

$$DF = cos(\theta) \quad (45)$$

Since the displacement factor is related to power factor, the capacitors in the line filter stage should be selected carefully. With a given minimum displacement factor (DF_{MIN}) at full-load condition, the allowable effective input capacitance is obtained as:

$$C_{EA} < \frac{P_{OUT}}{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE}} \cdot tan\left(cos^{-1}(DF_{MN})\right)[F] \quad (46)$$

One way to determine if the input capacitor is too high or PFC control routine has problems is to check Power Factor (PF) and Total Harmonic Distortion (THD). PF is the degree to which input energy is effectively transferred to the load by the multiplication of displacement factor and THD that is input current shape deterioration ratio. PFC control loop rarely has no relation to displacement factor and input capacitor rarely has no impact on the input current shape. If PF is low (high is preferable), but THD is quite good (low is preferable), it can be concluded that input capacitance is too high and PFC controller is fine.

(Design Example) Assuming the minimum displacement factor at full load is 0.98, the equivalent input capacitance is obtained as:

$$C_{EA} < \frac{P_{OUT}}{\eta \cdot (V_{LINE})^2 \cdot 2\pi \cdot f_{LINE}} \cdot tan\left(cos^{-1}(DF_{MN})\right)$$

$$< \frac{200}{0.9 \cdot (277)^2 \cdot 2\pi \cdot 50} \cdot tan\left(cos^{-1}(0.98)\right) = 1.6\mu F$$

Thus, the sum of the capacitors on the input side should be smaller than 2.0μF.

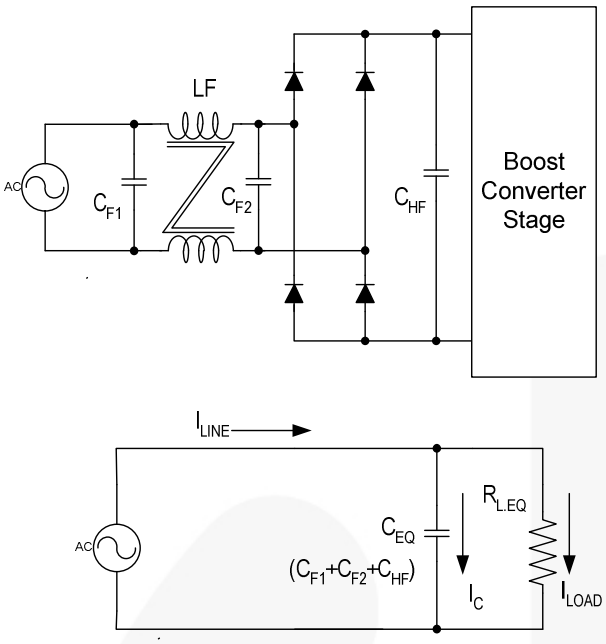


Figure 30. Equivalent Circuit of Line Filter Stage

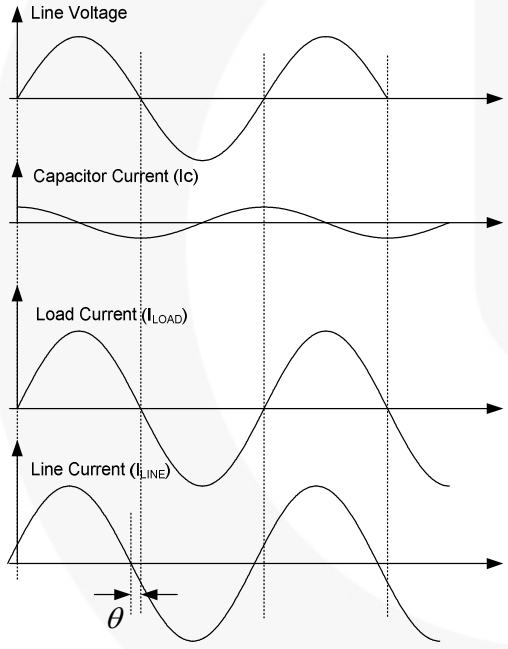


Figure 31. Line Current Displacement

3.2 LLC SRC Section

In this section, a design procedure is presented using the schematic in Figure 1 as a reference. An integrated transformer with center tap, secondary side is used and input is supplied from Power Factor Correction (PFC) pre-regulator. A DC-DC converter with 150W/103V output is selected as a design example. The design specifications are:

- Nominal input voltage: $400V_{DC}$ (output of PFC stage)
- Output: 103V/1.46A (150W)
- Hold-up time requirement: 30ms (50Hz line freq.)
- DC link capacitor of PFC output: 240μF

[STEP-10] Define System Specifications

Estimated Efficiency (E_{ff}): The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. If no reference data is available, use E_{ff} = 0.88~0.92 for low-voltage output applications and E_{ff} = 0.92~0.96 for high-voltage output applications. With the estimated efficiency, the maximum input power is given as:

$$P_{in} = \frac{P_o}{E_{ff}} \tag{47}$$

Input Voltage Range (V_{in}^{min} and V_{in}^{max}): The maximum input voltage would be the nominal PFC output voltage as:

$$V_{in}^{max} = V_{O.PFC} \tag{48}$$

Even though the input voltage is regulated as constant by PFC pre-regulator, it drops during the hold-up time. The minimum input voltage considering the hold-up time requirement is given as:

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}} \tag{49}$$

where $V_{O.PFC}$ is the nominal PFC output voltage, T_{HU} is a hold-up time, and C_{DL} is the DC link bulk capacitor.

(Design Example) Assuming the efficiency is 92%,

$$P_{in} = \frac{P_o}{E_{ff}} = \frac{150}{0.92} = 163W$$

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}}$$

$$= \sqrt{430^2 - \frac{2 \cdot 163 \cdot 30 \times 10^{-3}}{240 \times 10^{-6}}} = 379V$$

[STEP-11] Determine Maximum and Minimum Voltage Gains of the Resonant Network

As discussed in the previous section, it is typical to operate the LLC resonant converter around the resonant frequency (f_o) to minimize switching frequency variation. Since the input of the LLC resonant converter is supplied from PFC output voltage, the converter should be designed to operate at f_o for the nominal PFC output voltage.

As observed in Equation (9), the gain at f_o is a function of m ($m=L_p/L_r$). The gain at f_o is determined by choosing that value of m. While a higher peak gain can be obtained with a small m value, too small m value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set m to be 3~7, which results in a voltage gain of 1.1~1.2 at the resonant frequency (f_o).

With the chosen m value, the voltage gain for the nominal PFC output voltage is obtained as:

$$M^{\min} = \sqrt{\frac{m}{m-1}}_{@f=f_o} \quad (50)$$

which would be the minimum gain because the nominal PFC output voltage is the maximum input voltage (V_{in}^{max}).

The maximum voltage gain is given as:

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min} \quad (51)$$

(Design Example) The ratio (m) between L_p and L_r is chosen as 5. The minimum and maximum gains are obtained as:

$$M^{\min} = \frac{V_{RO}}{V_{in}^{\max}/\sqrt{2}} = \sqrt{\frac{m}{m-1}} = \sqrt{\frac{5}{5-1}} = 1.12$$

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} m^{\min} = \frac{400}{341} \cdot 1.12 = 1.31$$

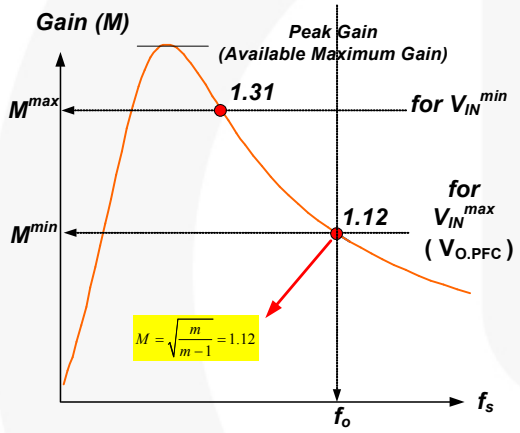


Figure 32. Maximum Gain / Minimum Gain

[STEP-12] Determine the Transformer Turns Ratio ($n=N_p/N_s$)

With the minimum gain (M^{min}) obtained in STEP-11, the transformer turns ratio is given as:

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_o + V_F)} \cdot M^{\min} \quad (52)$$

where V_F is the secondary-side rectifier diode voltage drop.

(Design Example) assuming V_F is 0.9V:

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_O + V_F)} \cdot M_{\min} = \frac{430}{2(103+0.9)} \cdot 1.12 = 2.06$$

[STEP-13] Calculate Equivalent Load Resistance

With the transformer turns ratio obtained from Equation (52), the equivalent load resistance is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} \quad (53)$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{(V_o + V_F)^2}{P_o} = \frac{8 \cdot 1.93^2 \cdot 103.9^2}{\pi^2 \cdot 150} = 217\Omega$$

[STEP-14] Design the Resonant Network

With the m value chosen in STEP-11, read the proper Q value from the peak gain curves in Figure 33 that allows enough peak gain. Considering the load transient and stable zero-voltage-switching (ZVS) operation, 10~20% margin should be introduced on the maximum gain when determining the peak gain. Once the Q value is determined, the resonant parameters are obtained as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} \quad (54)$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} \quad (55)$$

$$L_p = m \cdot L_r \quad (56)$$

(Design Example)

As calculated in STEP-11, the maximum voltage gain (M^{max}) for the minimum input voltage (V_{in}^{min}) is 1.31. With 15% margin, a peak gain of 1.51 is required. m has been chosen as 5 in STEP-11 and Q is obtained as 0.38 from the peak gain curves in Figure 33. By selecting the resonant frequency as 100kHz, the resonant components are determined as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} = \frac{1}{2\pi \cdot 0.38 \cdot 100 \times 10^3 \cdot 217} = 19nF$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} = \frac{1}{(2\pi \times 100 \times 10^3)^2 \cdot 19 \times 10^{-9}} = 133\mu H$$

$$L_p = m \cdot L_r = 665\mu H$$

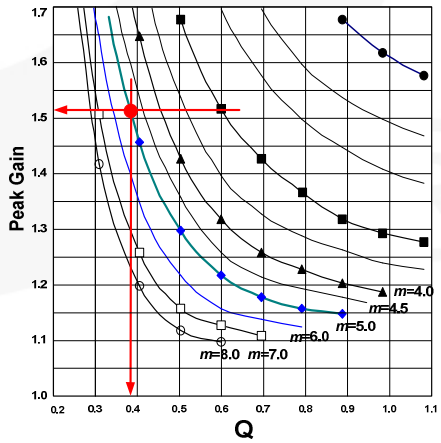


Figure 33. Resonant Network Design Using the Peak Gain (Attainable Maximum Gain) Curve for *m*=5

[STEP-15] Design the Transformer

The worst case for the transformer design is the minimum switching frequency condition, which occurs at the minimum input voltage and full-load condition. To obtain the minimum switching frequency, plot the gain curve using gain Equation (8) and read the minimum switching frequency. The minimum number of turns for the transformer primary-side is obtained as:

$$N_p^{\min} = \frac{n(V_o + V_F)}{2 f_s^{\min} \cdot M_V \cdot \Delta B \cdot A_e} \quad (57)$$

where A_e is the cross-sectional area of the transformer core in m^2 and ΔB is the maximum flux density swing in Tesla, as shown in Figure 34. If there is no reference data, use ΔB =0.3~0.4 T.

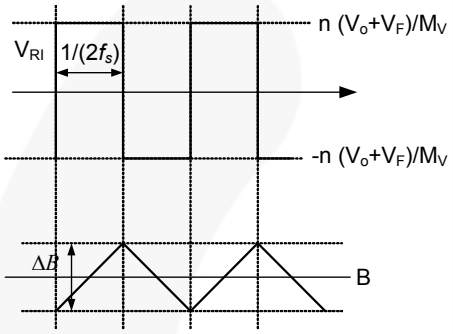


Figure 34. Flux Density Swing

Choose the proper number of turns for the secondary side that results in primary-side turns larger than $N_p^{\min}$ as:

$$N_p = n \cdot N_s > N_p^{\min} \quad (58)$$

(Design Example) EER3542 core (A_e=107mm^2) is selected for the transformer. From the gain curve of Figure 35, the minimum switching frequency is obtained as 82KHz. The minimum primary-side turns of the transformer is given as:

$$N_p^{\min} = \frac{n(V_o + V_F)}{2 f_s^{\min} \Delta B \cdot 1.11 \cdot A_e}$$

$$= \frac{1.93 \times 103.9}{2 \times 82 \times 10^3 \cdot 0.4 \cdot 1.11 \cdot 107 \times 10^{-6}} = 26\,turns$$

Choose N_s so that the resultant N_p is larger than $N_p^{\min}$:

$$N_p = n \cdot N_s = 1.93 \times 14 = 27 < N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 15 = 29 < N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 16 = 31 > N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 17 = 33 > N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 18 = 35 > N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 19 = 37 > N_p^{\min}$$

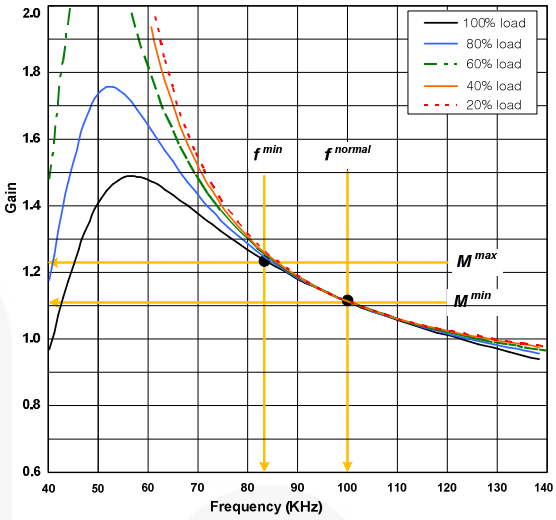


Figure 35. Gain Curve

[STEP-16] Transformer Construction

Parameters L_p and L_r of the transformer were determined in STEP-14. L_p and L_r can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively. Since LLC converter design requires a relatively large L_r, a sectional bobbin is typically used, as shown in Figure 36, to obtain the desired L_r value. For a sectional bobbin, the number of turns and winding configuration are the major factors determining the value of L_r, while the gap length of the core does not affect L_r much. L_p can be controlled by adjusting the gap length. Table 1. shows measured L_p and L_r values with different gap lengths. A gap length of 0.05mm obtains values for L_p and L_r closest to the designed parameters.

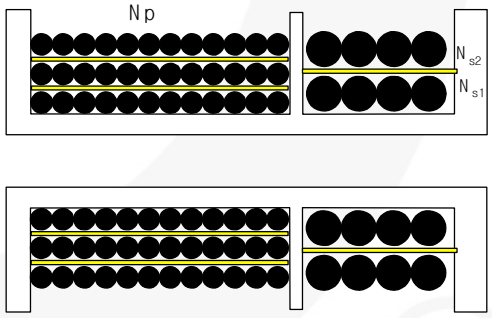


Figure 36. Sectional Bobbin

Table 1. Measured L_p and L_r with Different Gap Lengths

Gap Length	L_p	L_r
0.0mm	2,295μH	123μH
0.05mm	943μH	122μH
0.10mm	630μH	118μH
0.15mm	488μH	117μH
0.20mm	419μH	115μH
0.25mm	366μH	114μH

(Design Example)

Final Resonant Network Design

Even though the integrated transformer approach in LLC resonant converter design can implement the magnetic components in a single core and save one magnetic component, the value of L_r is not easy to control in real transformer design. Resonant network design sometimes requires iteration with a resultant L_r value after the transformer is built. The resonant capacitor value is also changed since it should be selected among off-the-shelf capacitors. The final resonant network design is summarized in Table 2. and the new gain curves are shown in Figure 37.

Table 2. Final Resonant Network Design Parameters

Parameters	Initial Design	Final Design
L_p	665μH	691μH
L_r	133H	122μH
C_r	19nF	22nF
f_o	100kHz	96kHz
m	5	5
Q	0.38	0.3
M at f_o	1.12	1.12
Minimum Frequency	75kHz	74.4kHz

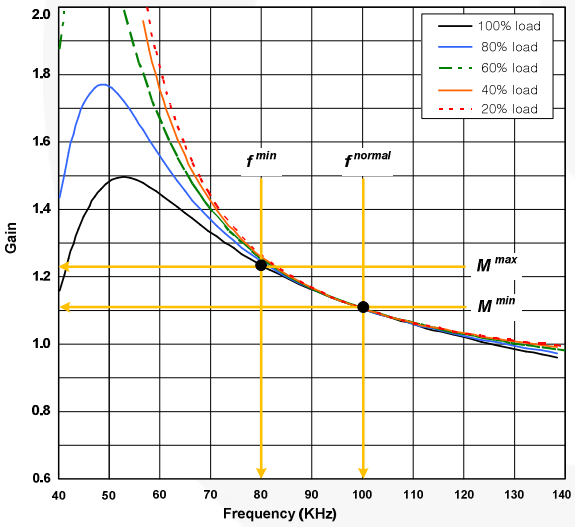


Figure 37. Gain Curve of the Final Resonant Network Design

[STEP-17] Select the Resonant Capacitor

When choosing the resonant capacitor, the current rating should be considered because a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor is given as:

$$I_{C_r}^{RMS} \cong \frac{1}{E_{ff}} \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n}\right]^2 + \left[\frac{n(V_o + V_F)}{4\sqrt{2} f_o M_V (L_p - L_r)}\right]^2} \quad (59)$$

The nominal voltage of the resonant capacitor in normal operation is given as:

$$V_{C_r}^{nom} \cong \frac{V_{in}^{\max}}{2} + \frac{\sqrt{2} \cdot I_{Cr}^{RMS}}{2 \cdot \pi \cdot f_o \cdot C_r} \quad (60)$$

However, the resonant capacitor voltage increases higher than this at overload condition or load transient. Actual capacitor selection should be based on the Over-Current Protection (OCP) trip point. With the OCP current, I_{OCP}, the maximum resonant capacitor voltage is obtained as:

$$V_{C_r}^{nom} \cong \frac{V_{in}^{\max}}{2} + \frac{I_{OCP}}{2 \cdot \pi \cdot f_o \cdot C_r} \quad (61)$$

(Design Example)

$$I_{C_r}^{RMS} \cong \frac{1}{E_{ff}} \sqrt{\left[\frac{\pi I_O}{2\sqrt{2}n}\right]^2 + \left[\frac{n(V_o + V_F)}{4\sqrt{2} f_o M_v (L_p - L_r)}\right]^2}$$

$$= \frac{1}{0.92} \sqrt{\left[\frac{\pi \cdot 1.4}{2\sqrt{2} \cdot 1.93}\right]^2 + \left[\frac{1.93(103 + 0.9)}{4\sqrt{2} \cdot 96 \times 10^3 \cdot 1.12 \cdot 500 \times 10^{-6}}\right]^2}$$

$= 1.12A$

The peak current in the primary side in normal operation is:

$$I_{C_r}^{peak} = \sqrt{2} \cdot I_{C_r}^{rms} = 1.58A$$

OCP level is set to 2.5A with 50% margin on I_{Cr}^{peak}:

$$V_{C_r}^{nom} \cong \frac{V_{in}^{\max}}{2} + \frac{\sqrt{2} \cdot I_{C_r}^{RMS}}{2 \cdot \pi \cdot f_o \cdot C_r}$$

$$= \frac{430}{2} + \frac{\sqrt{2} \cdot 1.18}{2 \cdot \pi \cdot 96 \times 10^3 \cdot 22 \times 10^{-9}} = 340V$$

$$V_{C_r}^{\max} \cong \frac{V_{in}^{\max}}{2} + \frac{I_{OCP}}{2 \cdot \pi \cdot f_o \cdot C_r}$$

$$= \frac{430}{2} + \frac{2.5}{2 \cdot \pi \cdot 96 \times 10^3 \cdot 22 \times 10^{-9}} = 403.3V$$

A 630V rated low-ESR film capacitor is selected for the resonant capacitor.

[STEP-18] Rectifier Network Design

When the center tap winding is used in the transformer secondary side, the diode voltage stress is twice of the output voltage expressed as:

$$V_D = 2(V_o + V_F) \quad (62)$$

The RMS value of the current flowing through each rectifier diode is given as:

$$I_D^{RMS} = \frac{\pi}{4} I_o \quad (63)$$

Meanwhile, the ripple current flowing through output capacitor is given as:

$$I_{Co}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o \quad (64)$$

The voltage ripple of the output capacitor is:

$$\Delta V_o = \frac{\pi}{2} I_o \cdot R_C \quad (65)$$

where R_C is the effective series resistance (ESR) of the output capacitor and the power dissipation is the output capacitor is:

$$P_{Loss.Co} = (I_{Co}^{RMS})^2 \cdot R_C \quad (66)$$

(Design Example) The voltage stress and current stress of the rectifier diode are:

$$V_D = 2(V_o + V_F) = 2(103 + 0.9) = 207.8V$$

$$I_D^{RMS} = \frac{\pi}{4} I_o = 1.14A$$

The 600V/8A ultra-fast recovery diode is selected for the rectifier, considering the voltage overshoot caused by the stray inductance.

The RMS current of the output capacitor is:

$$I_{C_o}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o = 0.584A$$

When two electrolytic capacitors with ESR of 100mΩ are used in parallel, the output voltage ripple is given as:

$$\Delta V_o = \frac{\pi}{2} I_o \cdot R_C = \frac{\pi}{2} \cdot 1.46 \cdot (\frac{0.1}{2}) = 0.114V$$

The loss in electrolytic capacitors is:

$$P_{Loss,C_o} = (I_{C_o}^{RMS})^2 \cdot R_C = 0.584^2 \cdot 0.05 = 0.017W$$

[STEP-19] Control Circuit Configuration

Figure 38 shows the typical circuit configuration for the RT pin of FAN7621S, where the opto-coupler transistor is connected to the RT pin to control the switching frequency. The minimum switching frequency occurs when the opto-coupler transistor is fully tuned off, which is given as:

$$f_{\min} = \frac{5.2k\Omega}{R_{\min}} \times 100(kHz) \quad (67)$$

Assuming the saturation voltage of opto-coupler transistor is 0.2V, the maximum switching frequency is determined as:

$$f_{\max} = (\frac{5.2k\Omega}{R_{\min}} + \frac{4.68k\Omega}{R_{\max}}) \times 100(kHz) \quad (68)$$

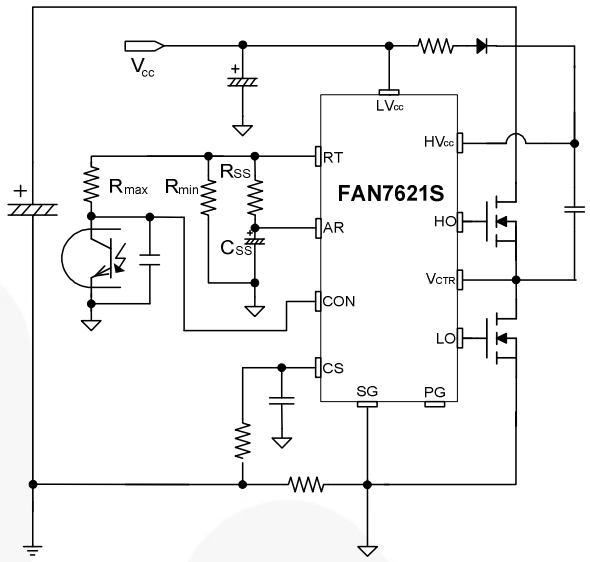


Figure 38. Typical Circuit Configuration for RT Pin

Soft-start prevents excessive inrush current and overshoot of output voltage during startup, increases the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is reversely proportional to the switching frequency, soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established, as illustrated in Figure 39. The soft-start circuit is made by connecting RC series network on the RT pin as shown in Figure 38. FAN7621S also has an internal soft-start for 3ms to reduce the current overshoot during the initial cycles, which adds 40KHz to the initial frequency of the external soft-start circuit, as shown in Figure 39. The actual initial frequency of the soft-start is given as:

$$f^{ISS} = (\frac{5.2k\Omega}{R_{\min}} + \frac{5.2k\Omega}{R_{SS}}) \times 100 + 40\ (kHz) \quad (69)$$

It is typical to set the initial frequency of soft-start (f^{ISS}) at 2~3 times of the resonant frequency (f_o).

The soft-start time is determined by the RC time constant:

$$t_{SS} = 3 \sim 4(R_{SS} \bullet C_{SS}) \quad (70)$$

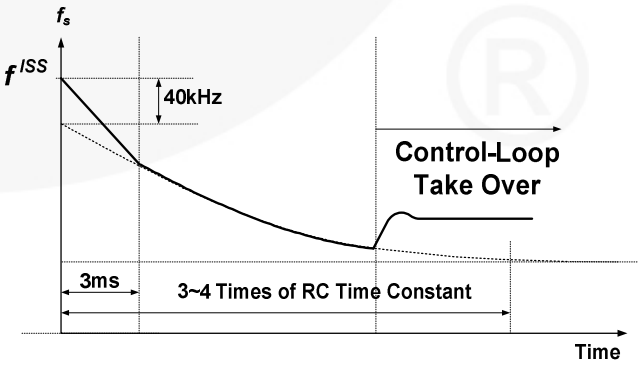


Figure 39. Frequency Sweep of the Soft-Start

(Design Example) The minimum frequency is 75kHz in STEP-15. R_{min} is determined as:

$$R_{\min} = \frac{100KHz}{f_{\min}} \times 5.2K\Omega = 6.93K\Omega$$

Considering the output voltage overshoot during transient (10%) and the controllability of the feedback loop, the maximum frequency is set as 140kHz. R_{max} is determined as:

$$R_{\max} = \frac{4.68K\Omega}{(\frac{f_o \times 1.40}{100KHz} - \frac{5.2K\Omega}{R_{\min}})}$$

$$= \frac{4.68K\Omega}{(\frac{96KHz \times 1.40}{100KHz} - \frac{5.2K\Omega}{6.93K\Omega})} = 7.88K\Omega$$

Setting the initial frequency of soft-start as 250kHz (2.5 times of the resonant frequency), the soft-start resistor R_{SS} is given as:

$$R_{SS} = \frac{5.2K\Omega}{(\frac{f_{ISS} - 40KHz}{100KHz} - \frac{5.2K\Omega}{R_{\min}})}$$

$$= \frac{5.2K\Omega}{(\frac{250KHz - 40KHz}{100KHz} - \frac{5.2K\Omega}{6.93K\Omega})} = 3.85K\Omega$$

[STEP-20] Current Sensing and Protection

FAN7621S senses low-side MOSFET drain current as a negative voltage, as shown in Figure 40. and Figure 41. Half-wave sensing allows low power dissipation in the sensing resistor, while full-wave sensing has less switching noise in the sensing signal. Typically, an RC low-pass filter is used to filter out the switching noise in the sensing signal. The RC time constant of the low-pass filter should be 1/100~1/20 of the switching period.

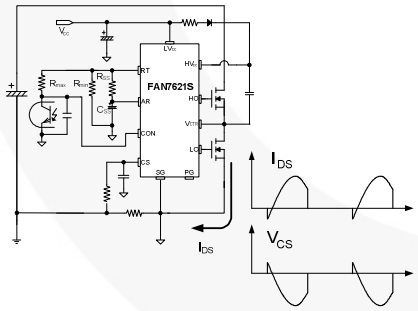


Figure 40. Half-Wave Sensing

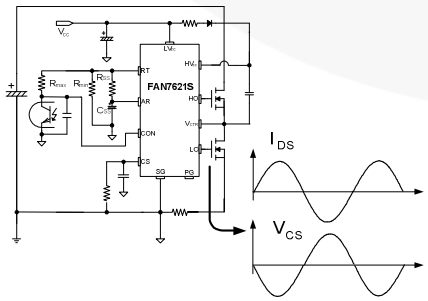


Figure 41. Full-Wave Sensing

(Design Example) Since the OCP level is determined as 2.5A in STEP-17 and the OCP threshold voltage is -0.6V, a sensing resistor of 0.24Ω is used. The RC time constant is set to 100ns (1/100 of switching period) with 1kΩ resistor and 100pF capacitor.

[STEP-21] Voltage and Current Feedback

Power supplies for LED lighting must be controlled by Constant Current (CC) Mode as well as a Constant Voltage (CV) Mode. Because the forward-voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged.

Figure 42 shows an example of a CC and CV Mode feedback circuit for single-output LED power supply. During normal operation, CC Mode is dominant and the CV control circuit does not activate as long as the feedback voltage is lower than reference voltage, which means that CV control circuit only acts as OVP for abnormal modes.

(Design Example) The output voltage (V_O) is 103V in design target. V_O is determined as:

$$V_o = 2.5(1 + \frac{R_{FU}}{R_{FL}})$$

Set the upper-side feedback resistance (R_{FU}) as 330KΩ. R_{FL} is determined as:

$$R_{FL} = \frac{2.5 \times R_{FU}}{(V_o - 2.5)} = \frac{2.5 \times 330K\Omega}{(103 - 2.5)} = 8.2K\Omega$$

The output current (I_{LED}) is 1.46A in design target. Assuming the sensing resistor (R_{SENSE}) of 0.1Ω and feedback resistor (R202) of 47KΩ are used, the input resistor R203 is determined as:

$$R203 = \frac{V_{SENSE} \times R202}{0.36} = \frac{(R_{SENSE} \times I_{LED}) \times R202}{0.36}$$

$$= \frac{(0.1 \times 1.46) \times 47K\Omega}{0.36} = 19K\Omega$$

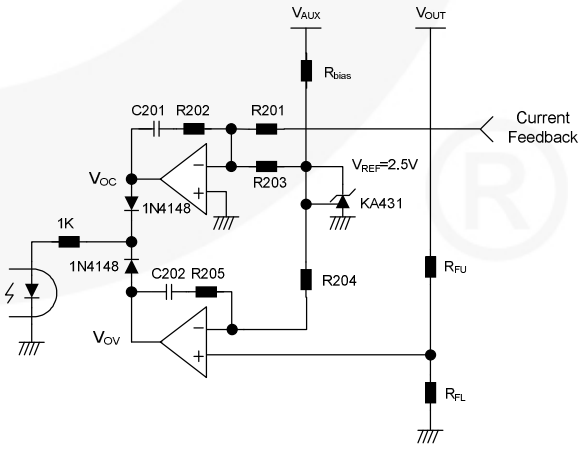


Figure 42. Example of CC and CV Feedback Circuit

4. Schematic of the Evaluation Board

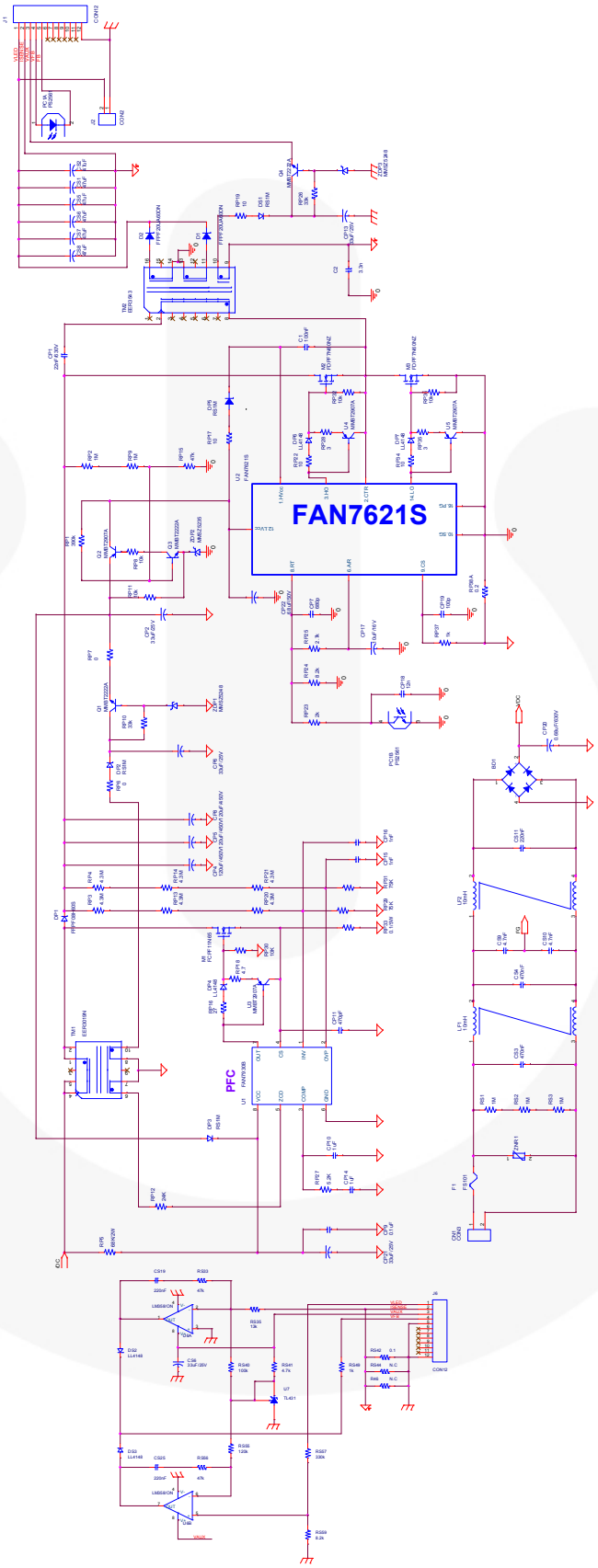


Figure 43. Evaluation Board Schematic

Dimensions: 240 (W) × 80 (H) [mm]

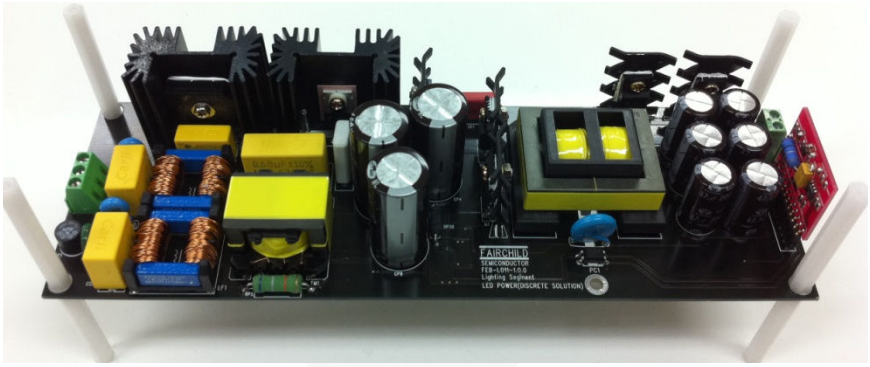


Figure 44. Top View of Evaluation Board

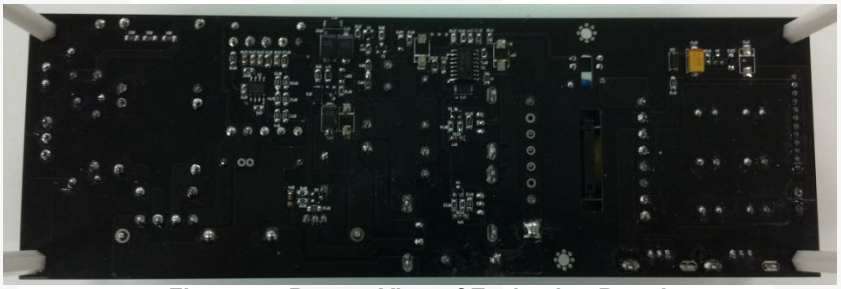


Figure 45. Bottom View of Evaluation Board

5. Bill of Materials

Item No.	Qty	Reference	Part Reference	Description (Manufacturer)
1	1	BD1	600V/8A	Bridge Diode (Fairchild Semiconductor)
2	1	CN1	3PIN	Connector
3	1	CP1	630V22nF	Film Capacitor
4	5	CP2,CP6,CP13,CP21	33µF/25V	SMD Tantal Capacitor
5	3	CP4,CP5,CP8	120µF/450V	Electrolytic Capacitor
6	1	CP7	680p/25V	SMD Capacitor 2012
7	1	CP9	0.1µF/25V	SMD Capacitor 2012
8	2	CP10,CP14	1µF/25V	SMD Capacitor 2012
9	1	CP11	470pF/25V	SMD Capacitor 2012
10	2	CP15,CP16	33µF/25V	SMD Capacitor 2012
11	1	CP17	10µF/16V	Electrolytic Capacitor
12	1	CP18	12nF/25V	SMD Capacitor 2012
13	1	CP19	100pF/26V	SMD Capacitor 2012
14	1	CP20	0.68µF/630V	Film Capacitor
15	1	CP22	100p/25V	SMD Capacitor 2012
16	6	CS1,CS2,CS5,CS6,CS7,CS8	47µF/200V	Electrolytic Capacitor
17	2	CS3,CS4	470nF/400V	Film Capacitor
		CS19,CS25	220nF/25V	SMD Capacitor 2012

Item No.	Qty	Reference	Part Reference	Description (Manufacturer)
18	2	CS9,CS10	220p/400V	Ceramic Capacitor
19	3	CS11	220nF/400V	Film Capacitor
20	1	C1	100nF/50V	SMD Capacitor 3216
21	1	C2	4.7μF/400V	Ceramic Capacitor
22	1	DP1	600V/8A	Hyperfast2 Diode
23	4	DS1,DP2,DP3,DP5	1000V/1A	Fast Rectifier Diode
24	5	DS2,DS3,DP4,DP6,DP7	100V/200mA	SMD General Purpose Diode
25	2	D1,D2	600V/20A	Ultra-Fast Diode
26	1	F1	FS101	Fuse
27	2	J1,J6	12PIN	Connector
28	1	J2	2PIN	Connector
29	2	LF1,LF2	10mH/2.3A	Common-Mode Filter
30	1	M1	650V/11A	MOSFET
31	2	M2,M3	600V/7A	MOSFET
32	1	PC1	Photo Copuler	Photo Coupler
33	3	Q1,Q3,Q4	40V/1A	SMD NPN Transitor
34	4	Q2,U3,U4,U5	40V/200mA	SMD PNP Transitor
35	1	RP1	390kΩ/25V	SMD Resistor 2012
36	5	RS1,RS2,RP2,RS3,RP9	1M/Ω50V	SMD Resistor 3216
37	6	RP3,RP4,RP13,RP14,RP20,RP21	4.3MΩ/50V	SMD Resistor 3216
38	1	RP5	68KΩ/2W	Watt Resistor
39	2	RP6,RP7	0Ω/50V	SMD Resistor 3216
40	5	RP8,RP11	10kΩ/25V	SMD Resistor 2012
		RP30,RP32,RP36	10kΩ/50V	SMD Resistor 3216
41	2	RP10,RP26	33kΩ/25V	SMD Resistor 2012
42	1	RP12	24kΩ/50V	SMD Resistor 3216
43	3	RP15,RS33,RS56	47kΩ/25V	SMD Resistor 2012
44	1	RP16	2.7Ω/25V	SMD Resistor 2012
45	4	RP17,RP19	10Ω/50V	SMD Resistor 3216
		RP22,RP34	10Ω/25V	SMD Resistor 2012
46	1	RP18	4.7Ω/25V	SMD Resistor 2012
47	1	RP23	10kΩ/25V	SMD Resistor 2012
48	2	RP24,RS59	8.2kΩ/25V	SMD Resistor 2012
49	1	RP25	1.8KΩ/25V	SMD Resistor 2012
50	1	RP27	5.1kΩ/25V	SMD Resistor 2012
51	2	RP28,RP35	3Ω/25V	SMD Resistor 2012
52	2	RP29,RP31	75kΩ/50V	SMD Resistor 3216
53	1	RP33	0.1Ω/5W	Watt Resistor
54	2	RP37,RS49	1kΩ/50V	SMD Resistor 3216
55	1	RP38A	0.1Ω/1W	Watt Resistor
56	1	RS35	13kΩ/25V	SMD Resistor 2012
57	1	RS40	100kΩ/25V	SMD Resistor 2012
58	1	RS41	4.7kΩ/25V	SMD Resistor 2013
59	1	RS42	0.1Ω/2W	Watt Resistor

Item No.	Qty	Reference	Part Reference	Description (Manufacturer)
60	2	RS44,R46	NC	NC
61	1	RS55	120kΩ/25V	SMD Resistor 2012
62	1	RS57	330kΩ/25V	SMD Resistor 2012
63	1	TM1	EER3019N-10	PFC Inductor
64	1	TM2	EER3543-16	LLC Transformer
65	1	U1	FL7930B	CRM PFC Controller
66	1	U2	FAN7621S	LLC Resonant Controller
67	1	U6	LM358	OP-AMP
68	1	U7	KA431	Shunt Regulator
69	2	ZDP1,ZDP3	MMSZ5248	Zener Diode 18V
70	1	ZDP2	MMSZ5235	Zener Diode 6.8V
71	1	ZNR1	10D471	Varistor 470V

Related Datasheets

FL7930B — Single-Stage Flyback and Boundary Mode PFC Controller for Lighting

FAN7621S — Controller for Resonant Half Bridge

FDPF17N60NT — 600V N-Channel MOSFET, UniFET™2

FDPF7N60NZ — 600V N-Channel MOSFET, UniFET™2

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