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AN-9716
Reset Timers

Applications

As smart phones continually add functionality, it increases the likelihood of device lock up. This condition has been called the “White Screen of Death” which is a new take on the popular phrase used to describe Windows PCs after a system fault. Before the advent of standalone reset timers, users were required to remove the phone battery to force a device restart. As more device suppliers remove access to the device battery, it has become necessary to provide a more convenient way of forcing a device reset.

Reset timers create a failsafe mechanism for users to reset the phone using a single- or multiple-button long key press. Reset timers have an advantage over software solutions in that the independent, hardware-based solution is not susceptible to software crashes. The need for hardware-based reset timers is the result of an increased likelihood that device operating systems can be derailed by the growing applications and features they must support.

Figure 1. “White Screen of Death” Example

Considerations in Choosing a Reset Timer

Configurable Reset Time

Is it unclear what the final reset time should be? Are you concerned that the preset reset time is too close to a critical system timing parameter? Fairchild reset timers feature selectable reset times (*see Table 1*). When choosing a reset timer, select a delay sufficient to prevent unintended resets caused by accidental key presses. For this reason, the shortest reset configuration offered by Fairchild reset timers is three seconds.

Reset Timer Output Type

Fairchild offers open-drain and push-pull outputs that vary in the output pulse duration. In reset timers where the last digit in the product name is 0, i.e. FT8010, the reset output signal remains LOW or HIGH for the entire time the SRx inputs are held LOW (as long as the initial reset time requirement was met). In this case, as soon as either SRx input is released, the reset outputs return to their default states. Reset timers where the last digit is 1, i.e. FT7521, feature a fixed-output pulse width of 400ms, regardless of the time when the SRx pins are released. Figure 2 illustrates the relationship between SRx and the output signal generated by the reset timer.

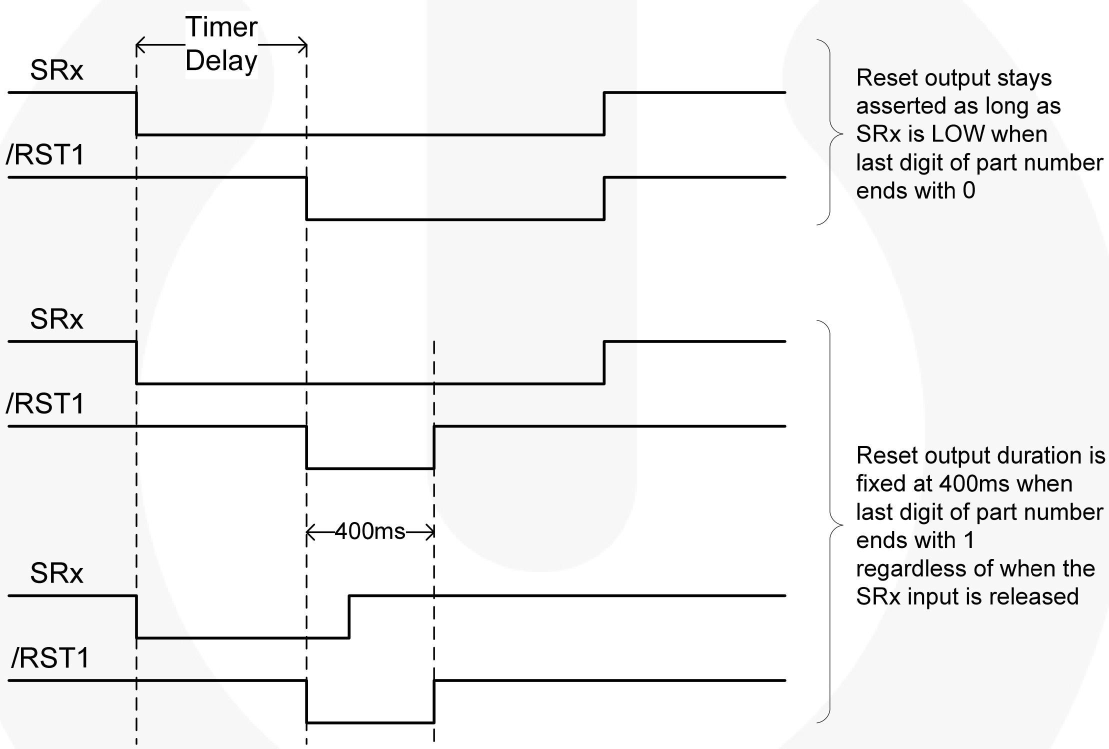

Figure 2. Reset Time Output Pulse Type

Application Examples

Example 1:

The rest timer output is connected to the gate control of a power PFET in series with the battery supply. By using the push-pull output, the reset timer immediately shuts the power FET off when the reset timer output is driven HIGH. The duration of the output pulse is not important because shutting off the PFET starves the remaining circuitry of power and forces a system reboot when the reset timer output returns to default state. Note that, as soon as the reset timer output goes HIGH, the device screen goes black, indicating that the reset function has been enabled and it is OK to release the reset button(s). In this case, the desired reset time and availability of a push-pull output option are important in the selection of a reset timer.

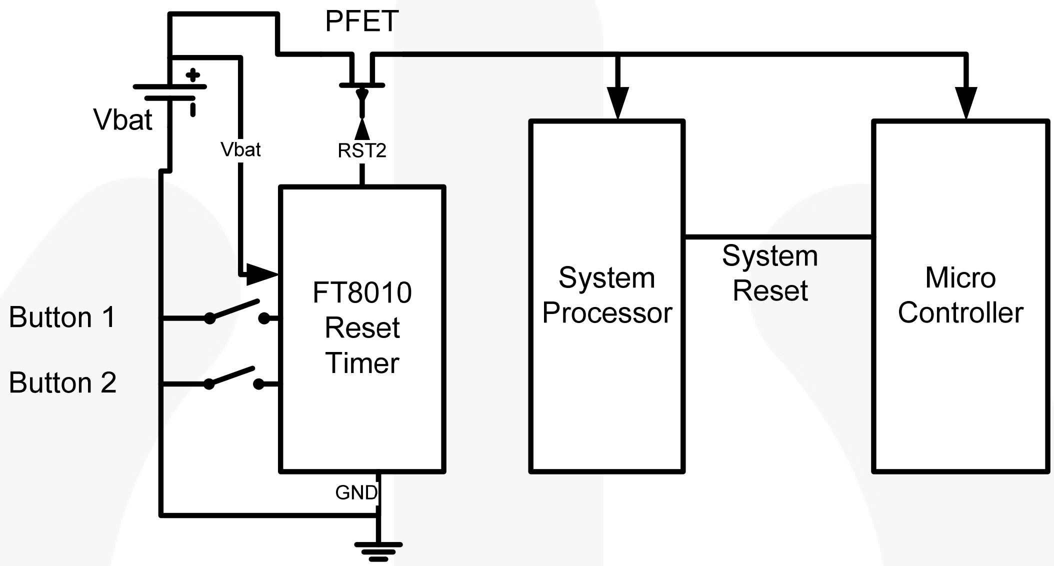

Figure 3. Application Example Scenario 1, Timer Output as Power FET Gate Control

Example 2:

As shown in Figure 4, the reset timer output is connected to the power management IC (PMIC), which then controls the system processor. For this application, the reset timer output signals the PMIC to reset by asserting a reset pin on the PMIC. The PMIC immediately resets and sends a fixed-pulse to the central processor, which signals it to also reset.

Similar to the first example, the output pulse duration is not critical in this application because the phone reset sequence begins as soon as the reset timer output is asserted. The desired reset time and availability of the correct output type are critical in selecting a reset timer for this application.

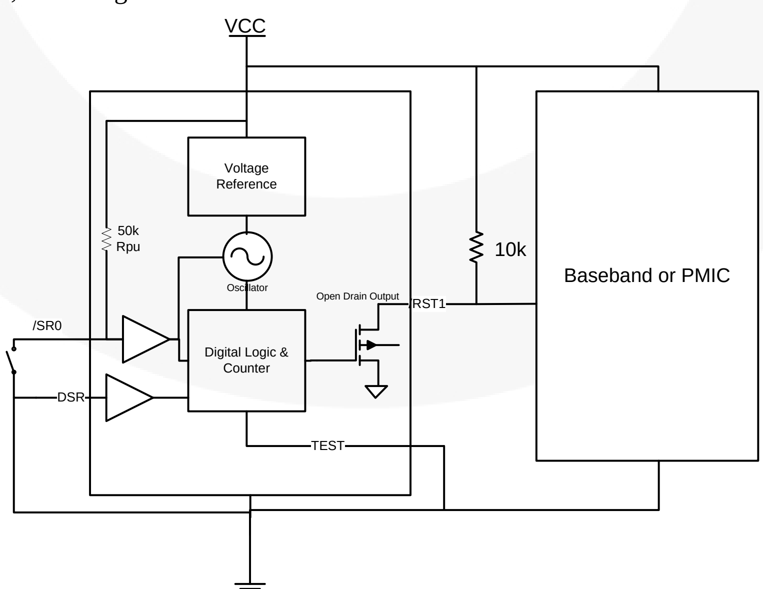

Figure 4. Application Example Scenario 2, Timer Output into PMIC using the FT7521

Example 3:

In this final example, the reset time output feeds directly into both the PMIC and central processor. In the previous examples, the user has visual cues that the system had been reset before the reset chip output signal has returned to its default state.

In this last application, the central processor may require a pulse in the reset pin to begin the reset process; the user can hold the reset buttons, waiting for an indication of reset, if a reset timer without the fixed output pulse is chosen.

Selecting a reset timer with a fixed output pulse[(1)], allows the system to begin the reset process before the user releases the buttons to provide a better user experience.

Note:

1. This feature is offered by Fairchild's FTXXX1 series.

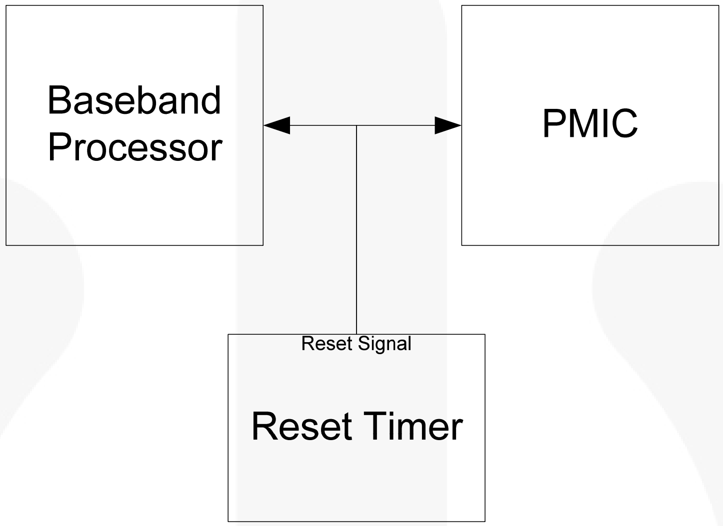

Figure 5. Application Example Scenario 3, Timer Output into PMIC and Baseband

Reference Schematic for FT-Series Devices

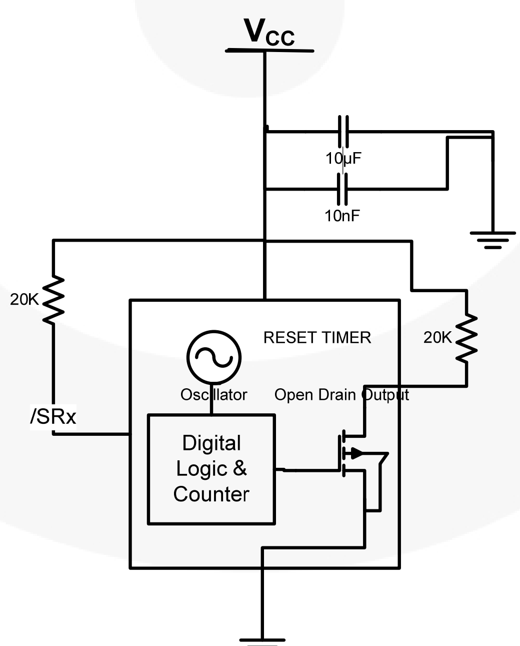

Figure 6. Reset Timer Decoupling and Pull-Up Resistor Reference Schematic (FT8010[(2)] Shown)

Decoupling Capacitor Value and Placement

Decoupling capacitors should be placed as close to the V_{CC} supply pin of the reset timer as possible. Decoupling values shown here are typical values, where the larger 10µF capacitor is used to stabilize the reset timer supply voltage in the event of significant loading on the power supply that could lead to supply droop. Depending on the stability of the system supply, this value could be reduced. Fairchild recommends that the final value be between 1µF and 10µF.

The second, smaller capacitor is included to filter high-frequency power supply noise and provide a return path for fast edge rate transient voltages. This value is can also be adjusted to suit the specific needs of the application. Fairchild recommends it be in the range of 10nF to 100nF.

There is flexibility in the selection of pull-up resistor values on the SRx inputs and open-drain output. The reference schematic in Figure 6 provides a conservative estimate for the pull-up resistor values with the intent to limit system power consumption while the SRx inputs and open-drain output are held LOW. Fairchild reset timer outputs are designed to sink, at most, 500µA. Based on this and the assumption of a worst -case V_{CC} supply referenced pull-up voltage of 5V, the minimum pull-up resistor value should be 10kΩ. Larger pull-up values result in less current consumption when in LOW state.

When choosing a pull-up resistor, the designer must also consider the desired edge of the output/input transition. Larger values, while saving power, result in slower output/input transitions as a function of the pull-up resistance and line capacitance. In most reset time applications, output/input transition times are not critical and the designer opts for lower power consumption by choosing a larger pull-up resistor.

Table 1. Reset Timer Selection Table

Reset Timer	Fixed-Output Pulse	Open-Drain Output	0-Second Test Mode	Integrated Pull-Up	Time Duration	Static Current	Number of Reset Inputs
FT8010	No	Yes	No	No	7.5, 11.25 Seconds	20µA	2
FT7521	Yes	Yes	Yes	Yes	7.5 Seconds	1µA	1
FT3001	Yes	Yes	No	No	3, 3.75, 4.5, 6 Seconds	1µA	2
FT10001	Yes	Yes	Yes	Yes	10 Seconds	1µA	1

Note:

2. FT7521 and FT10001 have a built-in pull-up resistor on the reset timer input /SR0; therefore, external pull-up resistors are not required.

Application Guidelines

Table 2 should help the designers properly configure the reset timer. Following these suggestions avoids errors, increasing the probability first pass design success.

Table 2. Use Guidelines

Do	Don't
Tie TRIG to GND for Normal Operating	Tie the TRIG to V_{CC}
Tie DSR to Valid V_{CC} or GND Before Power-up	Leave DSR Floating
Leave the DSR Pin Unchanged During Normal Operation	Change the DSR Pin During Normal Operation
Pull-Up Resistor Connected for Output /RST1	No Pull-Up Resistor Connected for Output /RST1

Summary

Reset timers provide a solution to the "White Screen of Death" crash and subsequent need to reboot in portable devices. Selection of the best timer in the application occurs after considering the system requirements, where the reset timer delay and output pulse types are generally the deciding factors. Depending on the application, there is a solution available with devices that offer both push-pull and open-drain outputs.

Related Datasheets

FT8010 — Reset Timer with Configurable Delay Time

FT7521 — Reset Timer with Fixed Delay and Reset Pulse

FT3001 — Reset Timer with Configurable Delay Time

FT10001 — Reset Timer with Fixed Delay and Reset Pulse

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