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Application Note AN9046

Assembly Guidelines for Dual Power56 Packaging

By Dennis Lang

INTRODUCTION

The Fairchild® Dual Power56 package is based on Molded Leadless Packaging (MLP) technology. This technology has been increasingly used in packaging for power related products due to its low package height, excellent thermal performance with large thermal pads in the center of the package which solder directly to the printed wiring board (PWB). Modularity in package design, single and multi-die packages, is within the capability of MLP technology.

The Dual Power56 has two large die attach pads allowing direct soldering to the PWB for best thermal and electrical performance. These two pads are the co-packaged high and low side MOSFETs. The Dual Power56 is designed to be used in high current synchronous buck DC-DC circuits, saving board space and component count by integrating the high and low side MOSFETs into one package.

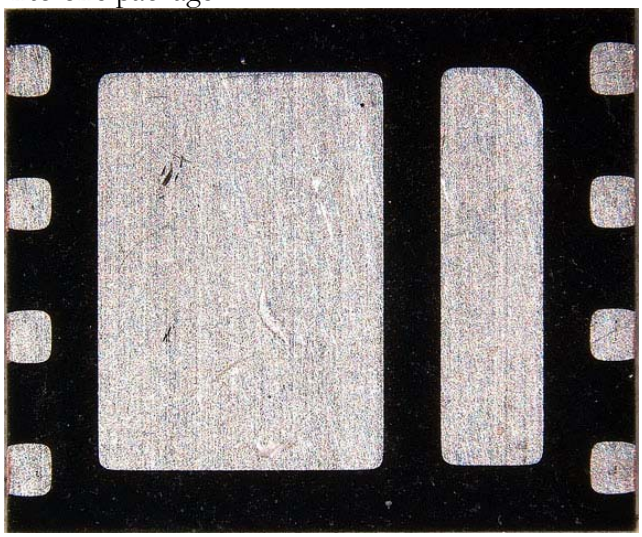

Figure 1: Bottom side view showing pads for Dual Power56.

This application note focuses on the soldering and back end processing of the Dual Power56.

BOARD MOUNTING

The solder joint and pad design are the most important factors in creating a reliable assembly. The pad dimensions must be designed to allow for tolerances in PWB fabrication and pick and place, which are necessary for proper solder fillet formation. MLP packages, when the pre-plated lead-frame is sawn, show bare copper on the end of the exposed edge leads. This is normal, and is addressed by IPC JEDEC J-STD-001C "Bottom Only Termination". In practice it has been found that optimized PWB pad design and a robust solder process often yields solder fillets to the ends of the lead due to the cleaning action of the flux in the solder paste.

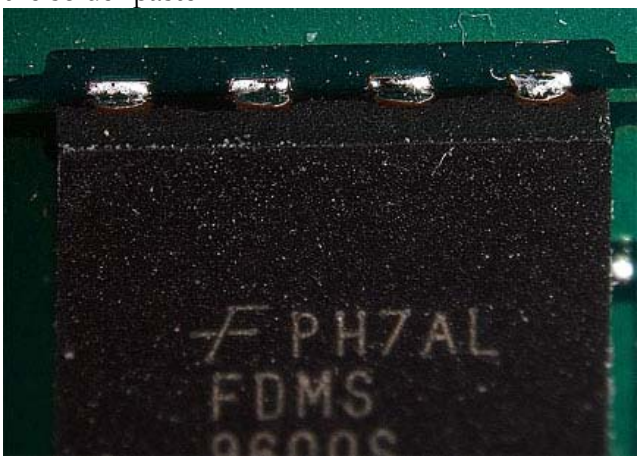

Figure 2: Exposed copper on package edge, with solder wetting after reflow, from singulation process.

PWB DESIGN CONSIDERATIONS

Any land pad pattern must take into account the various PWB and board assembly tolerances for successful soldering of the MLP to the PWB. These factors have already been considered for the recommended footprint given on the datasheet. It

is recommended the customer follow this recommended footprint to assure best assembly yield, thermal performance and overall system performance.

PAD FINISH

The dual Power56 is sold with a NiPdAu lead free lead finish. Immersion silver, immersion nickel gold and organic surface protectant, OSP are the pad finishes of choice for lead free processing. Each finish has useful properties, and each has its challenges. It is beyond the scope of this paper to debate each system's merits. No one finish will be right for all applications, but currently the most commonly seen in large scale consumer electronics, largely due to cost, is OSP. A high quality OSP, formulated for the rigors of lead free reflow, like Enthone® Entek® Plus HT is recommended.

PWB MATERIAL

It is recommended that lead free FR-4 is used in PWB construction. Lower quality FR-4 can cause numerous problems with the reflow temperatures seen when using lead free solder. IPC-4101B "Specification for Base Materials for Rigid and Multilayer Printed Boards" contains further information on choosing the correct PWB material for the intended application.

USING VIAS WITH DUAL POWER56

Often the designer will wish to place vias inside of the thermal pads. While this is acceptable, the user should realize that vias often create voiding, and is advised to carefully characterize the PWB and process designs with x-ray inspection to ensure there is not a voiding problem. There are several types of vias that can be used in PWB design. Blind vias are not recommended due to the fact they often trap gases generated during reflow and yield high percentages of voiding. Solder mask can also be placed over the top of the via to prevent solder from wicking down the via. It has been shown in previous studies that this will create a higher incidence of voiding than an open through-hole or filled via. If through hole vias are used, a drill size of 0.3mm with 1 ounce copper plating yields good performance. With through-hole vias, solder wicking through the hole, or solder protrusion, must be considered. In high reliability applications, filled vias are the preferred due to lower incidences of voiding during reflow. The user can expect this approach to eliminate the stress riser created by a void at the edges of the via barrel.

STENCIL DESIGN

It is estimated that 60% of all assembly errors are due to paste printing. For a controlled, high yielding manufacturing process, it is therefore the most critical phase of assembly. Due to the importance of the stencil design, many stencil types have been characterized to determine the optimal stencil design for the recommended footprint pad, on a typical application board with Organic Surface Protectant (OSP) surface finish, thermal vias, on FR-4. Solder paste coverage for the thermal pads was printed ranging from 50-65% coverage. To allow gases to escape during reflow it is recommended that the paste be deposited in a grid allowing "channels" for gases to vent. It was found that 40-60% solder coverage on the large "S1/D2" pad yielded good void performance, while maintaining good standoff height. The paste was printed from a 5 mil thick stainless steel stencil. Various different stencil apertures shapes can be used, but were not studied here. The paste is printed on the outer pins with a slightly reduced ratio to the PWB pad. Per IPC-7525 "Stencil Design Guidelines" gives a formula for calculating the area ratio for paste release prediction:

$$Area\ Ratio = \frac{Area\ of\ Pad}{Area\ of\ Aperture\ Walls} = \frac{L * W}{2 * (L * W) * T}$$

Where L is the length, W the width, and T the thickness of the stencil. When using this equation, an Area Ratio >0.66 should yield acceptable paste release. The recommended stencil apertures can be found in the appendix.

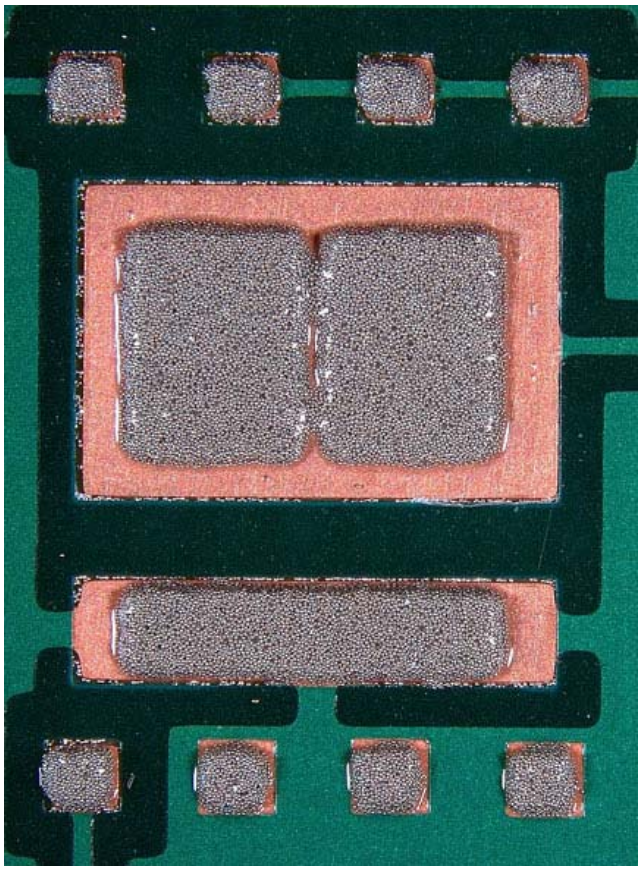

Figure 3: Printed Solder Paste, 50% coverage.

SOLDER PASTE

The Dual Power56 is a RoHS compliant and lead free package. The lead finish is NiPdAu. Any standard lead free no clean solder paste commonly used in the industry should work with this package. The IPC Solder Products Value Council has recommended that the lead free alloy, 96.5 Sn/3.0Au/0.5Cu, commonly known as SAC 305, is "…the lead free solder paste alloy of choice for the electronics industry". Type 3 no-clean paste, SAC 305 alloy, was used for the construction of the boards studied to optimize the process.

REFLOW PROFILE

The optimum reflow profile used for every product and oven is different. Even the same brand and model oven in a different facility may require a different profile. The proper ramp and soak rates are determined by the solder paste vendor for their specific products. Obtaining this information from the paste vendor is highly recommended. If one is using a KIC® profiler, downloading the latest paste library from KIC® will yield ramp rate and soak times at temperature for most commonly used solder pastes. Using this data the software can optimize the zone set-points and speed. The Fairchild® Dual Power56 is rated for 260ºC peak temperature reflow. Below is a sample reflow profile used for building demonstration boards. Attached in the appendix is a reflow profile example. This profile is provided for reference only; different PWBs, ovens and pastes will change this profile, perhaps dramatically.

VOIDING

Voiding is a very controversial topic in the industry currently. The move to lead free solders has driven the need for intense study in the area of solders, solder joints and reliability effects. There are varying viewpoints on the effect of vias and allowable quantity. There are several types of voids; for simplicity in this applications note we will classify them into two categories, macro voids, and micro voids.

Macro voids could also be called process voids. Macro voids are the large sized voids commonly seen on x-ray during inspection. These voids are due to process design and process control issues, or PWB design issues. All of the parameters discussed in this application note will effect macro-voiding. Most standards that currently exist, such as IPC-610D specifically address void criteria for BGA, and limit it to 25%. This standard is for macro voiding.

There is currently no industry standard for macro voiding in MLP solder joints. Fairchild® has completed several reliability studies characterizing voiding in various types of components with large thermal pads, and the effect on reliability. It was found that components with ≤25% voiding exhibit acceptable reliability performance in package qualification temperature cycling. Fairchild® recommends the guideline of 25% maximum voiding for MLP type packages.

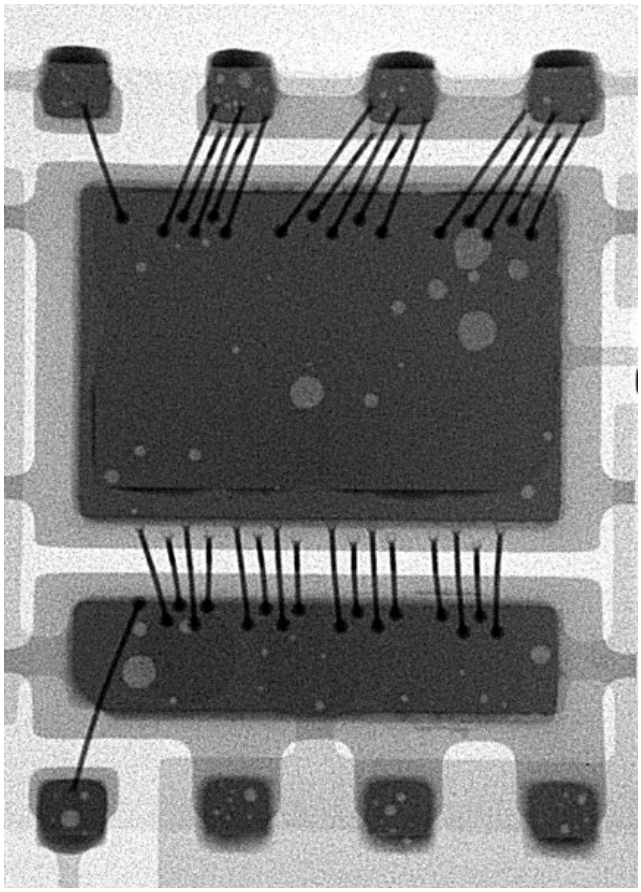

Figure 4: X-ray image showing voiding caused by normal process variation during reflow.

There are also several forms of micro-voiding, namely planar micro voids and Kirkendall voids. The mechanism of void creation is different for each; however both are practically undetectable by x-ray inspection. Both types are also currently the subject of several in-depth studies; however, none have confirmed theories of creation.

Planar micro voids, or "champagne voids" occur at the PWB land to solder joint interface. There are several theories on the mechanism that creates planar micro voids, but there is no industry consensus on the causal mechanism for this type of voiding. Planar micro voids are a risk for reliability failures.

Kirkendall voids are created at the interface of two dissimilar metals at higher temperatures. In the case of solder attachments, at the pad to joint intermetallic layer. They are not due to the reflow process; Kirkendall voids are created by electro-migration in assemblies that spend large amounts of time above 100ºC. There is currently conflicting evidence whether Kirkendall voids are a reliability risk or not.

REWORK

Due to the high temperatures associated with lead free reflow, it is recommended that this component not be reused if rework becomes necessary. The Dual Power56 should be removed from the PWB with hot air. After removal, the Dual Power56 should be discarded. The solder remnants should be removed from the pad with a solder vacuum or solder wick, the pads cleaned and new paste printed with a mini stencil. Localized hot air can then be applied to reflow the solder and make the joint. Due to the thermal performance of this component, and the typical high performance PWB it will be mounted on, quite a bit of heat energy will be necessary. Heating of the PWB may be helpful for the rework process.

BOARD LEVEL RELIABILITY

As mentioned previously, per JDC-STD-001D a solder fillet is not required on the side of the lead for this package. But it has been found through modeling and temperature cycling that a solder fillet on the lead end can improve reliability. An improvement of 20% can be expected with this fillet. It has also been found that the 20% reliability enhancement is attained even when the fillet only wets halfway up the side of the lead. The customer can expect to create reliability enhancing solder fillets through proper process design and control.

As part of the standard reliability testing this package was temperature cycled from -10 to 100C. There could be no failures in the sample set at 1000 cycles to pass the test.

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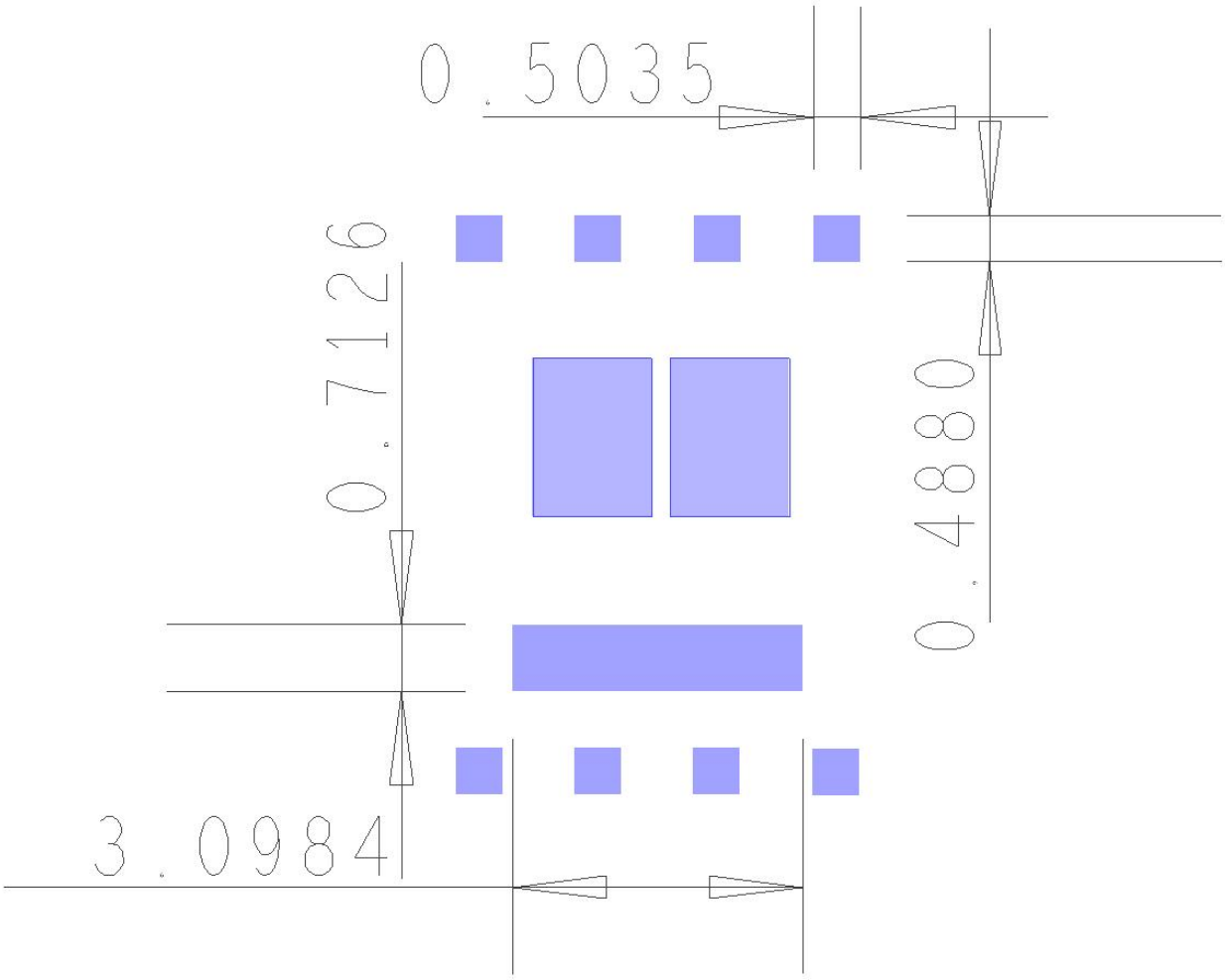
Applicable FSIDs: FDMS9600S, FDMS9620S

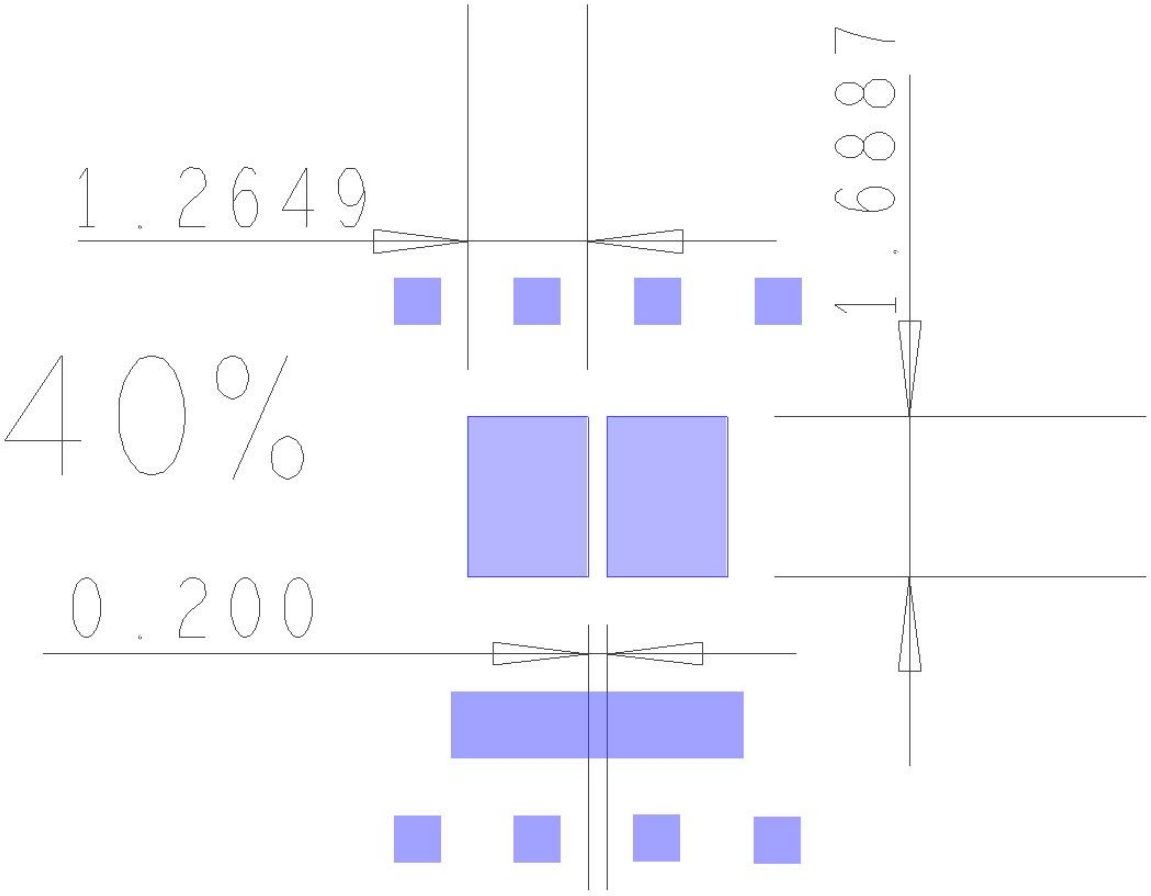
APPENDIX

NOTE: *The 8 edge pins and "D1" high side solder apertures were not varied, only the "S1/D2" pad had solder area coverage varied.*

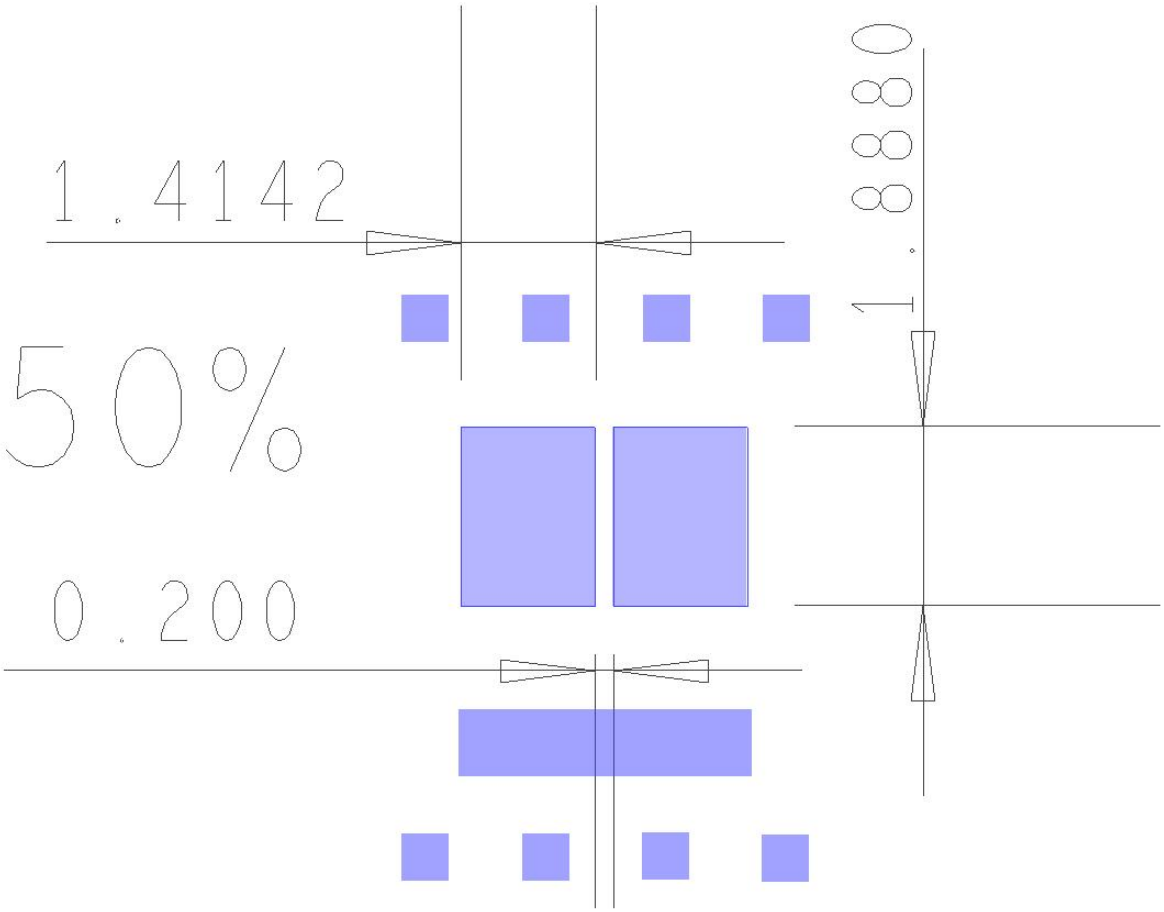
Dimensioned Stencil Apertures, Edge pins and "D1" pad dimensions, the same for all three drawings:



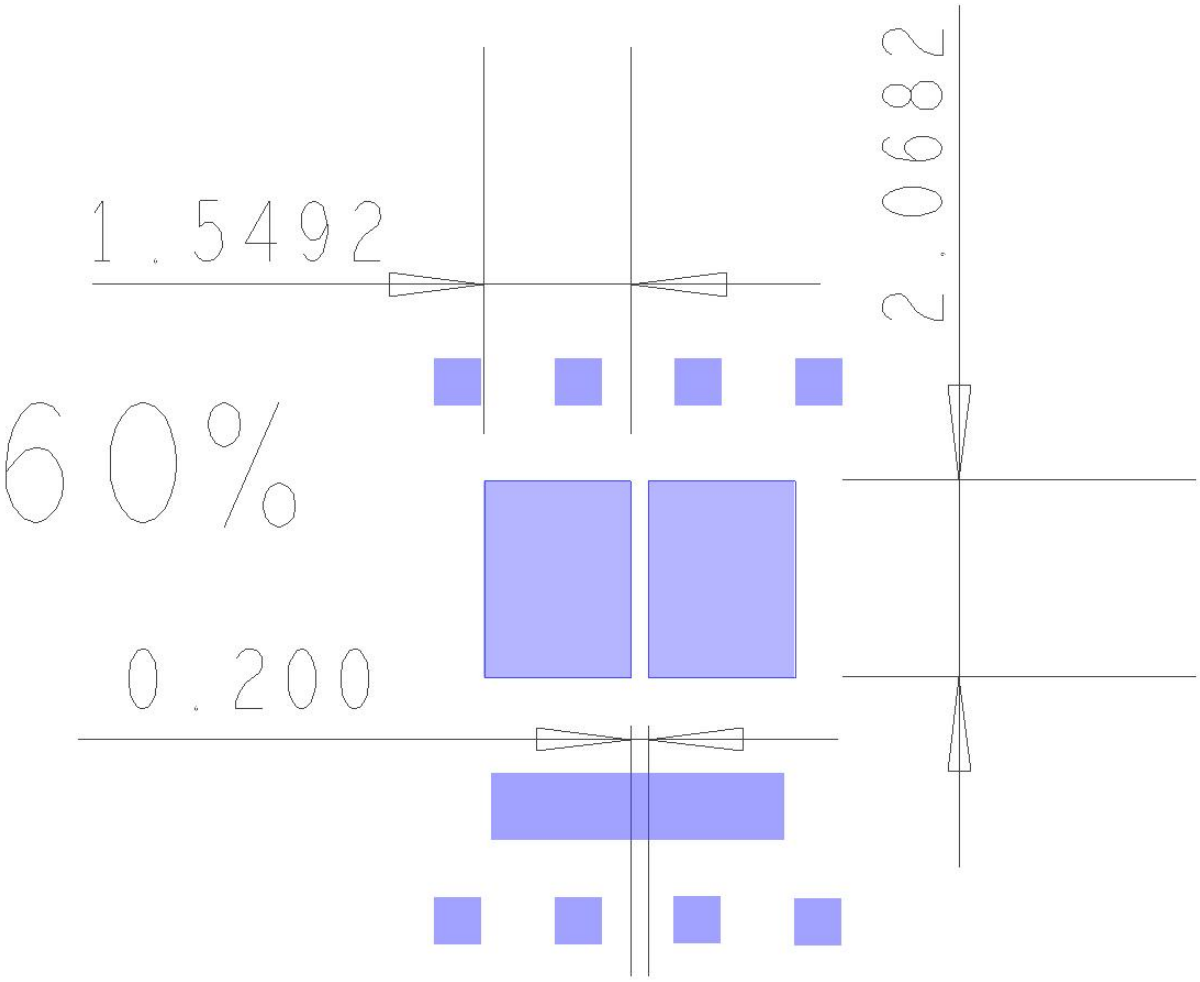
Dimensioned Stencil Apertures, 40% large pad coverage:



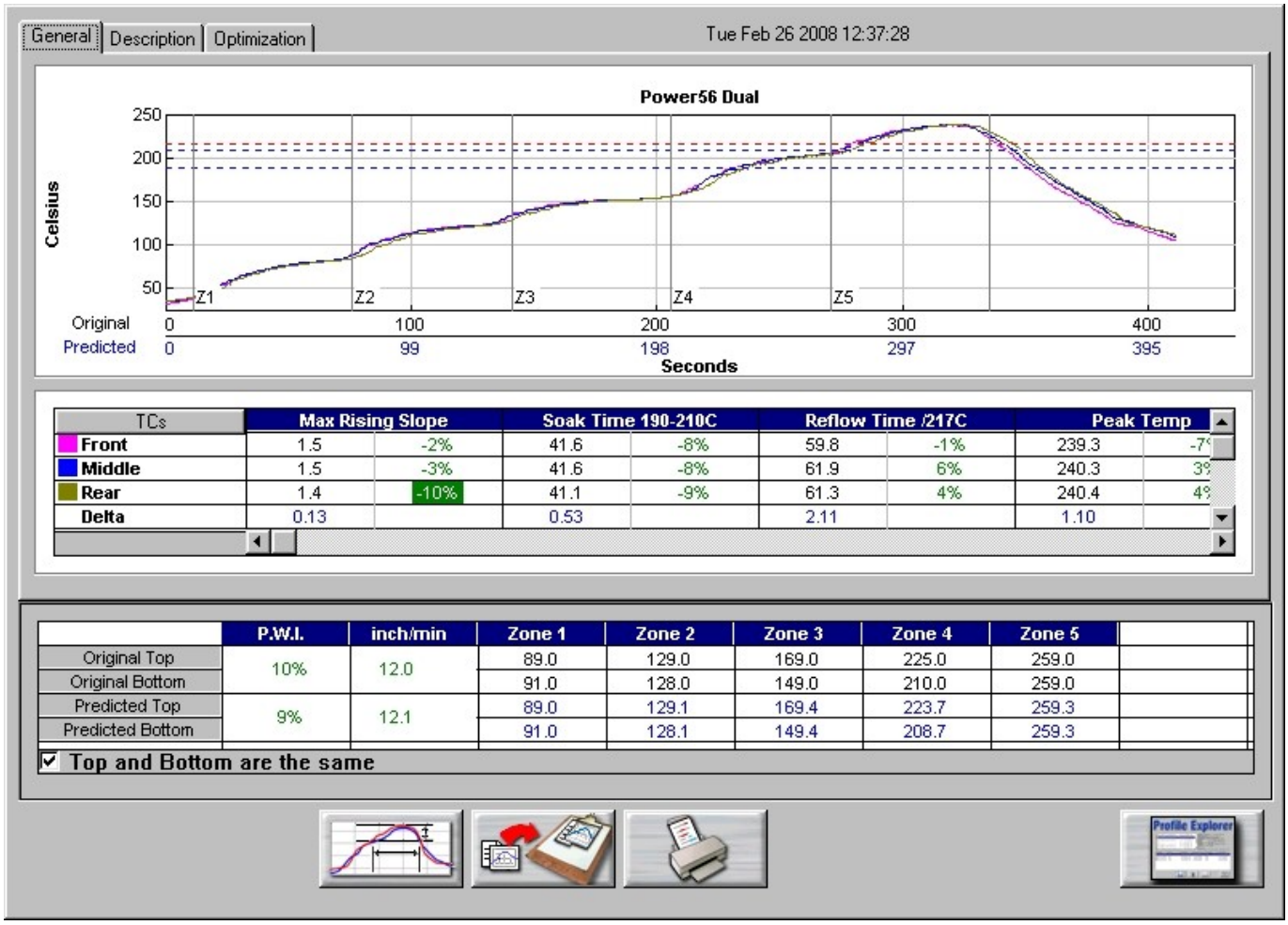
Dimensioned Stencil Apertures, 50% large pad coverage:



Dimensioned Stencil Apertures, 60% large pad coverage:



Reflow profile used for building demonstration boards.



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