Power MOSFET Avalanche Guideline

AN-9034

Introduction

The Power MOSFET is a very popular switching device used in switching power supplies and DC-DC converters. Their operation frequency is being continuously increased to reduce size and increase power density. This causes high di/dt, intensifies the negative effect from para-sitic inductances, and results in high voltage spike between the Power MOSFET drain and source during device turn off. The spike is worst at power on due to empty bulk capacitors and small inductance because the transformer primary side inductance almost reaches the level of leakage inductance. Fortunately, the Power MOSFET is equipped to withstand a certain level of stress, unnecessitating expensive protection circuits. This note presents an effective way to determine the applicability of a Power MOSFET in an application. The designers can balance between cost and reliability.

1. A Rating System: Single Pulse UIS SOA

onsemi has introduced a rating system that specifies the Power MOSFET capability for single pulse Unclamped Inductive Switching (UIS) [1]. This system enables easy determination and/or estimation of device feasibility in any application with simple parameters: the peak current through the Power MOSFET during avalanche (I_{AS}), the junction temperature at the start of the UIS pulse (T_J), and the time the Power MOSFET remains in avalanche (t_{AV}). By plotting I_{AS} and t_{AV} on a graph the user can check the UIS capability of the device. The application specific part of **onsemi** UltraFET and POWERTRENCH® provide such rating chart, and a part of QFET datasheets will soon be updated.

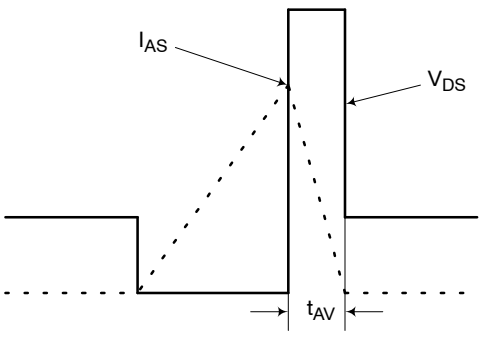

Figure 1. UIS Waveforms

2. Over-Voltage Conditions

The over-voltage conditions in actual applications can be classified into two different groups. One is when the drain-source voltage of Power MOSFET exceeds the specified absolute maximum rating but is still short of the breakdown voltage of the device. This is not an avalanche situation and the device feasibility can be determined through junction temperature analysis. Another is when the device breaks down and goes into avalanche mode. The Rating System is a great tool for avalanche mode analysis.

3. Avalanche Mode Analysis

When the Power MOSFET avalanches, the drain-source voltage is clamped to its effective breakdown voltage and the current is commutated through a parasitic antiparallel diode. Figure 2 shows typical avalanche waveforms in switching power supplies. The drain-source voltage is over 1 kV and a commutating current is observed.

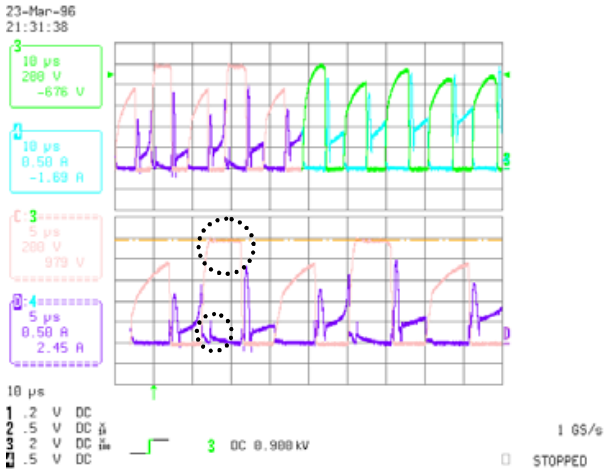

Figure 2. Device Breakdown, 800 V Rated MOSFET

The UIS Rating System is very useful in dealing with avalanche situations. There are three areas in the UIS SOA graph as indicated in Figure 3: (1) above and right of the 25 °C line, (2) below and left of the maximum junction temperature line, (3) in between the two lines. (1) and (2) are easy to determine: the device is within the UIS rating ((2)), or beyond the rating ((1)). But the junction temperature of the Power MOSFET at the start of the UIS pulse is required to determine (3). The junction temperature analysis methods will be discussed later in detail.

This UIS Rating System can also be applied to repetitive pulses through superposition technique. Each UIS pulse is evaluated separately just as in single pulse. Usually, the last pulse in a series of power pulses occurs at the highest junction temperature and is therefore the worst stress. If the Power MOSFET is within the specified UIS rating for the last pulse, it is certainly within the UIS ratings for previous pulses which occurred at a lower junction temperature [2].

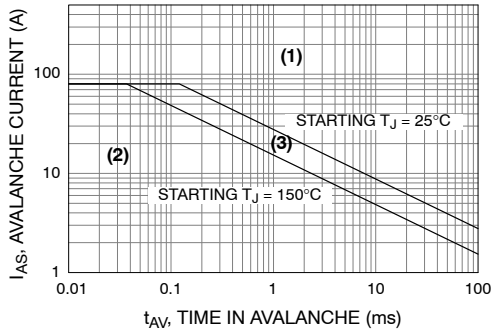

Figure 3. UIS Capability, FDP050AN06A0

4. Junction Temperature Analysis

Generally, breakdown of the Power MOSFET seldom occurs even if the drain-source voltage exceeds the absolute maximum rating. The BV_{DSS} of the Power MOSFET has a positive temperature coefficient as shown in Figure 4. It reaches about 990 V at 120 °C in this example. Therefore, a greater voltage is required to cause device breakdown at higher temperature. In many cases, the ambient temperature during the Power MOSFET operation is over 25 °C and the power loss causes the junction temperature of the Power MOSFET to rise above the ambient temperature.

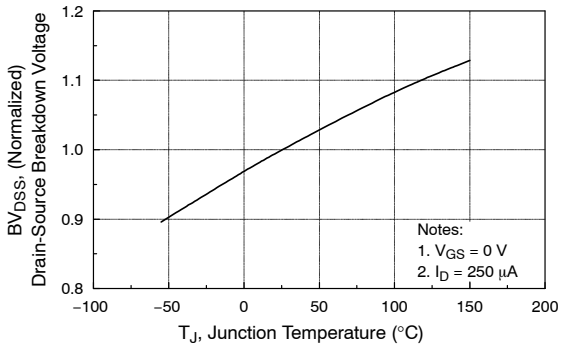

Figure 4. Normalized BV_{DSS} vs T_J, FQA11N90C

Also, note that the BVDSS in Figure 4 is measured at 250 μA of the drain current. In a real breakdown, the drain current reaches a much higher level and the breakdown voltage is even higher than the above value.

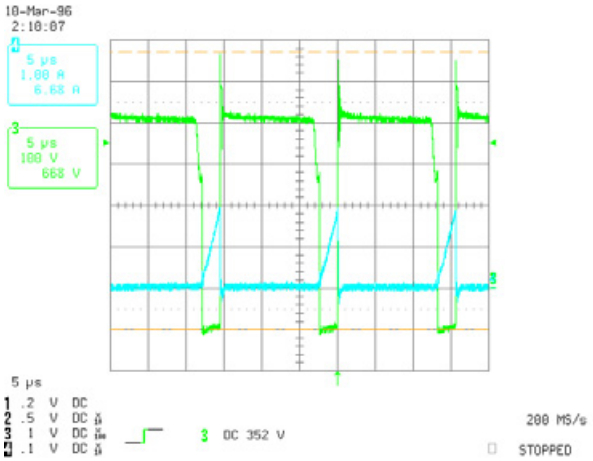

Figure 5. Waveforms from Switching Power Supply, 600 V Rated MOSFET

For practical purposes, an actual breakdown voltage in applications is chosen as 1.3 times the rated low current breakdown voltage [1]. Figure 5 is an example of this non-breakdown but over the absolute maximum rating. The peak drain-source voltage is 668 V but there is no breakdown yet.

Even though the abnormal voltage spike did not cause a device breakdown, the junction temperature of the Power MOSFET should be kept below the specified maximum junction temperature to ensure reliability. The steady state junction temperature can be expressed as

$$T_J = P_D R_{\Theta JC} + T_C \quad \text{(eq. 1)}$$

where
T_J: junction temperature
T_C: case temperature
P_D: power dissipated in the junction
$R_{\Theta JC}$: steady state thermal resistance from junction to case

In many applications, however, the power dissipated in the Power MOSFET is pulsed rather than DC. When a power pulse is applied to the device, the peak junction temperature varies depending on peak power and pulse width. Thermal resistance at a given time is called transient thermal resistance and is expressed as

$$Z_{\Theta JC}(t) = r(t) \times R_{\Theta JC} \quad \text{(eq. 2)}$$

where r(t) is a time dependent factor regarding thermal capacity. For very short pulses, r(t) is quite small, but for long pulses it is nearly 1 and transient thermal resistance approaches the steady state thermal resistance. Most **onsemi** Power MOSFET datasheets have a graph similar to that of Figure 6.

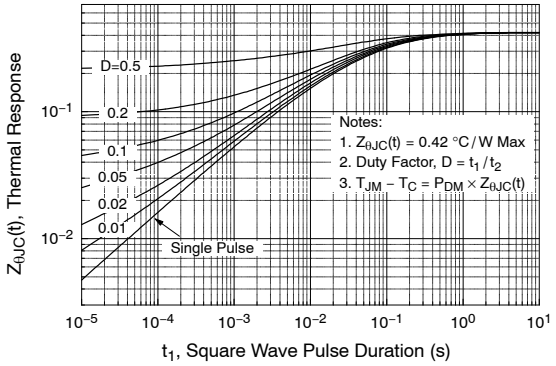

Figure 6. Transient Thermal Response, FQA11N90C

From this curve, the junction temperature can be obtained as follows:

$$T_J = P_D Z_{\Theta JC}(t) + T_C \quad \text{(eq. 3)}$$

For example, the calculation of the temperature rise resulting from single 2 kW power pulse applied to FQA11N90C during 1 μs can be expressed as follows:

$$T = P_D Z_{\Theta JC}(1\ \mu s) = 2000 \times 1.49 \times 10^{-3} \approx 3\ ^\circ C \quad \text{(eq. 4)}$$

The applied power is substantial but the temperature rise is only 3 degrees. Note that a power dissipation rating specified in the datasheet is a steady state power rating, and in a relatively short time the Power MOSFET can handle even greater power pulse.

In the above example, however, transient thermal resistance of 1 μs is not available in Figure 6. In cases where the given time is too short and out of the graph range, the single pulse transient thermal resistance is known to be proportionate to the square root of time. So $Z_{\Theta JC}(1\ \mu s)$ becomes

$$Z_{\Theta JC}(1\ \mu s) = Z_{\Theta JC}(10\ \mu s) \times \sqrt{\frac{1\ \mu s}{10\ \mu s}} = \quad \text{(eq. 5)}$$

$$= 4.72 \times 10^{-3} \times \sqrt{0.1} = 1.49 \times 10^{-3}$$

where
$Z_{\Theta JC}(10\ \mu s)$: taken from Figure 6

The above thermal response is based on a rectangular power pulse. It is possible to obtain a response for arbitrary shapes. However, since the mathematical solution would be very complex, it would be easiest to convert it to an equivalent rectangular pulse. Some examples for triangular and sine wave power pulses are shown in Figure 7.

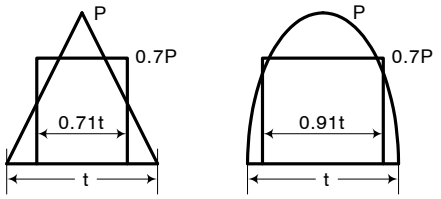

Figure 7. Conversion of Power Pulses

The equation 3 can also be applied to applications that have repetitive pulses. The transient thermal resistance for repetitive pulses can be approximated as follows [3]

$$Z_{\Theta JC}(t) = \left[\frac{t_1}{t_2} + \left(1 - \frac{t_1}{t_2}\right) r(t_1 + t_2) + r(t_1) - r(t_2)\right] R_{\Theta JC} =$$

$$= \frac{t_1}{t_2} R_{\Theta JC} + \left(1 - \frac{t_1}{t_2}\right) Z_{\Theta JC}(t_1 + t_2) + Z_{\Theta JC}(t_1) - Z_{\Theta JC}(t_2) \quad \text{(eq. 6)}$$

where
t_1: pulse width of the power pulse
t_2: period of the power pulse

Assume a situation where the drain-source voltage of a Power MOSFET applied to a switching power supply exceeds its maximum rating specified in the datasheet during delay time to protection activation while conducting short circuit test. The specific conditions are as follows: FQA9N90C switching device, 100 ns t_{AV}, 9.2 μs period, and 20 ms delay time. In this case, the transient thermal resistance becomes

$$Z_{\Theta JC}(t) = 0.01 \times Z_{\Theta JC}(20\ ms) + (1 - 0.01) \times$$

$$\times Z_{\Theta JC}(9.3\ \mu s) + Z_{\Theta JC}(100\ ns) - Z_{\Theta JC}(9.2\ \mu s) = 0.00274 \quad \text{(eq. 7)}$$

If a 5 kW power loss is assumed during avalanche, the resulting junction temperature rise will be

$$\Delta T = 5\ kW \times 0.00274\ ^\circ C/W = 13.7\ ^\circ C \quad \text{(eq. 8)}$$

This is an additional junction temperature rise caused by avalanche. Therefore, the system designer should first calculate the junction temperature of a normal operation, and then add the above value to obtain the transient junction temperature during avalanche. This temperature should be kept below the maximum allowable junction temperature with some safety margin according to the designer's choice.

5. Conclusions

The system designers are frequently forced to determine the applicability of a Power MOSFET to their application. This can be done by using the avalanche mode analysis and/or junction temperature analysis which are very practical.

References

[1] "Single Pulse Unclamped Inductive Switching: A Rating System", **onsemi** Application Note AN-7514

[2] "A Combined Single Pulse and Repetitive UIS Rating System", **onsemi** Application Note AN-7515

[3] Rudy Severns, 1984, "Safe Operating Area and Thermal Design for MOSPOWER Transistors", MOSPOWER Applications Handbook, Siliconix

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