# AN-8102/D

# Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

## INTRODUCTION

The High−Voltage Integrated Circuit (HVIC) gate driver family is designed to drive an N−channel MOSFET or IGBT up to 600 V. One of the most common methods to supply power to the high−side gate drive circuitry of the high−voltage gate drive IC is the bootstrap power supply. This bootstrap power supply technique has the advantage of being simple and low cost. However, duty cycle is limited by the requirement to charge the bootstrap capacitor and serious problems occur when extremely short pulse width is used in the application system. This application note explains the features of HVIC gate drivers and provides recommendations to avoid short pulse−width issues in the application.

In the HVIC gate driver block diagram shown in Figure1, a typical HVIC gate driver consists of input, pulse generator, level shifter, Under−Voltage Lockout (UVLO), control latch, and driver circuit. HVIC gate driver IC uses bootstrap method to control MOSFET and IGBT. By adding a bootstrap circuit outside the HVIC, the high side can be supplied with a signal power source. This kind of “floating supply” is suitable for providing gate drive circuitry to directly drive high−side switches that operate up to rail voltages. The basic application circuit of the bootstrap supply, shown in Figure 2, is comprised of bootstrap diode (D1) and capacitor (C1).

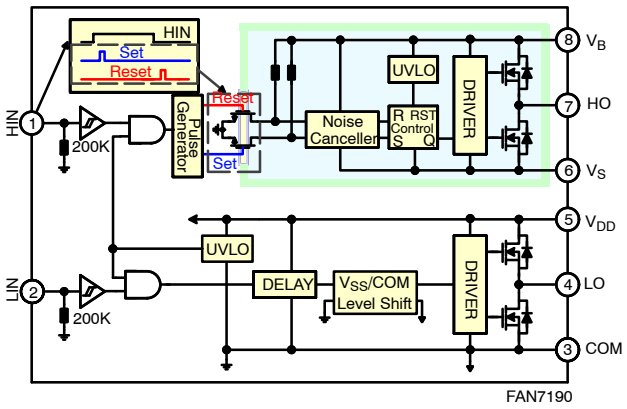


**Figure 1. Block Diagram of High−Voltage Gate Driver IC**

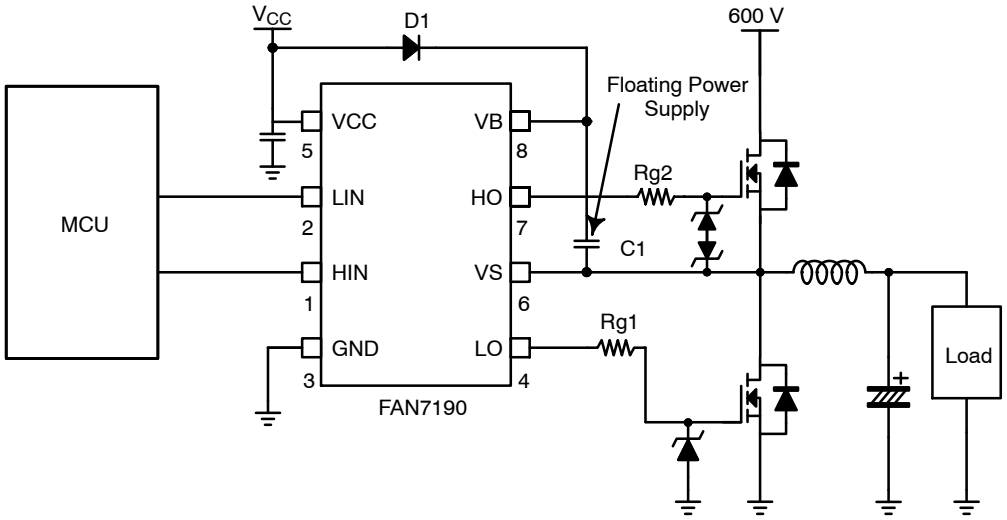


**Figure 2. Typical Application Circuit for FAN7190**

## OPERATION MODES AND AVOIDING POTENTIAL APPLICATION ISSUES

This section discusses three operation condition: normal, missing output, and abnormal.

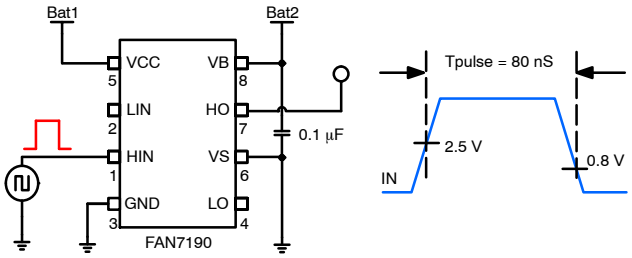


**Figure 3. Evaluation Circuit for HVIC Gate Driver IC**

Latch−on can result in keeping the status of output HIGH even if input is LOW. This condition leads to shoot−through when HO and LO are turned on at the same time. This failure mode is the worst case and is discussed in the “Abnormal Output Operating Condition” section.

### Normal Output Operating Condition

As shown in Figure 4, the SET and RESET pulse is generated from the pulse generator according to input edge because the power dissipation of R1 and R2 should be large in case $V_B$ is 600 V. That is why short pulse SET and RESET is used to reduce power consumption and power dissipation and size of R1 and R2.

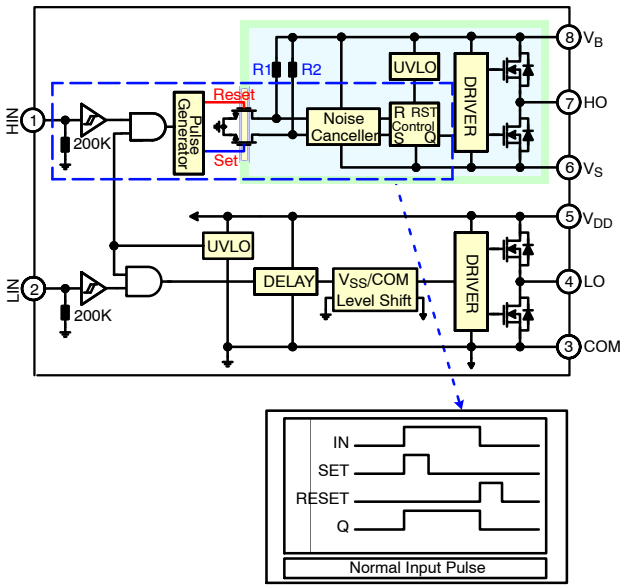


**Figure 4. Normal Operating Simulation Result**

The set and reset signal is delivered to set and reset latch (control latch) circuit through the level−shifter circuit between the low−voltage circuit and high−voltage circuit.

The control latch circuit keeps output status according to the SET and RESET pulse signal. The control latch circuit turns the output circuit on and off and output is generated. That complex circuit creates the propagation delay between input and output.

### Missing Output Operating Condition

Missing output means HO is not generated even though input signal is provided to HIN. Although the pulse generator generates both SET and RESET pulses according to input signal, the reconstructed signal by control latch circuit is too short and is filtered by parasitic RC filter in RRS latch output circuit. The control latch output signal is not delivered to the next driver circuit, shown in Figure 5.

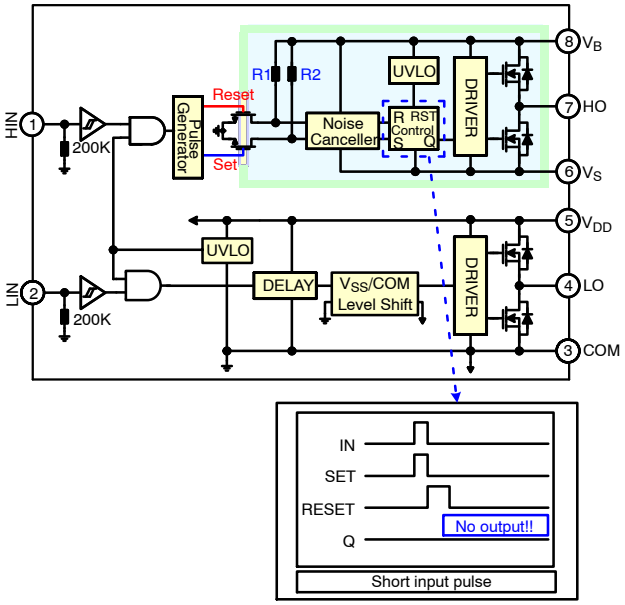


**Figure 5. Missing Output Operating Simulation Result**

Missing output range is from 30 ns to 50 ns at 25°C. With temperature increasing, the missing output range is shifted up to around 58 ns, as shown in Figure 7. The short pulse width, where the missing−operation condition occurs, is also shifted according to temperature, as shown in Figure 7.

The output is LOW when input pulse width between 39 ns and 58 ns is provided to input pin.

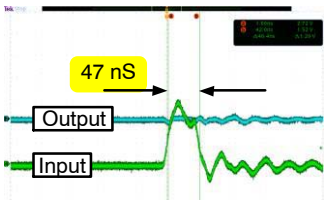


**Figure 6. No Output Operating Waveform**

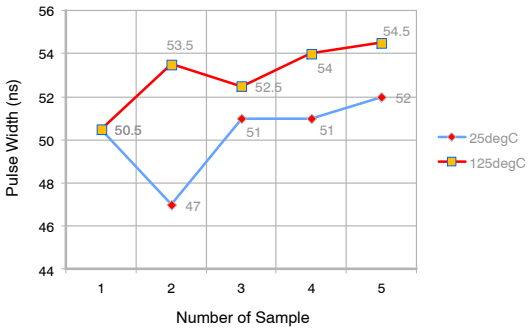


**Figure 7. No Output Range According by Temperature**

### Abnormal Output Operating Condition

The output of HVIC shows latch−on when the input pulse width between 19 ns and 37 ns is extremely short.

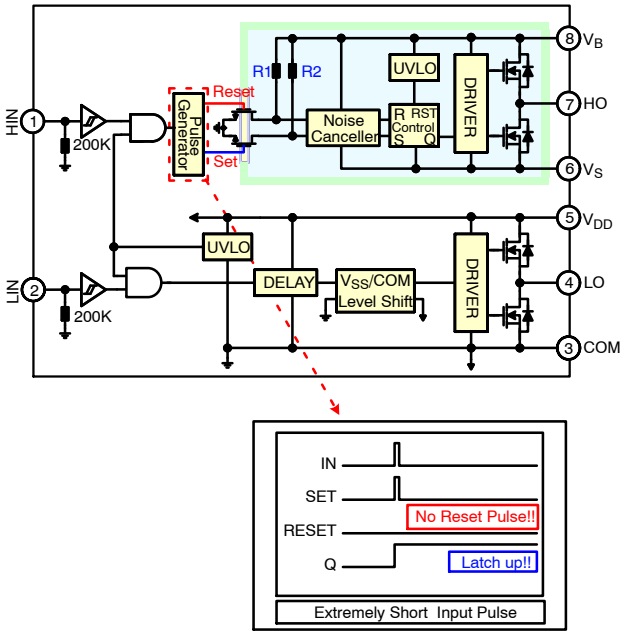


**Figure 8. Abnormal Operation Simulation Result**

The pulse generator cannot generate a RESET pulse when input pulse width is extremely short, while SET is generated.

The falling edge of input is filtered by an internal parasitic circuit in case of extremely short pulse width; the output of HVIC shows latch−on , as shown in Figure 8 and Figure 9.

Pulse width of 24 ns at 25°C causes abnormal output condition, as shown in Figure 9. Output is turned off by the next input pulse. Pulse width of around 24 ns is the boundary line of abnormal output operating condition.

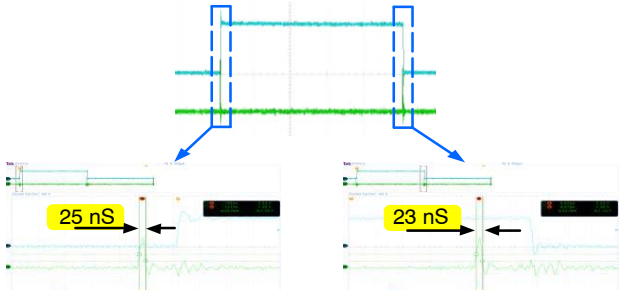


**Figure 9. Abnormal Output Operation Waveform**

In half−bridge topology, a short−circuit condition can occur that leads to shoot−through when HO and LO are turned on at the same time. This failure mode should be taken into consideration in all mission−critical designs. Short pulse width abnormal condition is shifted according to temperature, as shown in Figure 10. Because the RC filter constant is changed if $R_{ON}$ of the internal MOSFET is increased according to temperature, a minimum short pulse width is recommended to avoid malfunction.

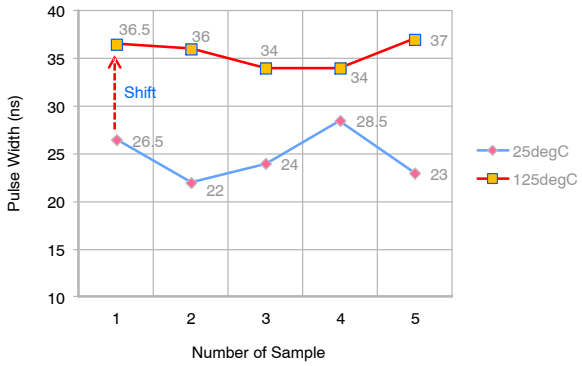


**Figure 10. Abnormal Output Range by Temperature**

Minimum short pulse width is around 60 ns from −40 to 125°C. Taking tolerance of the device into account with 40% margin results in a recommend minimum pulse width as below:

- Minimum pulse width: 54.5 ns at 125°C x 1.4 times = around 77 ns
- Recommended minimum pulse width is 77 ns from −40 to 125°C

### Different Types of Pulses

Short input pulses can be:

- turn on pulses, i.e. rising edge to the adjacent falling edge (see example Figure 11)
- turn off pulses i.e., falling edge to the adjacent rising edge (see example Figure 12)
- also parasitic pulses induced by noise

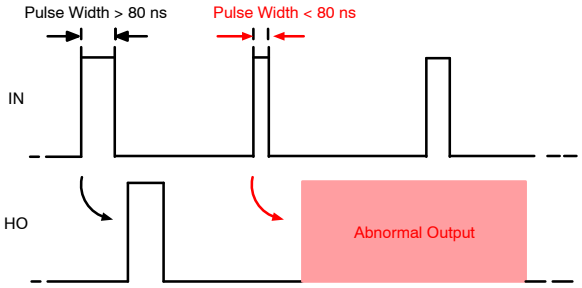


**Figure 11. Output Waveform with Short Turn On Input Pulse Width**

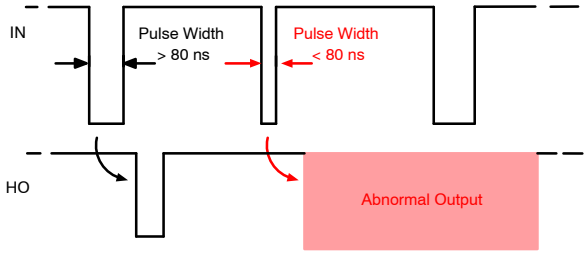


**Figure 12. Output Waveform with Short Turn Off Input Pulse Width**

## ASYNCHRONOUS GATING ISSUES

In some applications, an unwanted short pulse can be generated by the external circuit and cause potential failure modes in the HVIC.

If the source of the PWM signal is a free−running generator (e.g., voltage−controlled PWM or similar concept), as shown in the Figure 13, HIN could be the sort pulse at certain times in the PWM cycle, as shown in the Figure 14.

An external AND gate can cause a short pulse on both the rising and falling edges because the ENABLE signal is not sychronized with the PWM signal. In this case, the solution is to generate the PWM with an MCU with internal hardware with a synchronous ON/OFF feature.

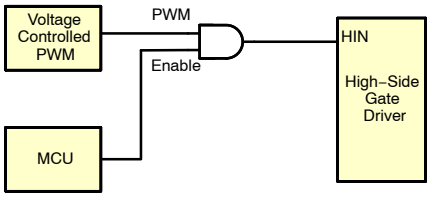


**Figure 13. Asynchronous Gating Diagram**

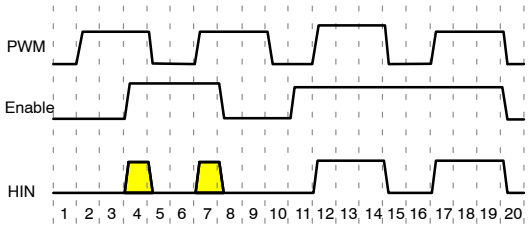


**Figure 14. Timing Diagram Showing Short Pulses**

Because this is an issue even when using gate driver products with a built−in enable pin, the PWM should be OFF before changing the status of the enable pin.

## CONCLUSION

This application note discusses operation and potential failure modes of HVIC gate drivers. A minimum pulse width is recommended to prevent abnormal conditions.

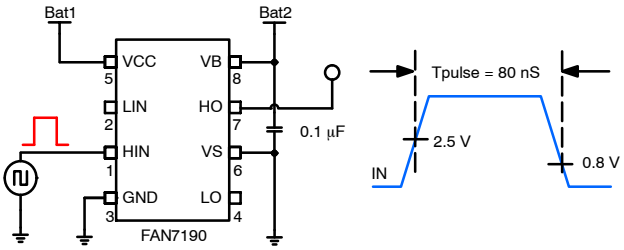


**Figure 15. Short Pulse Width Test Circuit and Pulse Width Waveform**

A short pulse−width test circuit and pulse width waveform are shown in Figure 15. The timing diagram in Figure 16 shows latch−on and missing output range from 25°C to 125°C temperature.

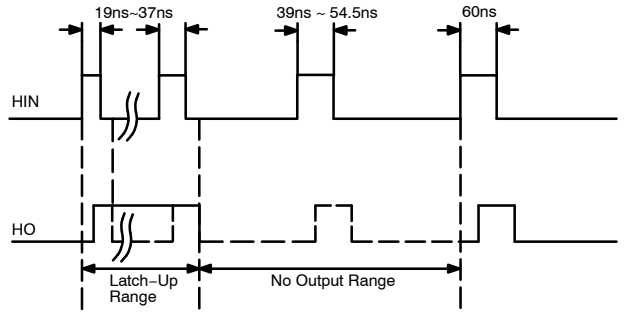


**Figure 16. Timing Diagram Input vs. Output**

Normal output signal occurs from 60 ns at 125°C. Take the worst−case into consideration and give 40% margin for minimum pulse width. Minimum Pulse Width: 54.5 ns at 125°C x 1.4 times = around 77 ns.

The best solution to address minimum short pulse width issues is determined by the requirements of each application. Each HVIC minimum short pulse width limit is different because internal circuit and layout are different.

For example; if the HVIC has half−bridge structure with one input (e.g., FAN7393), recommended minimum short pulse width should be 30% longer than dead time. In this case, effective short pulse width can be counted after it exceeds the dead time specified in the datasheet *(refer to Table 1)*.

**Table 1. MINIMUM SHORT−PULSE WIDTH**

| Feature | | | Recommended Min. Short Pulse Width |
|---|---|---|---|
| Input Channel | Output Channel | Topology | |
| 1 | 1 | High−Side Only | 77 ns |
| 2 | 2 | Half−Bridge | 2 × DT |
| 2 | 2 | High- & Low−Side, Dual High Side | 77ns |
| 6 | 6 | 3−Phase Half−Bridge | 77 ns |
| 1 | 2 | Half−Bridge | 2 × DT |

1. DT is dead time which is referenced to typical value specified in datasheet.
2. Recommended min. short pulse width reflects temperature dependency and the variation between setting and real dead time.
3. Some HVIC have built−in advanced input filter to prevent potential failure mode regarding short pulse input.

For more details, please refer to the corresponding HVIC datasheet. Minimum pulse time depends on internal parasitic RC time constants.

### References

[1] AN−6076 — Design and Application Guide of bootstrap Circuit for High−Voltage Gate Driver IC
[2] AN−9052 — Design Guide for Selection of Bootstrap Components

### Related Datasheets

- FAN7080−GF085 Half−Bridge Gate Driver
- FAN7081−GF085 High Side Gate Driver
- FAN7083−GF085 High Side Gate Driver with Reset
- FAN7085−GF085 High Side Gate Driver with Recharge FET
- FAN7171−F085 High−Current, High Side, Gate−Drive IC
- FAN7190−F085 High−Current, High & Low−Side, Gate−Drive IC
- FAN7361 — High−Side Gate−Driver IC
- FAN73611 — High−Side Gate−Driver IC
- FAN7362 — High−Side Gate−Driver IC
- FAN7371 — High−Current, High−Side Gate−Driver IC
- FAN73711 — High−Current, High−Side Gate−Driver IC
- FAN7380 — Half−Bridge Gate−Driver IC
- FAN7382 — High & Low−Side Gate−Driver IC
- FAN7383 — Half−Bridge Gate−Driver IC
- FAN73832 — Half−Bridge Gate−Driver IC
- FAN73833 — Half−Bridge Gate−Driver IC
- FAN7384 — Half−Bridge Gate−Driver IC
- FAN7385 — Dual−Channel High−Side Gate−Driver IC
- FAN7388 — 3−Phase Half−Bridge Gate−Driver IC
- FAN7390 — High−Current, High & Low−Side Gate−Driver IC
- FAN7390A — High−Current, High & Low−Side Gate−Driver IC
- FAN73901 — High & Low−Side Gate−Driver IC
- FAN7392 — High−Current, High & Low−Side Gate−Driver IC
- FAN7393 — Half−Bridge Gate−Driver IC
- FAN7393A — Half−Bridge Gate−Driver IC
- FAN73932 — Half−Bridge Gate−Driver IC
- FAN73933 — Half−Bridge Gate−Driver IC
- FAN7842 — High & Low−Side Gate−Driver IC
- FAN7888 — 3−Phase Half−Bridge Gate−Driver IC



**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative