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# AN-7733
# FL7732 Design Tool Flow (Buck Boost)

## Overview

This document is intended to provide in-depth guidance to using the Fairchild Design Tool for FL7732 in a boost buck topology. Use the Design Tool with the product datasheet.

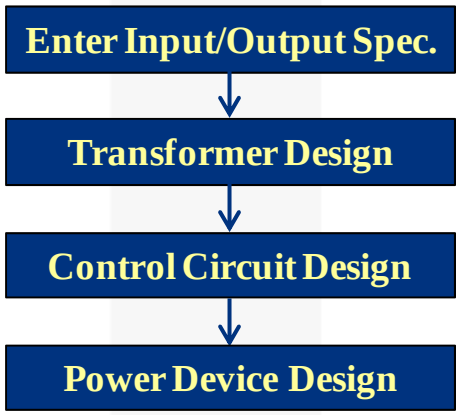
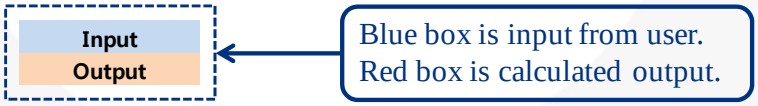



**Figure 1. Design Flow**

## Step 1 — Enter Input Output Specification




| Input & Output Spec | | |
|---|---|---|
| Min. Vin | 198 | Vac |
| Max. Vin | 264 | Vac |
| Vout | 100 | V |
| Max. Vout | 120 | V |
| Iout | 125 | mA |
| Pout | 12.500 | W |

Max. Vout is OVP level.

## Step 2 — Transformer Design

| Transformer Design | | |
|---|---|---|
| Max. Duty | 26 | % |
| Max. Ton | 4.727 | us |
| Switching freq. | 55 | kHz |
| Efficiency | 85 | % |
| Ae | 36.6 | $mm^2$ |
| Bmax | 0.25 | |
| Lm | 1.638 | mH |
| Np.min | 144.667 | T |
| Np | 145 | T |
| Na | 27.792 | T |
| Nap | 0.192 | |
| Vcs.max | 0.616 | V |
| Ts | 18.182 | us |
| Ton+Tdis | 17.964 | us |

Max. duty is generally between 20 ~ 50%.
High max. duty → Low conduction loss, Suitable for low-line
Low max. duty → More Bmax margin, Suitable for high-line

Max. $t_{on}$ should be less than 10μs.

This switching frequency is the operating frequency at the rated $V_{OUT}$ condition. The switching frequency should be <65kHz.

Enter Np over Np.min.
If Np is too big to fit in transformer window, reduce Max. Duty.

Pulse-by-pulse current limit is 0.67V.
If $V_{CS.MAX}$ is too close to 0.67V, increase Max. Duty.

$t_{DIS}$ means secondary diode conduction time at peak input voltage. If $t_{ON}+t_{DIS}$ s longer than $t_S$, CRM is shown at peak input voltage area. To operate only in DCM, $t_{ON}+t_{DIS}$ should be less than $t_S$. To make " $t_{ON}+t_{DIS} < t_S$ ", decrease Max. Duty

## Step 3 — Control Circuit Design

| Control Circuit Design | | |
|---|---|---|
| Rsense | 0.762 | ohm |
| Vin.bnk | 50 | V |
| Vf | 0.5 | V |
| Rvs1 | 137.631 | kohm |
| Rvs2 | 15.839 | kohm |
| Cvs | 10 | pF |
| Ccomi | 1 | uF |
| Cvdd | 33 | uF |
| Dvdd Vmax | 95.059 | V |
| Rstr | 342.857 | kohm |
| Rdummy | 400.000 | kohm |

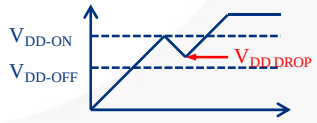
$V_{IN.BNK}$ is $V_S$ blanking level.
$V_S$ blanking : $V_S$ voltage detection is disabled.
$V_{IN.BNK}$ is generally set as 30~70V.

$V_f$ is secondary diode forward voltage.

$C_{VS}$ is $V_S$ filter capacitor, generally set as 10~30pF.

COMI capacitor is generally 0.68~3.3μF.
Check output voltage overshoot at startup in max. $V_{IN}$ condition.
If output voltage overshoot is too big, increase $C_{COMI}$.

$V_{DD}$ capacitor is generally in 10~47μF.
If $V_{DD}$ drops too close to $V_{DD-OFF}$ at startup, increase $C_{VDD}$.




$R_{DUMMY}$ helps to maintain over -voltage level at open-LED condition. If output OVP is good, try to increase $R_{DUMMY}$ to maximize efficiency.

## Step 4 — Power Device Design

| Power Device Design | | |
|---|---|---|
| SW/Dout Vmax | 493.352 | V |
| SW/Dout Ipk | 0.808 | A |
| Inductor Irms | 0.282 | A |

$V_{MAX}$ is maximum voltage of MOSFET drain-source and output rectifier.

$I_{PK}$ is peak current of MOSFET and output rectifier.

## Related Resources

Locate the Design Tool at:

*http://www.fairchildsemi.com/design_tools/led-driver-design-tool/*

Consult the product datasheet at:

*FL7732 —Single-Stage PFC Primary-Side-Regulation Offline LED Driver*

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