APPLICATION NOTE
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Single-Pulse Unclamped Inductive Switching: A Rating System

AN-7514/D

Summary

Unexpected transients in electrical circuits are a fact of life. The most potentially damaging transients enter a circuit on the power source lines feeding the circuit. Power control and conversion circuits are vulnerable because of their close proximity to the incoming lines. The circuit designer must provide protection or face frequent field failures. **onsemi** offers power MOSFET devices that are avalanche−failureresistant. Some semiconductor devices are intolerant of voltage transients in excess of their breakdown rating. Avalanche−capable devices are designed to be robust. The **onsemi**'s POWERTRENCH® product line typifies rugged power devices. To assist the designer in their use, **onsemi** has devised an application−specific rating. This application note is intended to explain and illustrate the use of the single−pulse Unclamped Inductive Switching (UIS) rating curves.

Failure Mechanisms

Early power MOSFET devices, not designed to be rugged, failed when the parasitic bipolar transistor indigenous to the vertical DMOS process turned on. Figure 1 is a cross−section of a unit cell from an N−channel enhancement mode device.

When a unit is in avalanche, the bipolar transistor is in a V_{CER} mode and heats rapidly. The avalanche−induced base−emitter voltage rises because of a positive resistive temperature coefficient. Simultaneously, the base emitter voltage, where the transistor becomes forward biased, decreases because of its negative temperature coefficient. If a forward−bias condition is reached, device failure occurs. Blackburn's[1] measurements showed that this failure mode is a function of avalanche current and junction temperature; it is not energy related.

Ruggedness improvement technology has advanced to such a level that devices fail via a different mechanism. Devices are being designed and manufactured in which the parasitic bipolar turn−on is effectively suppressed. Device failure is thermally induced and current is distributed uniformly across the die. In this case, the failure occurs because the device junction temperature reaches the point at which the thermally generated carrier concentration (in the n− region) becomes comparable to the background doping (also in the n− region). At this point, the effective charge (sum of the fixed charge from the doping concentration plus the thermally generated carriers) in the epi layer becomes too large to support the applied voltage.

onsemi's POWERTRENCH® MOSFET families epitomizes devices having UIS robustness. UIS capability testing of these devices shows that the failure current versus the time in avalanche closely approximates a negative one−half slope when the locus of device destruction point is plotted on a log−log graph. Device failure is not inversely proportional to current only, as it would be in the case of constant energy. **onsemi** supplies rating curves at starting junction temperatures of 25°C and 150°C *(see Figure 2)*.

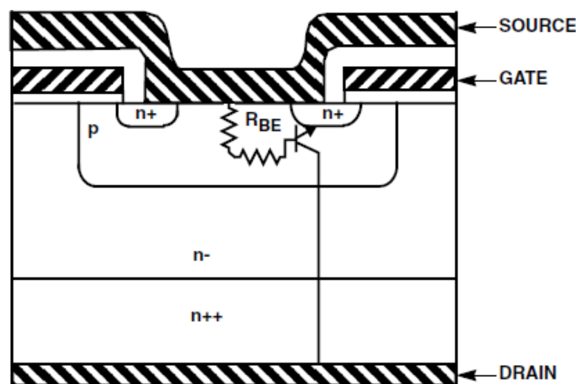

Figure 1. VDMOS Structure with Parasitic Bipolar Transistor

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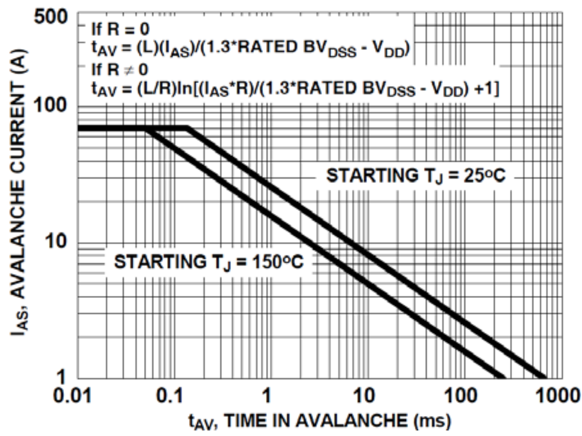

Figure 2. FDB8444 Unclamped−Inductive−Switching Safer Operating Area Curve (Single−Pulse UIS SOA)

Test Circuit Equations

The circuit model *(see Figure 3)* used to describe a UIS test is a simple, lumped parameter series inductor / resistor circuit in which both the power supply and device avalanche voltage are presumed to be constant. All the equations that result from the mathematical analysis are listed in Table 1 by the V_{DD}; R conditions commonly referenced in the test method and commercial datasheets. The equations in row 1 are for the general case. The factor K is the ratio of the net voltage across the inductor and resistor to the resistor voltage drop. When K is large (K >30), the equations in row 1 reduce to those in rows 2 and 3. This can be accomplished mathematically by substituting the series expansion: ln (1+X) = X−X2/2+. Only the first term is needed for t_{AV}, while two terms are required for E_{AS} and $P_{AS(AVE)}$. Time in avalanche, t_{AV}, is the important parameter for a rugged device. Reviewing the expressions for t_{AV} in Table 1, the following observations can be made:

- Series circuit resistance reduces the device avalanche stress.
- A supply voltage approaching the device avalanche voltage increases t_{AV}. Stress increases and the allowable avalanche current is reduced.
- When the supply voltage is zero, t_{AV} varies inversely with the device avalanche voltage.

The equations of Table 1 presume that the device avalanche voltage is constant. In an actual test, it is not. Experiments have been performed using devices with similar low−current room temperature BV_{DSS} readings. V_{DD}, L, R, I_{AS}, and t_{AV} were carefully measured and the avalanche breakdown was calculated. All units yielded similar results. The effective avalanche voltage in all cases was 30% larger than BV_{DSS} when avalanched near rated capability *(see Figure 5 and Figure 6)*. $V_{DSX(SUS)}$ is the effective voltage referenced in the JEDEC test method[2]. **onsemi** has chosen to list $V_{DSX(SUS)}$ in the t_{AV} equations on the rating curves for these devices as 1.3 times the rated low−current breakdown voltage.

- I_{AS} − peak current reached during device avalanche
- t_{AV} − time duration of device avalanche
- $V_{DSX(SUS)}$ − effective (constant) device breakdown voltage during avalanche (approximately $1.3 \cdot BV_{DSS}$)
- L − Inductance
- R − Resistance
- V_{DD} − output circuit supply voltage
- K − ($V_{DSX(SUS)}$−V_{DD})/(I_{AS}R) − ratio of the inductor plus the resistor voltage to the resistor voltage drop

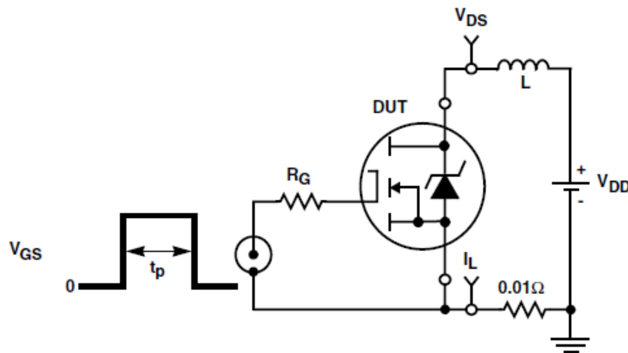

Figure 3. UIS Test Circuit

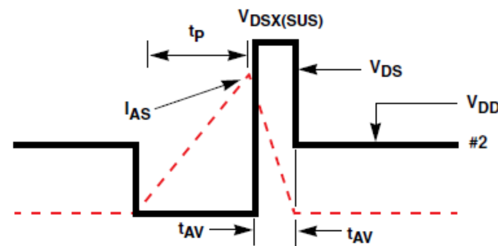

Figure 4. UIS Waveforms

Table 1. MATHEMATICAL ANALYSIS

Row #	Circuit Condition		Time in Avalanche	Avalanche Energy	Average Avalanche Power
	V_{DD}	R	t_{AV}	E_{AS}	$P_{AS(AVE)} = (E_{AS}/t_{rep}),\ t_{rep} \geq t_{AV}$
1	V_{DD}	R	$(L/R)\ln(1+1/K)$	$(LI_{AS}V_{DSX(SUS)}/R)[1-K\ln(1+1/K)]$	$[I_{AS}V_{DSX(SUS)}]\cdot[(1/\ln(1+1/K))-K)(t_{AV}/t_{rep})$
2	V_{DD}	0	$LI_{AS}/(V_{DSX(SUS)}-V_{DD})$	$LI_{AS}^2/[2(1-V_{DD}/V_{DSX(SUS)})]$	$(I_{AS}V_{DSX(SUS)}/2)(t_{AV}/t_{rep})$
3	0	0	$LI_{AS}/V_{DSX(SUS)}$	$LI_{AS}^2/2$	$(I_{AS}V_{DSX(SUS)}/2)(t_{AV}/t_{rep})$

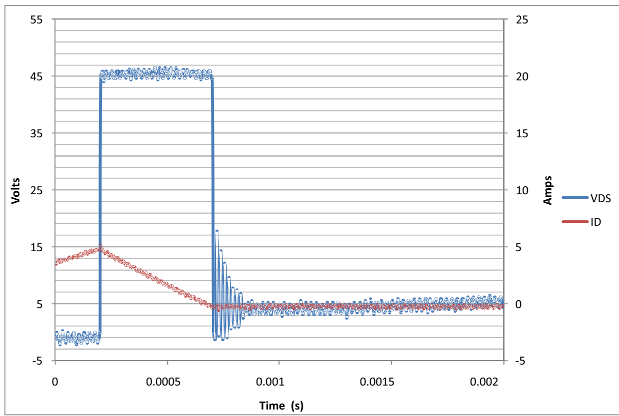

Figure 5. FDB8444 $V_{DSX(SUS)}$, L = 5 mH, I_{AS} = 5 A, Initial T_J = 25°C

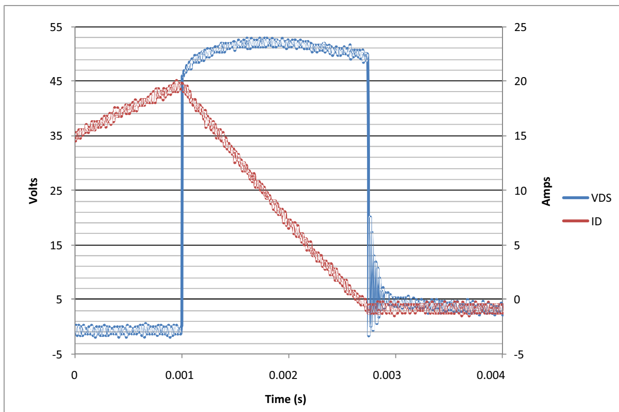

Figure 6. $V_{DSX(SUS)}$, L = 5 mH, I_{AS} = 20 A, Initial T_J = 25°C

Single−point avalanche−energy ratings at T_J = 25°C are not application specific nor are they useful for comparing similar devices offered by different manufacturers. To highlight the difficulty, a hypothetical example is in order.

Application Example: Operating Margin for a Single−Pulse UIS Event

Determine the safe single−pulse avalanche current for an application that uses L = 1 mH and V_{DD} = 0 V for **onsemi**'s FDB8444. Datasheet information is as follows (reference the UIS rating curve in Figure 2):

E_{AS} = 307 mJ Maximum

T_J = 25°C (Starting)

BV_{DSS} = 40 V

L = 200 μH

V_{DD} = 0 V during avalanche

I_{AS} = 56 A (Effective I_{AS} calculates to 55.4 A because $R \neq 0\ \Omega$ and a non−constant $V_{DSX(SUS)}$ as a result of self−heating, *(see Figure 5)*

t_{AV} = 477 μs (calculated using effective I_{AS} = 55.4 A)

Only a starting junction temperature of 25°C can be assessed. For a starting temperature other than that described in **onsemi** datasheets (usually 25°C and 150°C), additional analysis is required to extrapolate the duration and amplitude limits of the avalanche event.

Parasitic Bipolar Turn−on

Assuming the parasitic bipolar transistor is suppressed, it need not be considered for state−of−the−art devices.

Constant Energy

To use the relationship $E_{AS} = L\, I^2_{AS}/(2(1-V_{DD}/V_{DSX(SUS)}))$, use $V_{DSX(SUS)} = 1.3 \cdot BV_{DSS}$. For a constant energy of 307 mJ, the predicted safe I_{AS} (for L = 1 mH) would equal 24.8 A (t_{AV} = 477 μs). This data point is located beneath the 25°C Figure 2 UIS rating curve.

Thermal ($I^2_{AS}\, t_{AV}$ = Constant)

T_{JS} = 25°C

Again using $V_{DSX(SUS)} = 1.3 \cdot BV_{DSS}$ in the relationship $t_{AV} = L\, I_{AS}/(V_{DSX(SUS)}-V_{DD})$ for the intended application (L = 1 mH), predicted t_{AV} and I_{AS} are:

$I^3_{AS} = 0.654\ (V_{DSX(SUS)}-V_{DD})/L$

where:

L = 1 mH

V_{DD} = 0 V

$V_{DSX(SUS)} = 1.3 \cdot BV_{DSS}$

t_{AV} = 623 μs, and

I_{AS} = 32.4 A.

It is a simple matter to establish the safe avalanche current for an **onsemi** POWERTRENCH® devise when supplied with rating curves.

T_{JS} = 150°C

Datasheet $I^2_{AS}\, t_{AV}$ = 0.25. At the maximum rated starting junction temperature, t_{AV} = 452 μs and I_{AS} = 23.5 A. The safe avalanche current for any starting T_J can be established from the **onsemi** rating curves. Stoltenburg[3] showed that for avalanche−rated devices, avalanche failure was a linear function of starting T_J for a fixed inductor. This is also true for a constant t_{AV}. It is a simple matter then to establish the $I^2_{AS}\, t_{AV}$ = constant for any starting T_J. T_{JS} = 100°C is a common operating temperature for a practical application.

Entering the **onsemi** curves at any convenient t_{AV}, in this case; 0.6 ms; the I_{AS} temperature sensitivity is (20 A−33 A)/+125°C or −104 mA/°C. Therefore, I_{AS} = 33−(0.104)(100°C−25°C) = 25.2 A for t_{AV} = 0.6 ms and $I^2_{AS}\, t_{AV}$ = 0.381.

For the example application where L = 1 mH, using $I^3_{AS} = 0.381\ (V_{DSX(SUS)}-V_{DD})/L$; a maximum avalanche current of I_{AS} = 27.1 A for a starting T_J = 100°C.

Related Datasheets

*For **onsemi** documents available on the internet, see website https://www.onsemi.com*

[1] D. L. Blackburn, *"Power MOSFET Failure Revisited"*, Proc. 1988 IEEE Power Electronics Specialists Conference, pp 681−688, April 1988.

[2] *"Single−Pulse Unclamped Inductive Switching (UIS) Avalanche Test Method",* JEDEC Standard JESD24−5, October 2002.

[3] Rodney R. Stoltenburg, "*Boundary of Power−MOSFET, Unclamped Inductive−Switching (UIS) Avalanche−Current Capability"*, Proc. 1989 Applied Power Electronics Conference, pp 359−364, March 1989.

[4] Miroslav Glogolja, *"Ruggedness Test−Claims Demand Another Careful Look"*, Powertechnics Magazine, pp 23−28, July 1986.

[5] S. K. Ghandhi, *"Semiconductor Power Devices"*, John Wiley & Sons, New York, pp 15−29, 1977.

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