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AN-6920MR

Integrated Critical-Mode PFC / Quasi-Resonant Current-Mode PWM Controller FAN6920

1. Introduction

This application note presents practical step-by-step design considerations for a power supply system employing Fairchild's FAN6920 PFC / PWM combination controller, an integrated Boundary Conduction Mode (BCM) Power Factor Correction (PFC) controller and Quasi-Resonant (QR) PWM controller. Figure 1 shows the typical application circuit, where the BCM PFC converter is in the front end and the dual-switch quasi-resonant flyback converter is in the back end.

FAN6920 achieves high efficiency with relatively low cost for 75~200 W applications where BCM and QR operation with a two-switch flyback provides best performance. A BCM boost PFC converter can achieve better efficiency with lower cost than continuous conduction mode (CCM) boost PFC converter. These benefits result from the elimination of the reverse-recovery losses of the boost diode and zero-voltage switching (ZVS) or near ZVS (also called valley switching) of boost switch. The dual-switch QR flyback converter for the DC-DC conversion achieves higher efficiency than the conventional flyback converter with leakage inductor energy recycles.

The FAN7382, a monolithic high- and low-side gate-driver IC, can drive MOSFETs that operate up to +600 V.

Efficiency can be further improved by using synchronous rectification in the secondary side instead of a conventional rectifier diode.

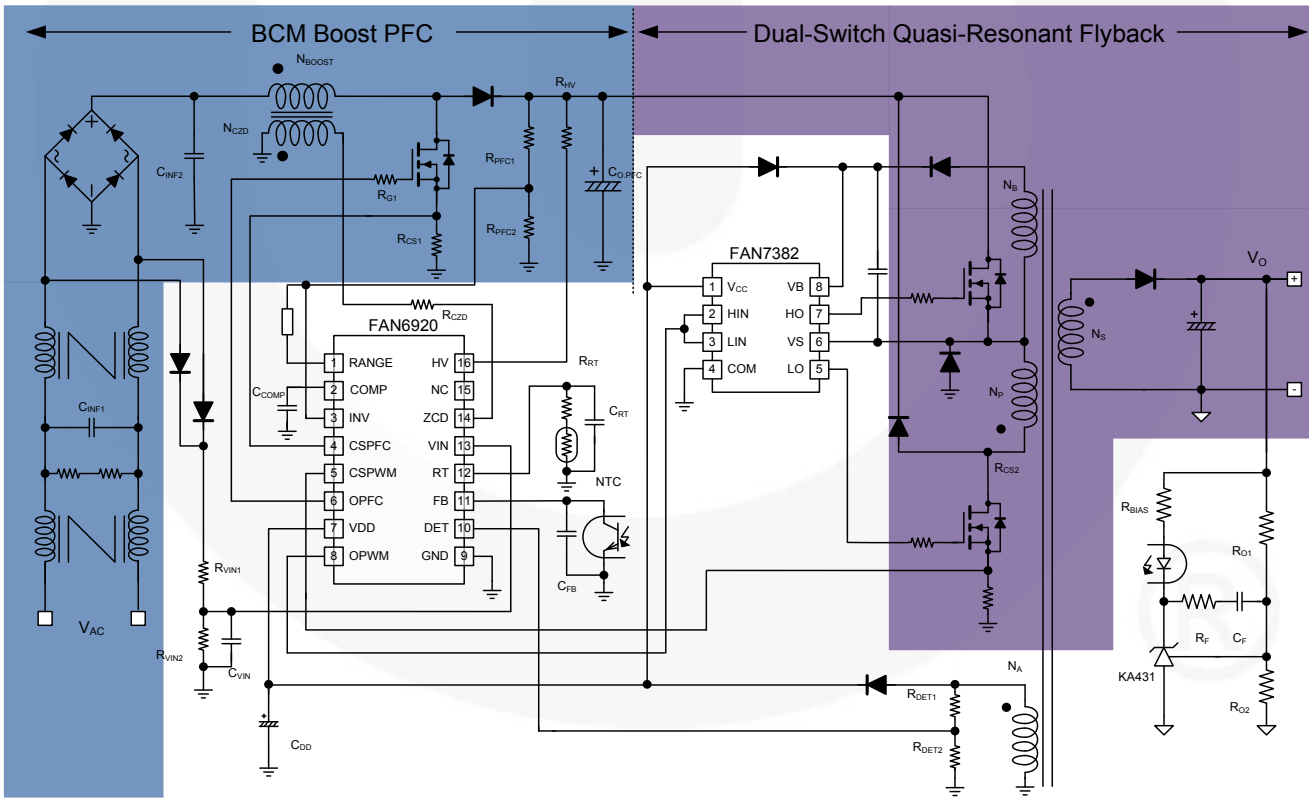

Figure 1. Typical Application Circuit

2. Operation Principles of BCM Boost PFC Converters

The most widely used operation modes for the boost converter are continuous conduction mode (CCM) and boundary conduction mode (BCM). These refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. As the names indicate, the inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. Even though the BCM operation has higher RMS current in the inductor and switching devices, it allows better switching condition for the MOSFET and the diode. As shown in Figure 2, the diode reverse recovery is eliminated and a fast silicon carbide (SiC) diode is not needed. MOSFET is also turned on with zero current, which reduces switching loss.

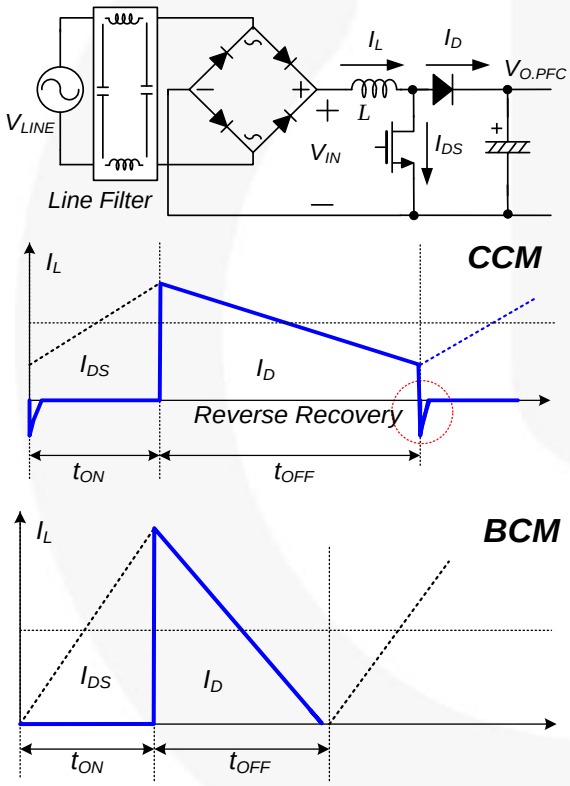

Figure 2. CCM vs. BCM Control

The fundamental idea of BCM PFC is that the inductor current starts from zero in each switching period, as shown in Figure 3. When the power transistor of the boost converter is turned on for a fixed time, the peak inductor current is proportional to the input voltage. Since the current waveform is triangular, the average value in each switching period is also proportional to the input voltage. In the case of a sinusoidal input voltage, the input current of the converter follows the input voltage waveform with a very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation an ideal candidate for power factor correction.

A by-product of the BCM is that the boost converter runs with variable switching frequency that depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input current follows the sinusoidal input voltage waveform, as shown in Figure 3. The lowest frequency occurs at the peak of sinusoidal line voltage.

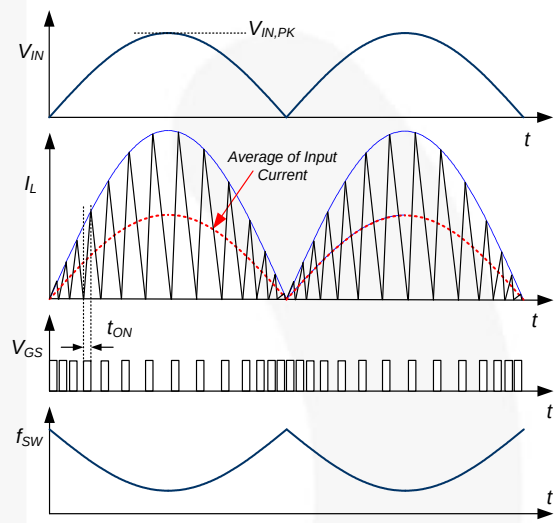

Figure 3. Operation Waveforms of BCM PFC

The voltage-second balance equation for the inductor is:

$$V_{IN}(t)\cdot t_{ON} = (V_{O.PFC} - V_{IN}(t))\cdot t_{OFF} \quad (1)$$

where $V_{IN}(t)$ is the rectified line voltage.

The switching frequency of BCM boost PFC converter is obtained as:

$$f_{SW} = \frac{1}{t_{ON}+t_{OFF}} = \frac{1}{t_{ON}}\cdot\frac{V_{O.PFC}-V_{IN}(t)}{V_{OUT}} = \frac{1}{t_{ON}}\cdot\frac{V_{O.PFC}-V_{IN,PK}\cdot|\sin(2\pi f_{LINE}t)|}{V_{O.PFC}} \quad (2)$$

where $V_{IN,PK}$ is the amplitude of the line voltage and f_{LINE} is the line frequency.

Figure 4 shows how the MOSFET on time and switching frequency change as output power decreases. When the load decreases, as shown in the right side of Figure 4, the peak inductor current diminishes with reduced MOSFET on time and the switching frequency increases.

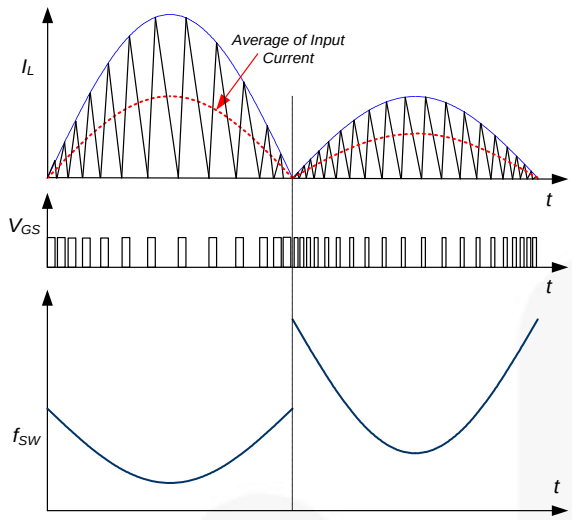

Figure 4. Frequency Variation of BCM PFC

Since the design of line filter and inductor for a BCM PFC converter with variable switching frequency should be at minimum frequency condition, it is worthwhile to examine how the minimum frequency of BCM PFC converter changes with operating conditions.

Figure 5 shows the minimum switching frequency, which occurs at the peak of line voltage, as a function of the RMS line voltage for different output voltage settings. For universal line application, the minimum switching frequency occurs at high line (265 V_{AC}) as long as the output voltage is lower than about 405 V.

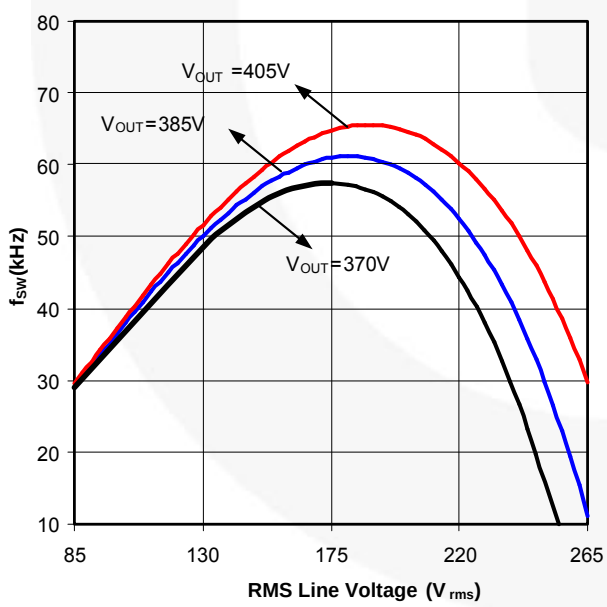

Figure 5. Minimum Switching Frequency vs. RMS Line Voltage (L = 780 µH, P_{OUT} = 100 W)

3. Operation Principle of Dual-Switch Quasi-Resonant (QR) Flyback Converter

The dual-switch QR flyback converter is derived from the conventional pulse-width modulated (PWM) flyback converter. With the recycling loop of the residual energy stored in leakage inductance, the primary-side snubber and its loss can be removed. This is especially suitable for high-power (up to 200 W) and slim-type applications. Figure 6 and Figure 7 show the simplified circuit diagrams of a dual-switch quasi-resonant flyback converter and its typical waveforms. The basic operation principles are:

- When primary power switches turn on, input voltage (V_{IN}) is applied across the primary-side inductor (L_m). MOSFET current (I_{DS}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.
- When the primary MOSFETs turn off, the leakage inductance energy generates voltage spikes on the drain-to-source voltage (V_{DS}) of MOSFETs. As soon as V_{DS} reaches V_{IN}, recycling diodes D1 and D2 are conducted and the residual energy is released to the input capacitor. As V_{DS} is lower than V_{IN}, the energy stored in the primary inductor forces the output rectifier (D3) to conduct. During the diode on time (t_D), the output voltage (V_o) is applied across the secondary-side inductor and the diode current (I_D) decreases linearly from the peak value to zero. At the end of t_D, all the energy stored in the inductor has been delivered to the output. During this period, the output voltage is reflected to the primary side as $V_o \times N_P/N_S$. The sum of input voltage (V_{IN}) and reflected output voltage ($V_o \times N_p/N_s$) is imposed across the MOSFETs.

  The voltage on the primary-side winding is clamped to V_{IN}. If the voltage of input is too low, the voltage of secondary side could be lower than output voltage target ($V_{IN} < N_P/N_S \times V_O$), and the output voltage would follow input voltage drop.
- When the inductor current reaches zero, the drain-to-source voltage (V_{DS}) begins to resonate by the resonance between the primary-side inductor (L_m) and the MOSFET output capacitor (C_{oss1}, C_{oss2}) with an amplitude of $V_o \times N_p/N_s$ on the offset of V_{IN}, as depicted in Figure 7. Quasi-resonant switching is achieved by turning on the MOSFET when V_{DS} reaches its minimum value. This reduces the MOSFET turn-on switching loss caused by the capacitance loading between the drain and source of the MOSFET.

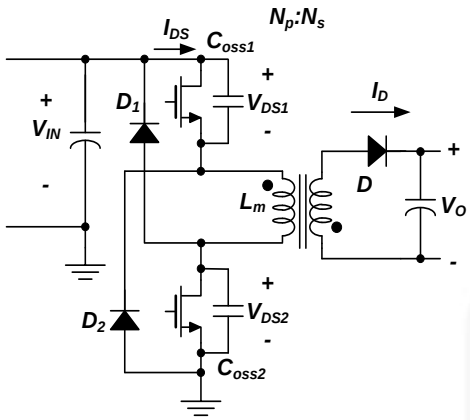

Figure 6. Schematic of Dual-Switch Flyback Converter

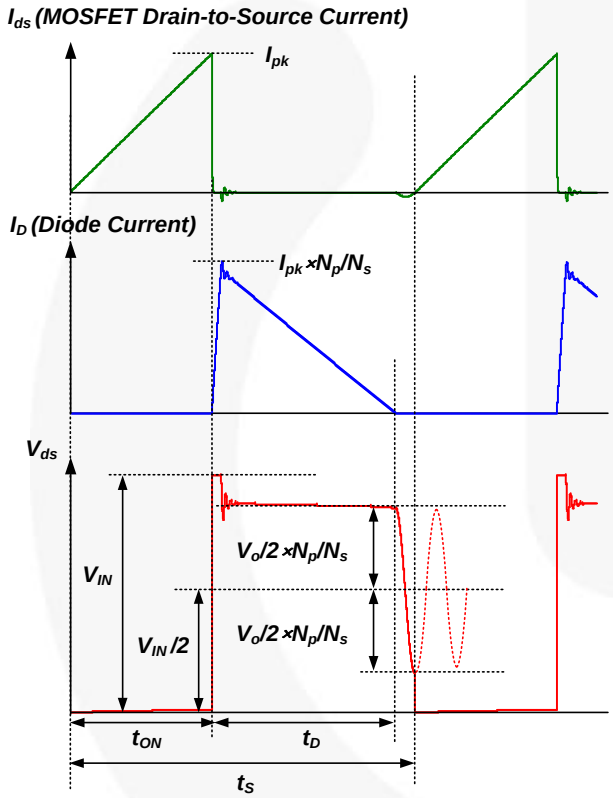

Figure 7. Typical Waveforms of Dual-Switch QR Flyback Converter

4. High-Side Gate-Drive Circuit

Figure 8 and Figure 9 show the high/low-side gate driver circuit. The high-side gate drive IC achieves high-performance, is simple and inexpensive, but has a limitation for dual-switch flyback application.

One of the most widely used methods to supply power to the high-side gate driver circuitry of the high-voltage gate-drive IC is the bootstrap power supply. This bootstrap power supply technique has the advantage of being simple and low cost. The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When the high-side V_S goes below the IC supply voltage V_{DD} or is pulled down to ground (the low-side switch is turned on and the high-side switch is turned off), the bootstrap capacitor, C_{BOOT}, charges through the transformer primary-side, from the V_{DD} power supply, as shown in Figure 8. This is provided by V_{BS} when high-side V_S is pulled to a higher voltage by the high-side switch. The V_{BS} supply floats and the bootstrap diode reverses bias and blocks the rail voltage (the low-side switch is turned off and high-side switch is turned on) from the IC supply voltage, V_{DD}. However, the dual-switch flyback high-side and low-side MOSFET turn on and off at the same time. Therefore, once the high-side MOSFET turns on, high-side V_S equals PFC V_O, the V_{DD} can't charge the C_{BOOT}, even though the high-side V_S is pulled down to ground at leakage energy recycle period, but the period is too short to charge C_{BOOT}.

Figure 8 shows the high-side gate-driver circuit with the auxiliary power supply. If V_{CBOOT} is less than the HV IC under-voltage threshold, the high-side gate output (V_{HO}) maintains turned-off state, then the low-side MOSFET turns on and charges the C_{BOOT} for one cycle, high-side driver restarts at the next PWM cycle. Finally, the voltage of auxiliary power supply follows the output voltage rise and continues to supply energy to the high-side circuit.

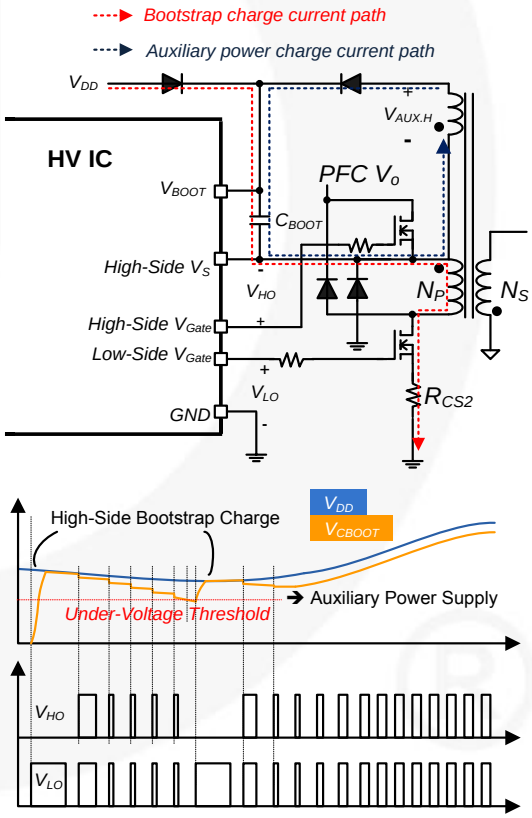

Figure 8. High-Side Driver Circuit and Start Waveform

Figure 9 shows the high-side driver circuit with standby power supply. This circuit uses the independent power supply for HV IC to keep the high-side driver operating. This circuit is used for applications with standby power, like the PC power.

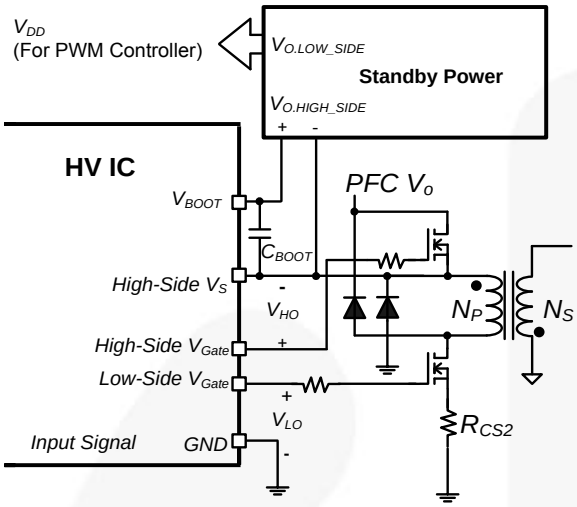

Figure 9. High-Side Driver Circuit with Standby Power Supply

5. Design Considerations

This design procedure uses the schematic in Figure 1 as a reference. A 90 W PFC application with universal input range is selected as a design example. The design specifications are:

- Line Voltage Range: 90~264 V_{AC} (60 Hz)
- Output of DC-DC Converter: 19 V/4.7 A (90 W)
- PFC Output Voltage: 400 V
- Minimum PFC Switching Frequency: > 50 kHz
- Brownout Protection Line Voltage: 70 V_{AC}
- Output Over-Voltage Protection Trip Point: 22.5 V
- Overall Efficiency: 90%
  (PFC Stage: 95%, DC-DC Stage: 95%)

Part A. PFC Section

[STEP-A1] Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. From Equation (2), the minimum frequency with a given line voltage and MOSFET on time is obtained as:

$$f_{SW,MIN} = \frac{1}{t_{ON}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE}}{V_{O.PFC}} \quad (3)$$

where:
V_{LINE} is RMS line voltage;
t_{ON} is the MOSFET conduction time; and
$V_{O.PFC}$ is the PFC output voltage.

The MOSFET conduction time with a given line voltage at a nominal output power is given as:

$$t_{ON} = \frac{2 \cdot P_{O.PFC} \cdot L}{\eta \cdot V_{LINE}^{2}} \quad (4)$$

where:
η is the overall efficiency;
L is the boost inductance; and
P_{OUT} is the nominal output power.

Using Equation (4), the minimum switching frequency of Equation (3) can be expressed as:

$$f_{SW,MIN} = \frac{\eta \cdot V_{LINE}^{2}}{2 \cdot P_{OUT} \cdot L} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE}}{V_{O.PFC}} \quad (5)$$

Since the minimum frequency occurs at high line as long as the PFC output voltage is lower than 405 V (as observed in Figure 5); once the output voltage and minimum switching frequency are set, the inductor value is given as:

$$L = \frac{\eta \cdot (V_{LINE.MAX})^{2}}{2 \cdot P_{OUT} \cdot f_{SW,MIN}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE.MAX}}{V_{O.PFC}} \quad (6)$$

where $V_{LINE,MAX}$ is the maximum line voltage.

As the minimum frequency decreases, the switching loss is reduced, while the inductor size and line filter size increase. Thus, the minimum switching frequency should be determined by the trade-off between efficiency and the size of magnetic components. The minimum switching frequency must be above 20 kHz to prevent audible noise.

Once the inductance value is decided, the maximum peak inductor current at the nominal output power is obtained at low-line condition as:

$$I_{L.PK} = \frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{LINE,MIN}} \quad (7)$$

where $V_{LINE,MIN}$ is the minimum line voltage.

Since the maximum on time is internally limited at 20 µs, it should be smaller than 20 µs such as:

$$t_{ON}^{MAX} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE.MIN}^{2}} < 20\mu s \quad (8)$$

The number of turns of boost inductor should be determined considering the core saturation. The minimum number is given as:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L}{A_e \cdot \Delta B} \quad (9)$$

where Ae is the cross-sectional area of core and ΔB is the maximum flux swing of the core in Tesla.

ΔB should be set below the saturation flux density.

(Design Example) Since the output voltage is 400 V, the minimum frequency occurs at high-line (264 V_{AC}) and full-load condition. Assuming the overall efficiency is 90% and selecting the minimum frequency as 50 kHz, the inductor value is obtained as:

$$L = \frac{\eta \cdot V_{LINE,MAX}^{2}}{2 \cdot P_{OUT} \cdot f_{SW,MIN}} \cdot \frac{V_{O.PFC.H} - \sqrt{2} \cdot V_{LINE,MAX}}{V_{O.PFC}}$$

$$= \frac{0.9 \cdot 264^2}{2 \cdot 90 \cdot 50 \times 10^3} \cdot \frac{400 - \sqrt{2} \cdot 264}{400} = 464 \mu H$$

The inductance of boot inductor is determined as 450 µH.

The maximum peak inductor current at nominal output power is calculated as:

$$I_{L,PK} = \frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{LINE,MIN}} = \frac{2\sqrt{2} \cdot 90}{0.9 \cdot 90} = 3.14A$$

$$t_{ON}^{MAX} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE.MIN}^{2}} = \frac{2 \cdot 90 \cdot 450 \times 10^{-6}}{0.9 \cdot 90^2}$$

$$= 11.1 \mu s < 20 \mu s$$

Assuming QP2512 core (3C96, A_e=110 mm^2) is used and setting ΔB as 0.30T, the primary winding should be:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L}{A_e \cdot \Delta B} = \frac{3.14 \times 450 \times 10^{-6}}{110 \times 10^{-6} \times 0.30} = 42.82 turns$$

Thus, the number of turns (N_{BOOST}) of boost inductor is determined as 44.

[STEP-A2] Auxiliary Winding Design

Figure 11 shows the internal block for zero-current detection (ZCD) for the PFC. FAN6920 indirectly detects the inductor zero current instant using an auxiliary winding of the boost inductor.

The auxiliary winding should be designed such that the voltage of the ZCD pin rises above 2.1 V when the boost switch is turned off to trigger internal comparator as:

$$\frac{N_{ZCD}}{N_{BOOST}} (V_{O.PFC.H} - \sqrt{2} V_{LINE.MAX}) > 2.1V \quad (10)$$

where $V_{O.PFC.H}$ is the PFC output voltage for high line condition.

The ZCD pin has upper and lower voltage clamping at 10 V and 0.45 V, respectively. When ZCD pin voltage is clamped at 0.45 V, the maximum sourcing current is 1.5 mA and, therefore, the resistor R_{ZCD} should be designed to limit the current of the ZCD pin below 1.5 mA in the worst case as:

$$R_{ZCD} > \frac{V_{IN}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} = \frac{\sqrt{2} V_{LINE.MAX}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} \quad (11)$$

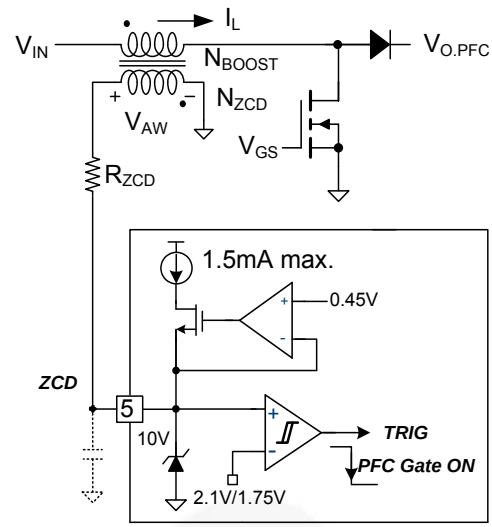

Figure 10. Internal Block for ZCD

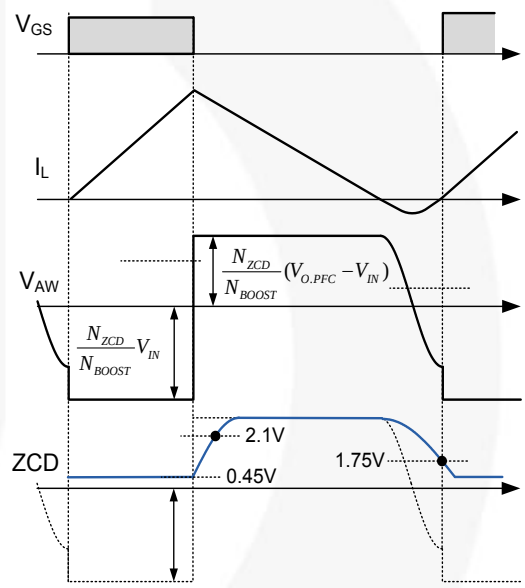

Figure 11. ZCD Waveforms

(Design Example) The number of turns for the auxiliary ZCD winding is obtained as:

$$N_{ZCD} > \frac{2.1 N_{BOOST}}{(V_{O.PFC.H} - \sqrt{2} V_{LINE.MAX})} = 3.5 turns$$

With a margin, N_{AUX} is determined as 8 turns.

Then R_{ZCD} is selected from:

$$R_{ZCD} > \frac{\sqrt{2} V_{LINE\,MAX}}{1.5mA} \cdot \frac{N_{ZCD}}{N_{BOOST}} = \frac{\sqrt{2} \cdot 264}{1.5 \times 10^{-3}} \cdot \frac{8}{44} = 45.248 k\Omega$$

as 47.5 kΩ.

[STEP-A3] Design V_{IN} Sense Circuit

FAN6920 senses the line voltage by using the averaging circuit shown in Figure 12, where the VIN pin is connected to the AC line through a voltage divider and low-pass filter capacitor. When V_{IN} drops below 1 V, the COMP pin is clamped at 1.6 V to limit the energy delivered to output. $V_{O.PFC}$ decreases with the INV pin voltage. When the INV pin voltage drops below 1 V, brownout protection is triggered, stopping gate drive signals of PFC and DC-DC. This protection is reset when V_{DD} drops below the turn-off threshold (UVLO threshold). When V_{DD} rises to the turn-on voltage after dropping below the turn-off threshold, FAN6920 resumes normal operation (if V_{IN} is above 1.2 V).

The brownout protection level can be determined as:

$$V_{LINE.BO} = \frac{\pi}{2\sqrt{2}} \cdot \frac{R_{VIN1} + R_{VIN2}}{R_{VIN2}} \tag{12}$$

The minimum line voltage for PFC startup is given as:

$$V_{LINE.STR} = 1.2 \cdot V_{LINE.BO} \tag{13}$$

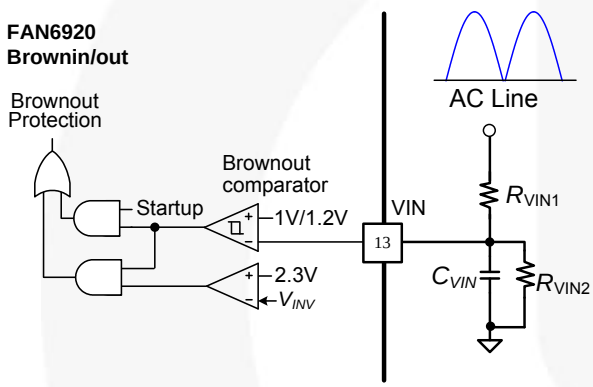

Figure 12. V_{IN} Sensing Internal Block

(Design Example) Setting the brownout protection trip point as 69 V_{AC}:

$$\frac{R_{VIN1} + R_{VIN2}}{R_{VIN2}} = V_{LINE.BO} \cdot \frac{2\sqrt{2}}{\pi} = 62$$

Determining R_{VIN2} as 154 kΩ, R_{VIN1} is determined as 9.4 MΩ.

The line voltage to startup the PFC is obtained as:

$$V_{LINE.STR} = 1.2 \cdot V_{LINE.BO} = 83 V_{AC}$$

[STEP-A4] Current Sensing Resistor for PFC

FAN6920 has pulse-by-pulse current limit function. It is typical to set the pulse-by-current limit level at 20~30% higher than the maximum inductor current:

$$R_{CS1} = \frac{0.82}{I_{L.PK}(1 + K_{MARGIN})} \tag{14}$$

where K_{MARGIN} is the margin factor and 0.82 V is the pulse-by-pulse current limit threshold.

(Design Example) Choosing the margin factor as 35%, the sensing resistor is selected as:

$$R_{CS1} = \frac{0.82}{I_{L.PK}(1 + K_{MARGIN})} = \frac{0.82}{3.14(1 + 0.35)} = 0.19\Omega$$

[STEP-A6] Design Compensation Network

The feedback loop bandwidth must be lower than 20 Hz for the PFC application. If the bandwidth is higher than 20 Hz, the control loop may try to reduce the 120 Hz ripple of the output voltage and the line current is distorted, decreasing power factor. A capacitor is connected between COMP and GND to attenuate the line frequency ripple voltage by 40 dB. If a capacitor is connected between the output of the error amplifier and the GND, the error amplifier works as an integrator and the error amplifier compensation capacitor can be calculated by:

$$C_{COMP} > \frac{100 \cdot g_M}{2\pi \cdot 2 f_{LINE}} \cdot \frac{2.5}{V_{O.PFC.H}} \tag{15}$$

To improve the power factor, C_{COMP} must be higher than the calculated value. However, if the value is too high, the output voltage control loop may become slow.

(Design Example)

$$C_{COMP} > \frac{100 \cdot g_M}{2\pi \cdot 2 f_{LINE}} \cdot \frac{2.5}{V_{O.PFC.H}} = \frac{100 \cdot 125 \times 10^{-6}}{2\pi \cdot 2 \cdot 60} \cdot \frac{2.5}{400} = 103nF$$

470 nF is selected for better power factor.

Part B. DC-DC Section

[STEP-B1] Determine the Secondary-Side Rectifier Voltage (V_D^{nom})

Figure 13 shows the typical operation waveforms of a dual-switch quasi-resonant flyback converter. When the MOSFET is turned off, the input voltage (PFC output voltage), together with the output voltage reflected to the primary (V_{RO}), are imposed on the MOSFET. When the MOSFET is turned on, the sum of input voltage reflected to the secondary side and the output voltage is applied across the secondary-side rectifier. Thus, the maximum nominal voltage across the MOSFET (V_{ds}^{nom}) and diode are given as:

$$V_{DS}^{nom} = \frac{V_{O.PFC} + n(V_O + V_F)}{2} = \frac{V_{O.PFC} + V_{RO}}{2} \tag{16}$$

where:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F}$$

$$V_D^{nom} = V_O + \frac{V_{O.PFC}}{n} \tag{17}$$

By increasing V_{RO} (i.e. the turns ratio, n), the capacitive switching loss and conduction loss of the MOSFET are reduced. This also reduces the voltage stress of the secondary-side rectifier. V_{RO} should be determined by a trade-off between the hold-up time and voltage stresses of the secondary-side rectifier diode.

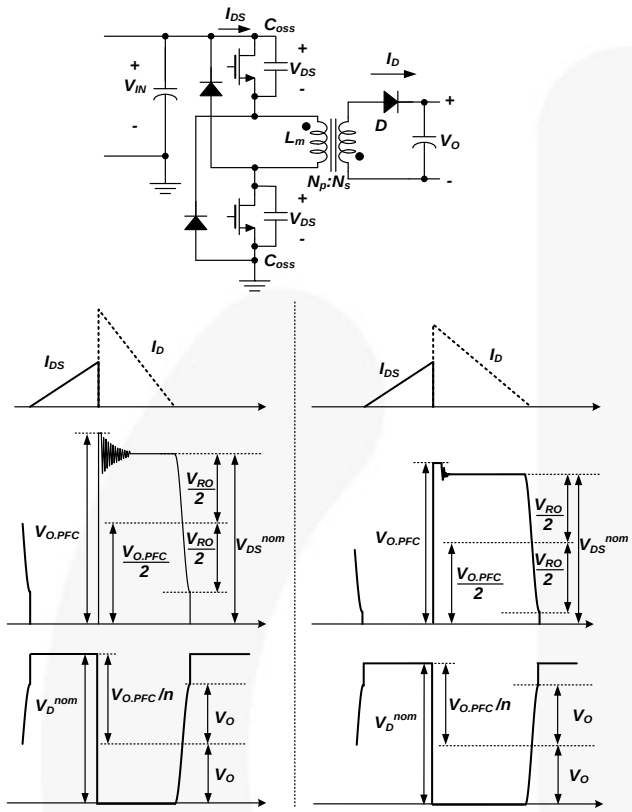

Figure 13. Typical Waveforms of QR Flyback Converter

(Design Example) Assuming 75 V MOSFET (synchronous rectification) is used for secondary side, with 70% voltage margin:

$$0.7 \cdot 75 > V_D^{nom} = V_O + \frac{V_{O.PFC}}{n}$$

$$\therefore n > \frac{V_{O.PFC}}{0.7 \cdot 75 - V_O} = \frac{400}{0.7 \cdot 75 - 19} = 11.94$$

Thus, n is determined as 12.

[STEP-B2] Calculate the Minimum PFC Output Voltage ($V_{O.PFC.L}$) for Hold-up Time

For the PFC output capacitor, it is typical to use 0.5~1 µF per 1 W output power for 400 V PFC output. Meanwhile, it is reasonable to use ~1 µF per 1 W output power for variable output PFC due to the larger voltage drop during the hold-up time than 400 V output. In this example, 100 µF capacitors is selected for the output capacitors ($C_{O.PFC}$).

Lower PFC output voltage can improve system efficiency at low AC line voltage condition, but the energy of the PFC output capacitor effects the hold-up time. The minimum PFC output voltage for required hold-up time is obtained as:

$$V_{O.PFC}^{\min} \geq \sqrt{\frac{2 \cdot t_{HOLD} \cdot P_{OUT}}{\eta \cdot C_{O.PFC}} + V_{O.PFC.HLD}^{2}} \quad (18)$$

where:

t_{HOLD} is the required holdup time;

P_{OUT} is total nominal output power;

$V_{O.PFC.L}$ is the minimum PFC output voltage for required hold-up time; and

$V_{O.PFC.HLD}$ is the allowable minimum PFC output voltage during the hold-up time.

The voltage of transformer primary-side winding is clamped to $V_{O,PFC}$, so the minimum PFC output voltage during the hold-up time is obtained as:

$$V_{O.PFC.HLD} = n \cdot (V_O + V_F) \quad (19)$$

where V_F is the body diode forward voltage of the synchronous rectification MOSFET, which is around 1 V.

(Design Example) Because the PFC response is very slow, the hold-up time needs to be more than 12 ms to avoid PFC output voltage drop affecting the output voltage at dynamic-load condition. Assuming hold-up time is 12 ms, the $V_{O.PFC}^{\min}$ as:

$$V_{O.PFC}^{\min} \geq \sqrt{\frac{2 \cdot t_{HOLD} \cdot P_{OUT}}{\eta \cdot C_{O.PFC}} + [n \cdot (V_O + V_F)]^2}$$

$$= \sqrt{\frac{2 \cdot 12 \times 10^{-3} \times 90}{0.9 \cdot 100 \times 10^{-6}} + [12 \cdot (19+1)]^2} = 286V$$

[STEP-B3] Transformer Design

Figure 14 shows the typical switching timing of a quasi-resonant converter. The sum of MOSFET conduction time (t_{ON}), diode conduction time (t_D), and drain voltage falling time (t_F) is the switching period (t_S). To determine the primary-side inductance (L_m), the following parameters should be determined first.

Minimum Switching Frequency ($f_{S.QR}^{\min}$)

The minimum switching frequency occurs at the minimum input voltage and full-load condition, which should be higher than 20 kHz to avoid audible noise. By increasing $f_{S.QR}^{\min}$, the transformer size can be reduced. However, this results in increased switching losses. Determine $f_{S.QR}^{\min}$ by a trade-off between switching losses and transformer size. Typically $f_{S.QR}^{\min}$ is set around 70 kHz.

Falling Time of the MOSFET Drain Voltage (t_F)

As shown in Figure 14, the MOSFET drain voltage fall time is half of the resonant period of the MOSFET's effective output capacitance and primary-side inductance. The typical value for t_F is 0.6~1.2 µs.

Non-Conduction Time of the MOSFET (t_{OFF})

FAN6920 has a minimum non-conduction time of MOSFET (5 µs), during which turning on the MOSFET is prohibited. To maximize the efficiency, it is necessary to turn on the MOSFET at the first valley of MOSFET drain-to-source voltage at heavy-load condition. Therefore, the MOSFET non-conduction time at heavy load condition should be larger than 5 µs.

After determining $f_{S.QR}^{min}$ and t_F, the maximum duty cycle is calculated as:

$$D_{\max} = \frac{V_{RO}}{V_{RO} + V_{O.PFC.L}} \cdot (1 - f_{S.QR}^{\min} \cdot t_F) \tag{20}$$

Then, the primary-side inductance is obtained as:

$$L_m = \frac{\eta_{QR} \cdot (V_{O.PFC.L} \cdot D_{\max})^2}{2 \cdot f_{S.QR}^{\min} P_{OUT}} \tag{21}$$

Once L_m is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as:

$$I_{DS}^{PK} = \frac{V_{O.PFC.L} \cdot D_{\max}}{L_m f_{S.QR}^{\min}} \tag{22}$$

$$I_{DS}^{RMS} = I_{DS}^{PK} \sqrt{\frac{D_{\max}}{3}} \tag{23}$$

The MOSFET non-conduction time at heavy load and low line is obtained as:

$$t_{OFF.L} = \frac{(1 - D_{\max})}{f_{S.QR}^{min}} \tag{24}$$

The MOSFET non-conduction time at heavy load and higher voltage of PFC output ($V_{O.PFC.H}$) is obtained as:

$$t_{OFF.H} = t_{OFF.L} \cdot \frac{V_{O.PFC.L}}{V_{O.PFC.H}} \cdot \frac{V_{O.PFC.H} + V_{RO}}{V_{O.PFC.L} + V_{RO}} \tag{25}$$

To guarantee the first valley switching at high line and heavy-load condition, $t_{OFF.H}$ should be larger than 5 µs.

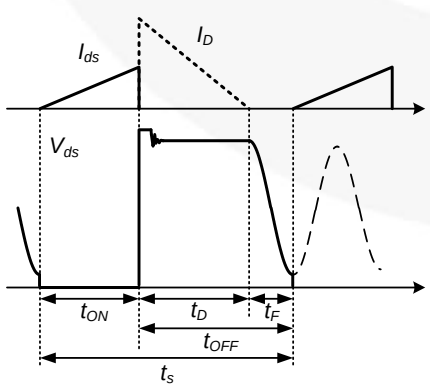

Figure 14. Switching Timing Sequence of QR Flyback Converter

When designing the transformer, the maximum flux density swing in normal operation (B) as well as the maximum flux density in transient (B_{max}) should be considered. The maximum flux density swing in normal operation is related to the hysteresis loss in the core, while the maximum flux density in transient is related to the core saturation.

The minimum number of turns for the transformer primary side to avoid over temperature in the core is given by:

$$N_P^{\min} = \frac{L_m I_{DS}^{PK}}{A_e \Delta B} \tag{26}$$

where B is the maximum flux density swing in Tesla.

If there is no reference data, use B =0.25~0.30 T.

Once the minimum number of turns for the primary side is determined, calculate the proper integer for N_S so that the resulting N_P is larger than N_p^{min} as:

$$N_P = n \cdot N_S > N_P^{\min} \tag{27}$$

The number of turns of the auxiliary winding for V_{DD} is given as:

$$N_{AUX} = \frac{V_{DD}^{nom} + V_{FA}}{(V_O + V_F)} \cdot N_S \tag{28}$$

where V_{DD}^{nom} is the nominal V_{DD} voltage, the range about 12~20 V, and the V_{FA} is forward-voltage drop of V_{DD} diode, about 1 V.

Once the number of turns of the primary winding is determined, the maximum flux density when the drain current reaches its pulse-by-pulse current limit level should be checked to guarantee the transformer is not saturated during transient or fault condition.

The maximum flux density (B_{max}) when drain current reaches I_{LIM} is given as:

$$B_{\max} = \frac{L_m I_{LIM}}{A_e N_P} < B_{sat} \tag{29}$$

B_{max} should be smaller than the saturation flux density.

If there is no reference data, use B_{sat} =0.35~0.40 T.

(Design Example) Setting the minimum frequency is 65 kHz and the falling time is 1 µs, and assuming $V_{O.PFC.L}$=300 V:

$$D_{\max} = \frac{V_{RO}}{V_{RO} + V_{O.PFC.L}} \cdot (1 - f_{S.QR}^{\min} \cdot t_F)$$

$$= \frac{240}{240 + 300} \cdot (1 - 70 \times 10^3 \cdot 1 \times 10^{-6}) = 0.413$$

$$L_m = \frac{\eta \cdot (V_{O.PFC.L} \cdot D_{\max})^2}{2 \cdot f_{s.QR}^{\min} \cdot P_O}$$

$$= \frac{0.95 \cdot (300 \cdot 0.413)^2}{2 \cdot 70 \times 10^3 \cdot 90} = 1160 \mu H$$

$$I_{DS}^{PK} = \frac{V_{O.PFC.L} \cdot D_{\max}}{L_m f_{S.QR}^{\min}}$$

$$= \frac{300 \cdot 0.413}{1160 \times 10^{-6} \cdot 70 \times 10^3} = 1.53A$$

$$t_{OFF.L} = \frac{(1 - D_{\max})}{f_{S.QR}^{\min}} = \frac{1 - 0.413}{70 \times 10^3} = 8.39 \mu s$$

$$t_{OFF.H} = t_{OFF.L} \cdot \frac{V_{O.PFC.L}}{V_{O.PFC.H}} \cdot \frac{V_{O.PFC.H} + V_{RO}}{V_{O.PFC.L} + V_{RO}}$$

$$= 8.39 \times 10^{-6} \cdot \frac{300}{400} \cdot \frac{400 + 240}{300 + 240} = 7.46 \mu s > 5 \mu s$$

Assuming QP2912 (Ae=144 mm^2) core is used and the flux swing is 0.28 T

$$N_P^{\min} = \frac{L_m I_{DS}^{PK}}{A_e \Delta B} = \frac{1160 \times 10^{-6} \cdot 1.53}{144 \times 10^{-6} \cdot 0.28} = 44$$

$$N_P = n \cdot N_S \Rightarrow 12 \cdot 3 = 36 < N_P^{\min}$$

$$\Rightarrow 12 \cdot 4 = 48 > N_P^{\min}$$

N_P is determined as 48, N_S is 4.

$$\frac{12 + V_{FA}}{(V_O + V_F)} \cdot N_S < N_{AUX} < \frac{20 + V_{FA}}{(V_O + V_F)} \cdot N_S$$

$$\Rightarrow \frac{12 + 1}{20} \cdot 4 < N_{AUX} < \frac{20 + 1}{20} \cdot 4$$

$$\Rightarrow 2.6 < N_{AUX} < 4.2$$

Thus, N_{AUX} is determined as 3.

The number of turns of the high-side driver auxiliary is given as:

$N_{AUX.H} \leqq N_{AUX}$

$N_{AUX.H}$ is determined as 2.

Assuming the pulse-by-pulse current limit for low PFC output voltage is 140% of peak drain current at heavy load:

$$B_{\max} = \frac{L_m I_{LIM}}{A_e N_P} = \frac{1160 \times 10^{-6} \cdot 2.14}{144 \times 10^{-6} \cdot 48} = 0.36T$$

[STEP-B3] Design the Valley Detection Circuit

The valley of MOSFET voltage is detected by monitoring the current flowing out of the DET pin. The typical application circuit is shown as Figure 15 and typical waveforms are shown in Figure 16. The DET pin has upper and lower voltage clamping at 5 V and 0.7 V, respectively. The valley detection circuit is blanked for 5 µs after the MOSFET is turned off. When V_{AUX} drops below zero, V_{DET} is clamped at 0.7 V and current flows out of the DET pin. MOSFET is turned on with 200 ns delay once the current flowing out of DET pin exceeds 30 µA. To guarantee that valley detection circuit is triggered when the DET pin is clamped at 0.7 V, the current flowing through R_{DET2} should be larger than 30 µA as:

$$\frac{0.7}{R_{DET2}} > 30 \mu A \quad (30)$$

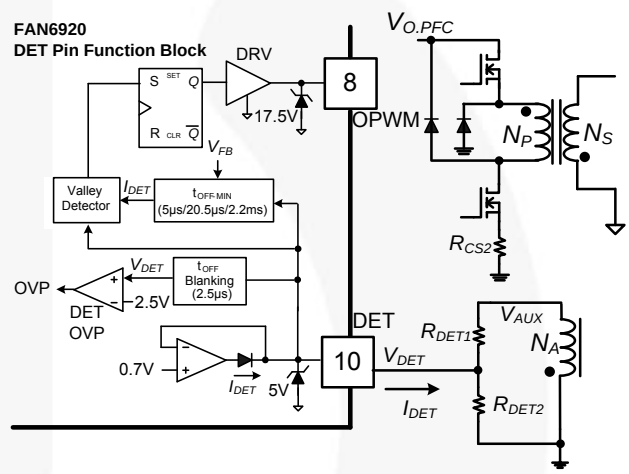

Figure 15. Typical Application Circuit of DET Pin

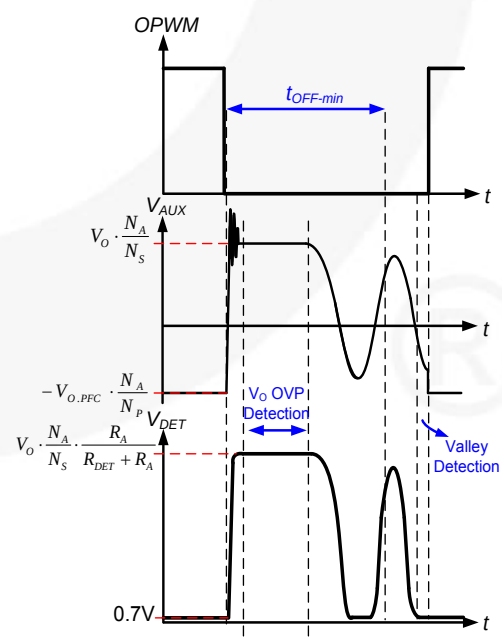

Figure 16. Waveforms of Valley Detection and V_O OVP Detection

The output is indirectly monitored for over-voltage protection using the DET pin voltage while the MOSFET is turned off. The ratio of R_{DET1} and R_{DET2} should be determined as:

$$2.5 = \frac{R_{DET2}}{R_{DET1} + R_{DET2}} \frac{N_A}{N_S} V_{OVP} = \frac{1}{K_{DET} + 1} \frac{N_A}{N_S} V_{OVP} \quad (31)$$

where the ratio between R_{DET1} and R_{DET2} is obtained as:

$$K_{DET} = \frac{R_{DET1}}{R_{DET2}} = \frac{N_A}{N_S} \cdot \frac{V_{OVP}}{2.5} - 1 \quad (32)$$

For a quasi-resonant flyback converter, the peak-drain current with a given output power decreases as input voltage increases. Thus, constant power limit cannot be achieved by using pulse-by-pulse current limit with constant threshold. FAN6920 has high/low line over-power compensation that reduces the pulse-by-pulse current limit level as input voltage increases. FAN6920 senses the input voltage using the current flowing out of the DET pin while the MOSFET is turned on. The pulse-by-pulse current limit level vs. DET current is depicted in Figure 18.

The DET pin current for low-line and high-line PFC output voltages are given as:

$$I_{DET.L} = \frac{V_{O.PFC.L} \frac{N_A}{N_P} - 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}} \cong \frac{V_{O.PFC.L} \frac{N_A}{N_P}}{R_{DET1}} \quad (33)$$

$$I_{DET.H} = \frac{V_{O.PFC.H} \frac{N_A}{N_P} - 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}} \cong \frac{V_{O.PFC.H} \frac{N_A}{N_P}}{R_{DET1}} \quad (34)$$

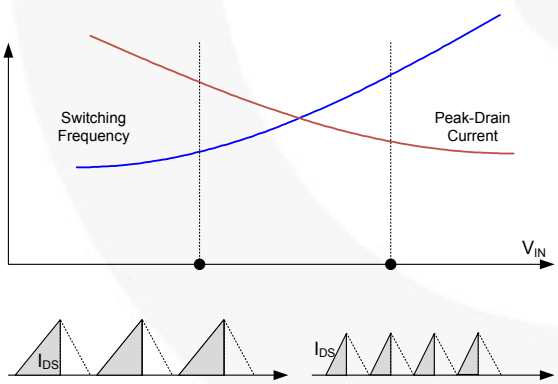

Figure 17. Switching Frequency and Peak-Drain Current Change as Input Voltage Increases

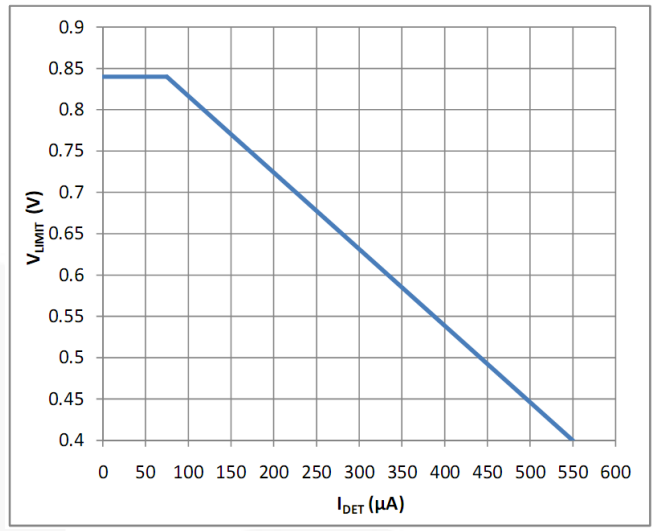

Figure 18. I_{DET}-V_{LIMIT} Curve

The relationship between I_{DET} and V_{LIMIT} in the linear region (I_{DET}=100~500 µA) can be approximated as:

$$V_{LIMIT} = -877 \cdot I_{DET} + 0.882 \quad (35)$$

Assuming two-level voltage PFC output: for a given output power, the ratio between drain-peak currents at low line and high line is obtained as:

$$\frac{I_{DS}^{PK.L}}{I_{DS}^{PK.H}} = \frac{V_{O.PFC.H}}{V_{O.PFC.L}} \cdot \frac{V_{O.PFC.L} + V_{RO}}{V_{O.PFC.H} + V_{RO}} \quad (36)$$

For a given output power, the ratio between pulse-by-pulse current limit levels at low line and high line is obtained as:

$$\frac{V_{LIMIT.L}}{V_{LIMIT.H}} \cong \frac{-994 \cdot V_{O.PFC.L} \frac{N_A}{N_P} + R_{DET1}}{-994 \cdot V_{O.PFC.H} \frac{N_A}{N_P} + R_{DET1}} \quad (37)$$

To get a constant power limit, R_{DET1} should be determined such that Equations (38) and (39) are equal. However, for actual design, it is typical to use 108~115% of Equation (38), considering the pulse-by-pulse turn-off delay and increased PFC output voltage ripple at low line.

Once the current-limit threshold voltage is determined with R_{DET1}, the current-sensing resistor value is obtained as:

$$V_{LIMIT} = -877 \cdot \left(\frac{V_{O.PFC.L} \frac{N_A}{N_P} - 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}} \right) + 0.882 \quad (38)$$

The current-sensing resistor value can be obtained from:

$$R_{CS2} = \frac{V_{LIMIT}}{I_{DS}^{LIM}} \quad (39)$$

(Design Example)

$$\frac{0.7}{R_{DET2}} > 30\mu A \ , \quad R_{DET2} < 23.3k\Omega$$

Setting the OVP trip point at 22.5 V,

$$K_{DET} = \frac{R_{DET1}}{R_{DET2}} = \frac{N_{AUX}}{N_S} \cdot \frac{V_{OVP}}{2.5} - 1 = \frac{3}{4} \cdot \frac{22.5}{2.5} - 1 = 5.75$$

Then $R_{DET1} = K_{DET \cdot R} \cdot R_{DET2} < 134k\Omega$

$$\frac{I_{DS}^{PK.L}}{I_{DS}^{PK.K}} = \frac{V_{O.PFC.H}}{V_{O.PFC.L}} \cdot \frac{V_{O.PFC.L} + V_{RO}}{V_{O.PFC.H} + V_{RO}}$$

$$= \frac{400}{300} \cdot \frac{300+240}{400+240} = 1.125$$

Using 113% of 1.125,

$$\frac{V_{LIMIT.L}}{V_{LIMIT.H}} = 1.27 = \frac{-994 \cdot V_{O.PFC.L} \frac{N_A}{N_P} + R_{DET1}}{-994 \cdot V_{O.PFC.H} \frac{N_A}{N_P} + R_{DET1}}$$

$$= \frac{-994 \cdot 300 \cdot \frac{3}{48} + R_{DET1}}{-994 \cdot 400 \cdot \frac{3}{48} + R_{DET1}} = \frac{-18637.5 + R_{DET1}}{-24850 + R_{DET1}}$$

Then, R_{DET1} = 47.5 kΩ and R_{EDT2}=8.25 kΩ.

R_{DET1} and R_{DET2} are selected from the off-the-shelf components as 150 kΩ and 18 kΩ, respectively.

Then, the pulse by pulse current limit threshold voltage is obtained as:

$$V_{LIMIT} = -877 \cdot \left(\frac{V_{O.PFC.L} \frac{N_A}{N_P} - 0.7}{R_{DET1}} + \frac{0.7}{R_{DET2}}\right) + 0.882$$

$$= 0.474V$$

To set current limit level at low line as 115% of I_{DS}^{PK}

$$\frac{0.63}{1.53A \times 1.15} = 0.27\Omega$$

[STEP-B4] Design the Feedback Circuit

Figure 19 is a typical feedback circuit mainly consisting of a shunt regulator and a photo-coupler. R_{01} and R_{02} form a voltage divider for output voltage regulation. R_F and C_F are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB} = 100 Ω, C_{FB} = 1 nF) placed from the FB pin to GND can increase stability substantially. The maximum source current of the FB pin is about 1.2 mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor, R_{BIAS}, is determined as:

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \cdot CTR > 1.2 \times 10^{-3} \qquad (40)$$

where V_{OPD} is the drop voltage of photodiode, about 1.2 V; V_{KA} is the minimum cathode to anode voltage of shunt regulator (2.5 V); and CTR is the current transfer rate of the opto-coupler.

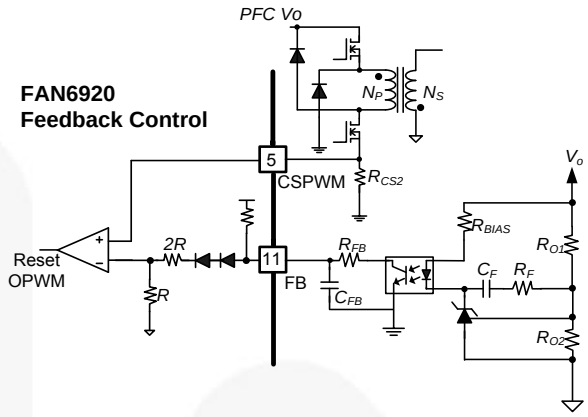

Figure 19. Feedback Circuit

(Design Example) Assuming CTR is 100%;

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \cdot CTR > 1.2 \times 10^{-3}$$

$$R_{BIAS} < \frac{V_O - V_{OPD} - V_{KA}}{1.2 \times 10^{-3}} = \frac{19 - 1.2 - 2.5}{1.2 \times 10^{-3}} = 12.75k\Omega$$

330 Ω resistor is selected for R_{BIAS}.

The voltage divider resistors for V_O sensing are selected as 66.5 kΩ and 10 kΩ.

[STEP-B5] Design the Over-Temperature Protection Circuit

The adjustable Over-Temperature Protection (OTP) circuit is shown in Figure 20. As can be seen, a constant sourcing current source (I_{RT}) is connected to the RT pin. Once V_{RT} is lower than 0.8 V for longer than 10 ms debounce time, FAN6920 is latched off. R_{RT} can be determined by:

$$0.8V = (R_{RT} + R_{NTC@OT}) \times 100\mu A \qquad (41)$$

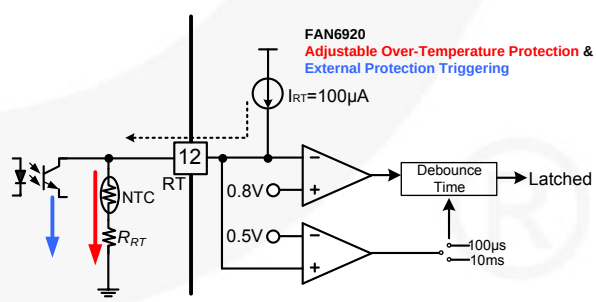

Figure 20. Adjustable Over-Temperature Protection and External Latched-off Function

(Design Example) Assuming the resistance of NTC at over-temperature protection point is 4.3 kΩ;

$$R_{RT} = \frac{0.8V}{100\mu A} - 4.3k\Omega = 3.7k\Omega$$

Final Schematic of Design Example

This section summaries the final design example. The key system specifications are summarized in Table 1 and the key design parameters are summarized in Table 2. The final schematic is in Figure 21. To have enough hold-up time for V_{DD} during startup, a two-stage circuit is used for V_{DD}. To maximize the efficiency, the synchronous rectification using Fairchild's FAN6204 is used for the secondary rectifier.

Table 1. System Specifications

Input	
Input Voltage Range	90~264 V_{AC}
Line Frequency Range	47~63 Hz
Output	
Output Voltage (V_o)	19 V
Output Power (P_o)	90 W

Table 2. Key Design Parameters

PFC Stage	
PFC Inductor (L_{BOOST})	450 µH
Turns of PFC Inductor (N_{BOOST})	44 T
Turns of ZCD Auxiliary Winding (N_{ZCD})	8 T
Minimum Switching Frequency ($f_{S.PFC}^{min}$)	40 kHz
PWM Stage	
Turns of Primary Inductor of PWM Transformer (N_P)	48 T
Turns of Auxiliary Winding of PWM Transformer (N_{AUX})	4 T
Turns of Auxiliary Winding of High-Side Driver Transformer ($N_{AUX.H}$)	3 T
Turns Ratio of PWM Transformer (n)	12
Primary Inductor (L_P)	1160 µH
Minimum Switching Frequency ($f_{S.QR}^{min}$)	70 kHz

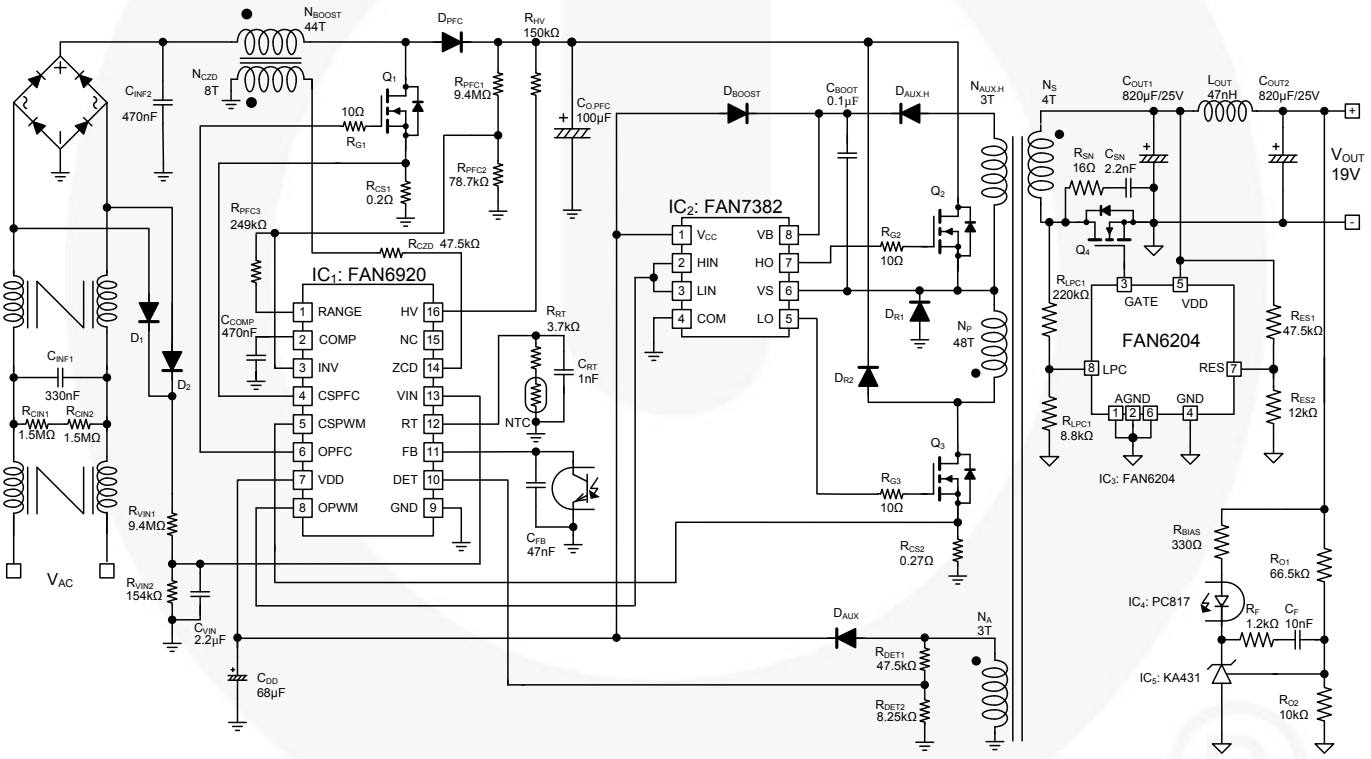

Figure 21. Final Schematic of Design Example

Table 3. Bill of Materials

Part	Value	Note
Resistor		
R_{PFC1}	9.4 MΩ	1/4 W
R_{PFC2}	78.7 kΩ	1/8 W
R_{PFC3}	249 kΩ	1/8 W
R_{VIN1}	9.4 MΩ	1/4 W
R_{VIN2}	154 kΩ	1/8 W
R_{ZCD}	47.5 kΩ	1/4 W
R_{HV}	150 kΩ	1 W
R_{RT}	3.7 kΩ	1/8 W
R_{CS1}	0.2 Ω	2 W
R_{CS2}	0.27 Ω	2 W
R_{G1}	10 Ω	1/4 W
R_{G2}	10 Ω	1/4 W
R_{G3}	10 Ω	1/4 W
R_{DET1}	47.5 kΩ	1/4 W
R_{DET2}	8.25 kΩ	1/8 W
R_{CIN1}	1.5 MΩ	1/4 W
R_{CIN2}	1.5 MΩ	1/4 W
R_{LPC1}	220 kΩ	1/8 W
R_{LPC2}	8.8 kΩ	1/8 W
R_{RES1}	47.5 kΩ	1/8 W
R_{RES2}	12 kΩ	1/8 W
R_{SN}	16Ω	1 W
R_{O1}	66.5 kΩ	1/8 W
R_{O2}	10 kΩ	1/8 W
R_{BIAS}	330 Ω	1/4 W
R_F	1.2 kΩ	1/8 W
Capacitor		
C_{INF1}	330 nF	XCAP
C_{INF2}	470 nF	
C_{VIN}	2.2 µF	
C_{COMP}	470 nF	
C_{DD}	68 µF	50 V
C_{RT}	1 nF	

Part	Value	Note
C_{FB}	47 nF	
$C_{O.PFC}$	100 µF	450 V
C_{SN}	2.2 nF	
C_F	10 nF	
C_{OUT1}	820 µF	25 V
C_{OUT2}	820 µF	25 V
C_{BOOT}	0.1 µF	
Diode		
D_1	S1J	
D_2	S1J	
D_{PFC}	ES3J	
D_{BOOST}	ES1H	Ultra-Fast Diode
D_{AUX}	RS1D	Fast Diode
$D_{AUX.H}$	RS1D	Fast Diode
D_{R1}	ES1H	Ultra-Fast Diode
D_{R2}	ES1H	Ultra-Fast Diode
MOSFET		
Q_1	FCB11N60	
Q_2	FCB11N60	
Q_3	FCB11N60	
Q_4	FDB031N08	
IC		
IC_1	FAN6921MR	
IC_2	FAN7382	
IC_3	FAN6204	
IC_4	PC817	
IC_5	KA431	
Other		
NTC	TTC104	
L_{OUT}	47 nH	

Lab Note

Before modifying or soldering / desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be damaged by external high-voltage.

This device is sensitive to electrostatic discharge (ESD). To improve the production yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

Printed Circuit Board Layout

Printed circuit board layout and design are very important for switching power supplies where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes EMI and prevents the power supply from being disrupted during surge/ESD tests.

IC Side

- Reference ground of the INV, COMP, CSPFC, CSPWM, and VDD pins are connected together and then connected to the IC's GND directly.
- Reference ground of ZCD, VIN, RT, FB, and DET pins are connected to IC's GND directly.
- Small capacitors around the IC should be connected to the IC directly.
- The trace line of CSPWM, OPFC, and OPWM should not be paralleled and should be close to each other to avoid introducing noise.
- Connections of IC's GND, $R_{CS.PWM}$ ground, HV IC's GND, and auxiliary winding of PWM XFMR:

  Approach

  - Auxiliary winding's ground ➔ IC's GND ➔ $R_{CS.PWM}$'s ground (2➔1➔4)
  - **HV IC's GND ➔ $R_{CS.PWM}$**'s ground (3➔4)

System Side

PFC Stage

- Auxiliary winding of PFC choke is connected to IC's GND.
- $R_{CS.PFC}$ should be connected to C_2's ground singly (6 & 8).
- External driver circuit can shorten MOSFET gate discharge current loop and improve the surge/ESD capability.
- Current loop constructed by the PFC choke, PFC diode, PFC MOSFET, C_{Bulk}, and C_2 should be as short as possible.

PWM Stage

- $R_{CS.PWM}$ should be connected to $C_{Bulk's}$ ground directly. Keep it short and wide.
- Current loop constructed by the C_{Bulk}, XFMR, PWM MOSFET, clamp diode, and $R_{CS.PWM}$ should be as short as possible.
- Ground of photo-coupler should be connected to IC's GND.
- On the secondary side, current loop constructed by XFMR, Schottky, and output capacitor should be as short as possible.
- Connections of Y Capacitor:

  Approach

  - Y CAP's primary ground ➔ C_1's ground (10➔9)

  Approach Ground Loop:

  - 7 & 2 ➔ 1 ➔ 4
  - 3 ➔ 4
  - 4 ➔ 5 ➔ 8
  - 6 ➔ 8
  - 8 & 10 ➔ 9

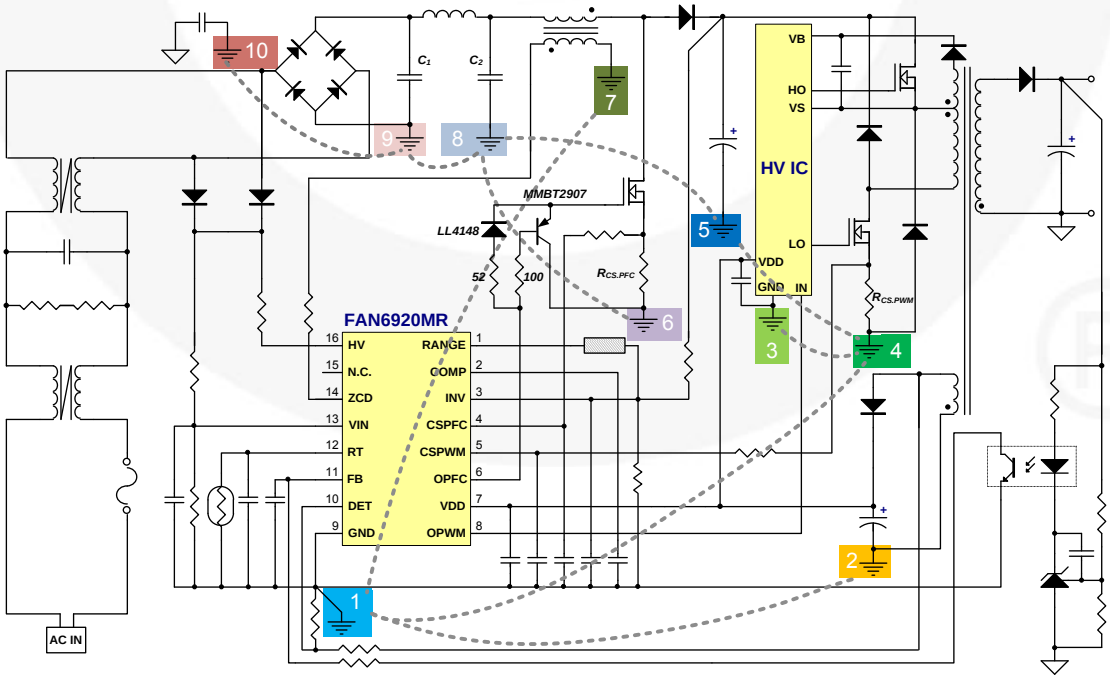

Figure 22. Layout Considerations

Related Documents

FAN6920MR — Highly Integrated Quasi-Resonant Current PWM Controller

FAN6204MY — Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

FAN7382 — High- and Low-Side Gate Driver

AN-6076 — Design and Application Guide of Bootstrap Circuit for High-Voltage Gate –Driver IC

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