

## Dynamic Threshold for Advanced CMOS Logic

### Introduction

Most users of digital logic are quite familiar with the threshold specifications found on family logic data sheets. Designers using products with TTL level input thresholds will see numbers like  $V_{IH} = 2.0\text{ V}$  and  $V_{IL} = 0.8\text{ V}$ . These threshold guarantees are static, a part's response to these levels during switching transients can be undesirable. Through the course of this paper the reader should gain an understanding for the difference between a static threshold and a dynamic threshold. This paper will also discuss how various products respond dynamically and how dynamic thresholds are tested and specified. Lastly, this paper will look at how FACT<sup>®</sup> Quiet Series has addressed and specified dynamic threshold characteristics.

### What Is a Dynamic Threshold?

If ON Semiconductor were able to package its I.C.'s in "ideal" packages, then dynamic and static thresholds would be one and the same. However, packages are not "ideal" and have a finite amount of inductance associated with each signal lead. As will be shown later, it is the inductance in the power leads which is the primary reason for dynamic thresholds.

To understand the phenomena of dynamic threshold, properties of ground bounce must first be examined. Figure 1 is a representation for a 74XX00 product which includes package inductance. Figure 2a shows an output pull-down making an HL/ZL transition. In discharging the load capacitor, a current  $I_C$  equaling  $C \cdot dv/dt$  flows into the chip. This current is approximated versus time in Figure 2b. The changing current,  $I_C$ , generates a voltage across the ground inductor represented in Figure 2c. The equation  $L \cdot di/dt$  provides the relationship of current and time with respect to a given inductor. It is the voltage across the ground inductor, commonly known as ground bounce, which causes static and dynamic thresholds to differ.



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### APPLICATION NOTE

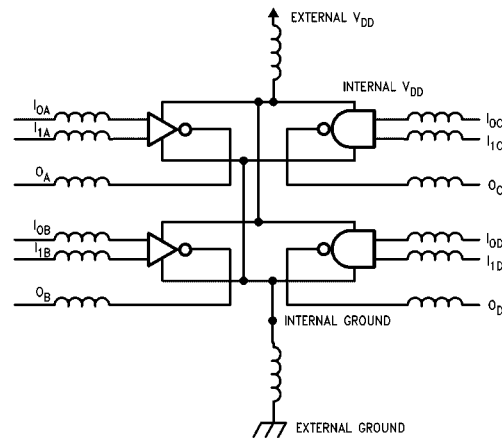


Figure 1. A Typical 2-Input Quad NAND Gate

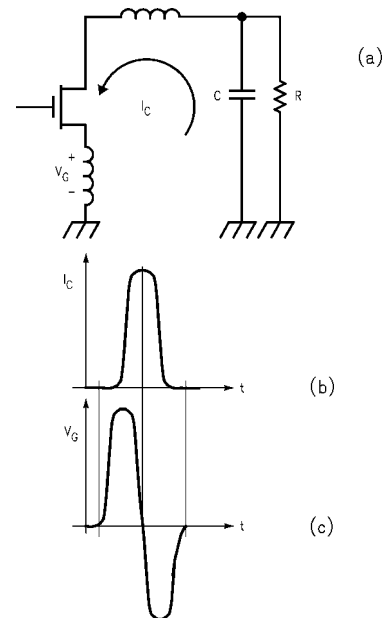


Figure 2. Package Inductance Causes Ground Bounce

The threshold of an IC is referenced to its internal ground. Therefore, voltages induced on the ground inductor are reflected directly as a change in threshold with respect to external ground. Figure 3 shows the effects of ground bounce on an input threshold. A problem area exists if when the threshold is moving, the threshold crosses the input voltage levels. However, having the threshold cross the input level does not necessarily induce a product failure. The threshold must cross the input level for a period of time for a false switch to occur. (Figure 4 shows the voltage time relationship). Note that in the high speed technologies two things have come together, faster delays and output edge rates. This translates to larger di/dt's and an ability to react to narrower pulses.

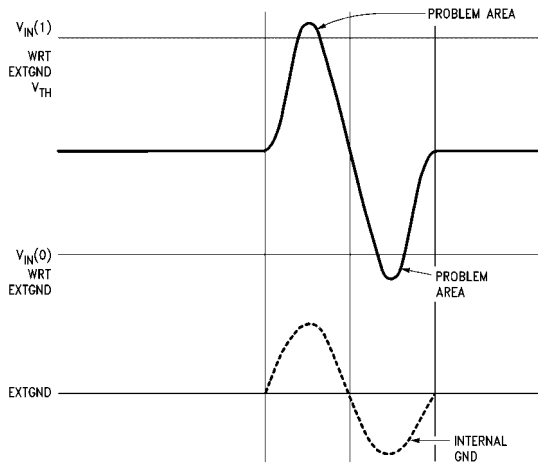


Figure 3. Ground Bounce Changes Input Threshold

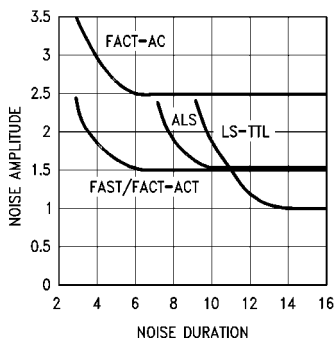


Figure 4. Device Speed Effects Noise Margins

In the example discussed above, ground bounce was outlined as the cause for the threshold change. For bipolar TTL technologies, this is the only noise source of concern since the threshold is created by a  $V_{BE}$  transistor stack referenced to ground. As  $V_{CC}$  changes in a bipolar circuit, the threshold will change logarithmically as the currents in the transistors change. For example, a 1 V change in  $V_{CC}$  creates approximately a 34 mV shift in threshold. CMOS thresholds are set up as a percentage of  $V_{DD}$  and track linearly with  $V_{DD}$  changes. Therefore, a noise spike on  $V_{DD}$

from an LH/ZH transition generates dynamic threshold characteristics which must be considered along with those of the HL/ZL edges. In this example let internal ground bounce to a 1 V peak; the bipolar threshold will peak to approximately 2.5 V. If we consider a TTL level static threshold for a CMOS device input of 1.5 V, the following applies:  $((V_{TH} / V_{DD} * V_{DD} * V_{bounce}) + 1.0 V) = ((0.3 * (4.0) + 1.0) = 2.2 V$ .

Consider a negative bounce of 1 V on the internal  $V_{DD}$  bus. The threshold delta for the bipolar product will be negligible, but the CMOS input threshold will change as follows:  $((V_{TH} / V_{DD} * (V_{DD} * V_{bounce})) = (0.3 * (4)) = 1.2 V$

**How are Dynamic Thresholds Specified?**

A circuits dynamic threshold characteristics are quantified with the specifications  $V_{IHD}$  and  $V_{ILD}$ , where the “D” appendage stands for “dynamic”. The definitions are as below:

- $V_{IHD}$   
The minimum HIGH input level such that normal switching/functional characteristics are observed during output transients.
- $V_{ILD}$   
The maximum LOW input level such that normal switching/functional characteristics are observed during output transients.

**How are Dynamic Thresholds Characterized?**

The characterization of dynamic thresholds requires some planning for each product. The test will vary depending upon which edge will generate the supply noise; i.e., is the edge an LH or a ZL? Is the test for a data or control pin? This section discusses the planning process for testing an 74ACQ244, 74ACQ374, and an 74ACT534. From this discussion the reader should be able to test other products and understand FACT Quiet Series dynamic noise specifications.

*Test Fixturing / Setup:* Dynamic threshold tests are sensitive to the test configuration. The same considerations used to measure AC propagation delays should be exercised. ON Semiconductor uses the same fixturing for both AC propagation delay and noise testing. The inputs for this test are driven with a word generator running at 1 MHz which has been deskewed such that no more than 150 ps exists between signal edges. FACT Quiet Series specifies  $V_{IHD}/V_{ILD}$  at 25°C with  $V_{DD}$  at 5.0 V. For CMOS, true worst case exists where ground bounce is maximized, at cold temperature high  $V_{DD}$ . Bipolar circuits are not as straightforward; the threshold has a temperature coefficient which tracks  $V_{BE}$  and can change nearly a volt from -55°C to +125°C. The temperature and  $V_{DD}$  that create worst case bounce may not induce worst case  $V_{IHD}/V_{ILD}$ .

Each product subject to  $V_{IHD}/V_{ILD}$  testing will have multiple test possibilities. Through the case studies below, the reader should gain an understanding for some of the test trade-offs.

*Case 1:*

Product = 74ACTQ244

## Test Data Pins with LH/HL Transitions

The algorithm for this test is as follows. Maximize the number of outputs switching,  $N$ , in this case 8.  $N - 1$  of the inputs will transition to and from non threshold levels,  $0\text{ V} - 3\text{ V}$ . The last input will transition from  $3\text{ V}$  to  $V_{ILD}$  or from  $0\text{ V}$  to  $V_{IHD}$ . It should be noted that values of  $V_{ILD}$  and  $V_{IHD}$  that induce failure will vary as test pin location is varied. This is due mostly to voltage drops on the internal power bussing. As a result, pins farthest from the ground pin, and sometimes the  $V_{CC}$  pin, are likely to be worst case pins.

*Case 2:*

Product = 74ACTQ244

## Test Data Pins with ZL/ZH Transitions

This test will ramp the enable pin from  $3\text{ V} - 0\text{ V}$  while holding the input under test at threshold, i.e., have all outputs transition to ZL, with  $N - 1$  inputs at  $0\text{ V}$  and the input under test at  $V_{ILD}$ . The other tests are as follows:  $N - 1$  transition to ZL under test (PUT) at  $V_{IHD}$ , all outputs going ZH and PUT at  $V_{IHD}$ , and  $N - 1$  at ZH transition and PUT at  $V_{ILD}$ .

*Case 3:*

Product = 74ACTQ244

## Test OE Pin with HL/LH Transitions

$V_{ILD}$  is the parameter to check here. Data inputs should be switching  $0\text{ V} - 3\text{ V}$  while the OE pin is being stepped up from  $0\text{ V}$  to  $V_{ILD}$ . While testing the OE pin with an LH output transition, the standard  $50\text{ pF}$  capacitor in parallel with  $500\ \Omega$  output load can be used. When testing with an HL on the output, the 3-STATE ZL/LZ  $500\ \Omega$  to  $V_{CC} * 2$  should be used. Without the pull-up resistor, failure cannot be detected. The LZ and HZ edges create supply noise by switching off currents being sourced or sunk by the device. With standard AC loading, transients are much less than those of the other edges. Therefore,  $V_{IHD}$  for the chip is guaranteed by the data pins.

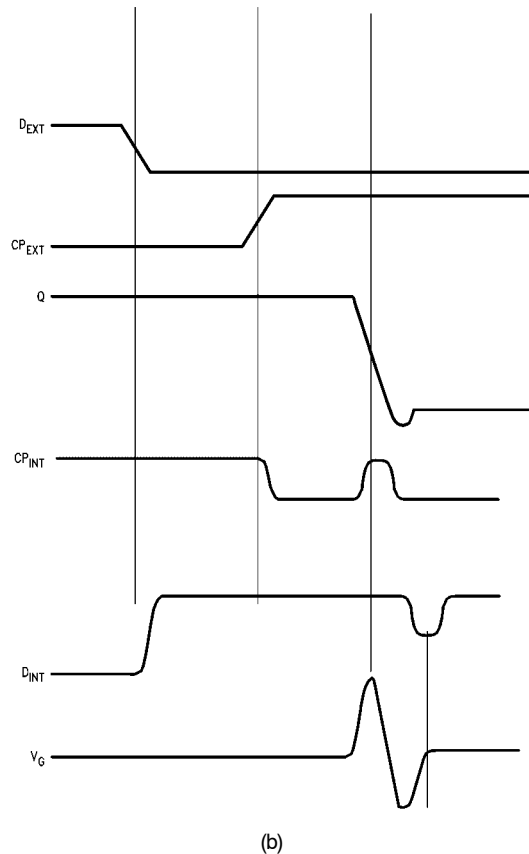
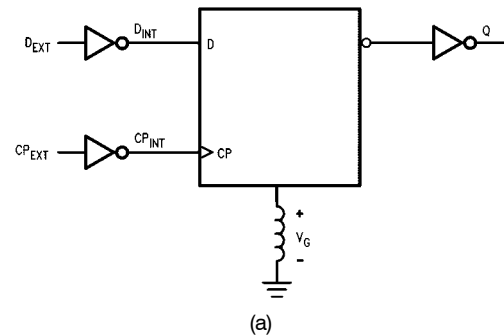
The test cases discussed in cases 1 – 3 are all possible test methods. Note there are other possible combinations. In practice ON Semiconductor has found that tests done in conjunction with HL transitions are worst case and will guarantee  $V_{ILD}$  and  $V_{IHD}$  for the chip.

*Case 4:*

Product = 74ACTQ374

This function, the non-inverting register, will have very good data and clock pin dynamic threshold characteristics. For instance, take the worst case bounce where all outputs are changing HL. To accomplish this, all inputs are LOW on the active edge of clock. If a  $V_{IHD}$  test of the clock is to be tested, the positive ground bounce at some level of  $V_{IHD}$  will stimulate one, if not multiple, false clocks to occur. A failure is not detected because the false clock or clocks merely

regenerated an existing low output. The positive ground bounce had the effect of making the logic low data look lower. Associated with positive bounce is negative bounce. Negative bounce occurs on the HL transition after the positive bounce. If this negative bounce switches the internal data gate, setup and hold times have been violated and again failure is not detected. Reference Figure 5 for a representation of this scenario.



**Figure 5. Noise Relates to Dynamic Threshold**

The most rigorous test for the non-inverting flop-flop will be to have the clock held at  $V_{IHD}$ , data held HIGH, and all outputs transition ZL.

## Case 5:

Product = 74ACTQ534

Inverting products inherently have poorer  $V_{IHD}/V_{ILD}$  characteristics compared to non-inverting. While testing a 240 is straightforward, 534 testing and results require further consideration. While the output is changing, both data and clock are HIGH. If data is held HIGH and clock lowered, false clocks occur, but a failure is not detected. The reverse is also true, as data is lowered, the data gate changes, but no clocks occur. However, as both data and clock HIGH levels are lowered simultaneously a window of  $V_{IHD}$  failure will be observed.

Figure 6 plots this “window of failure”. This plot will be examined by sweeping from right to left. It can be seen that for clock  $V_{IHD}$  levels down to approximately 2.7 V, proper data continues to clock out for data levels down to 1.5 V, the static threshold value. For all  $V_{IHD}$  voltages of the clock below 2.7 V, false clocking exists. If data is raised high enough, no internal data changes occur and therefore no failures. As data is lowered, internal data pulses down (Figure 7). The initial internal pulses may not cause device failure either because the voltage has not dropped to a valid logic level or because setup and hold times to the master latch have not been satisfied, but eventually failures are observed. It is interesting to note that were the 74ACT534 to have a more positive hold time (its hold time is slightly negative) the data voltage inducing failure would be much lower.

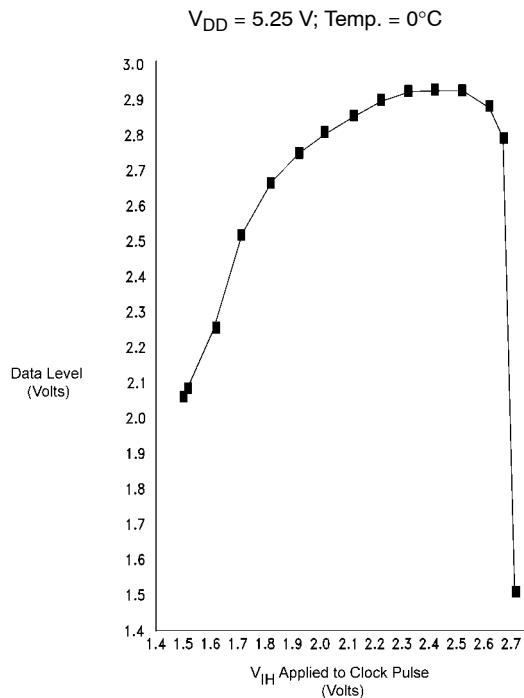


Figure 6. 74ACT534 Data/Clock  $V_{IH}$  Noise Margin

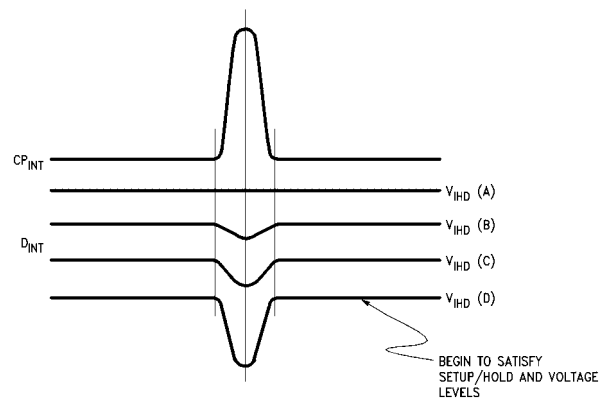


Figure 7. Data Input Level Can Cause Output Errors

The implication of the data in Figure 6 is that if the high voltage levels droop to approximately 2.9 V on data and 2.7 V on the clock simultaneously, a system failure is possible. How can these conditions exist at the same time? The temperature of Figure 6 is  $0^\circ\text{C}$ , if the inputs are driven by TTL drivers at a  $V_{DD} = 4.5 \text{ V}$ , a  $V_{OH}$  of 2.6 V is possible. However, the  $V_{CC}$  of the plot is 5.25 V. Assuming the drivers are TTL chips and are on the supply bus, the HIGH levels will be greater than 2.6 V. There is another variable to be considered before stating that no problem exists: what termination scheme is being used? If both data and clock signals come from transmission lines using either parallel or thevenin termination, HIGH voltage levels below 2.6 V are possible. If either or both of the signals are not terminated, series terminated, or AC terminated then functionality is assured.

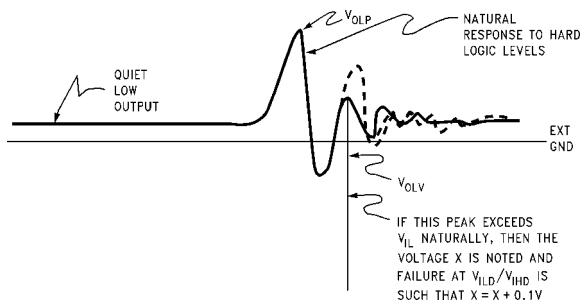
#### How Do Dynamic Threshold Problems Manifest Themselves?

There are a number of modes of failure found during dynamic threshold testing. Firstly, the part can malfunction through a state change. Also possible are oscillations, glitches, AC delay changes, and slew rate degradation. Failure criteria are as follows.

- On an output conditioned LOW, the LOW level will not rise above a LOW TTL threshold LOW (0.8 V), after the transition of the output.
- On a HIGH output the HIGH level will not drop below a CMOS threshold HIGH, (3.5 V at  $V_{DD} = 5.0 \text{ V}$ ), after the transition of the output.
- If the natural ringing, other than initial switching rail bounce, of the output violates the previous two criteria then the ringing amplitude will be noted. Failure is then defined as a 100 mV movement in the output toward the threshold from the peak ringing amplitude, (Figure 8).
- Gross failures will include functional state changes, oscillations, AC delay changes, and slew rate effects.

**How Do Dynamic Threshold Problems Affect Different Functions?**

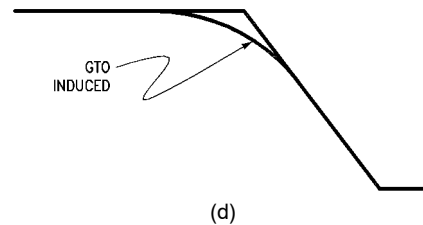
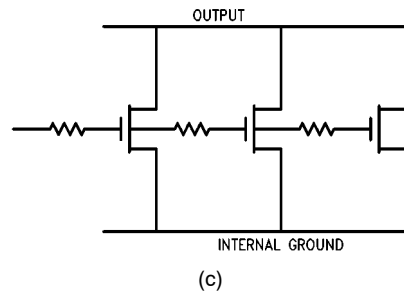
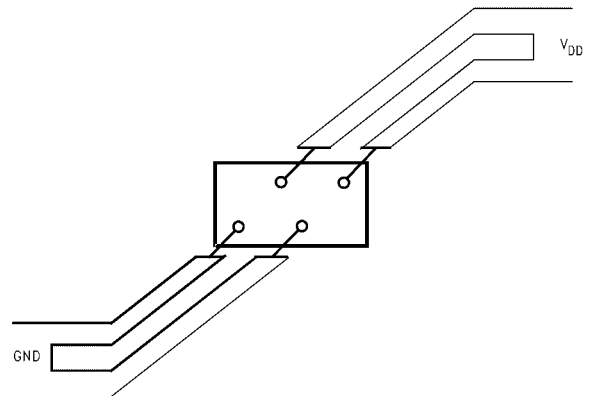
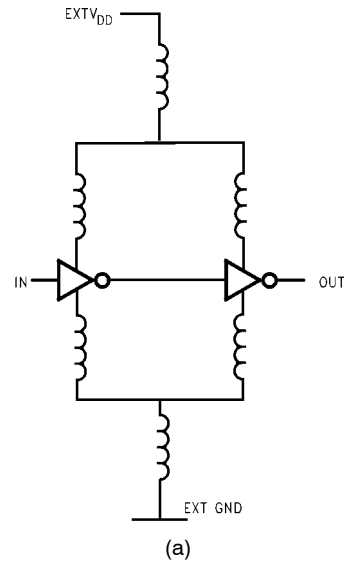
All the products discussed thus far pass the FACT Quiet Series dynamic threshold limits of  $V_{IHD} = 2.2\text{ V}$  and  $V_{ILD} = 0.8\text{ V}$ , which are specified as being tested singularly. The case of the 74ACT534 represents one where much effort was required to observe the failure mode. There are classes of product that will display clock  $V_{IHD}$  failures readily. These would be products which toggle the outputs independent of data. The most common functions in the list would be counters and shift registers. If the 74ACT299 shift register clock pin were tested, the initial clock edge would shift data inducing ground bounce. If the clock  $V_{IHD}$  is low enough, it can be observed that false clocks will continue until all outputs are in the same logic state as the serial data pin.



**Figure 8. Ground Bounce Causes Dynamic Threshold**

**What Does FACT Quiet Series Do to Address Dynamic Thresholds?**

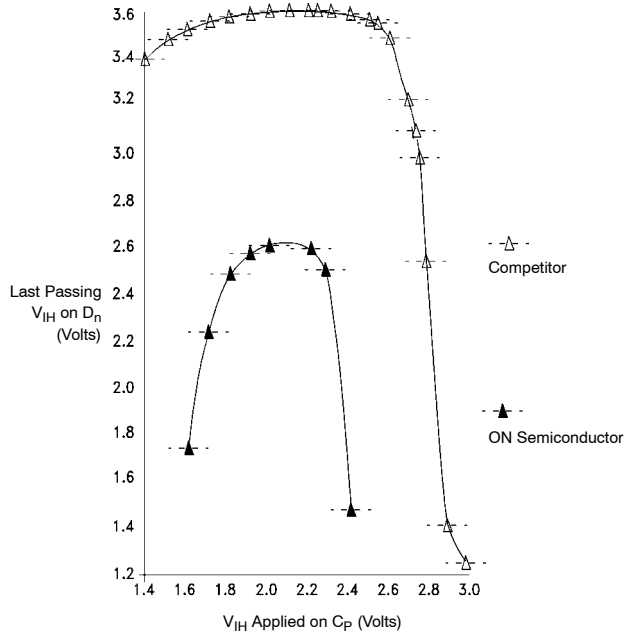
The FACT Quiet Series product utilizes two technical innovations to accomplish its performance. First, by using a split ground bus configuration, input and output grounds are given a degree of isolation. Schematically this is shown in Figure 9a and Figure 9b. The ground bus for inputs stages and outputs sections are separated on chip and only connected by the common inductance near the shoulder of the package and a mutual inductance between the lead frame fingers. Note, the input and output  $V_{DD}$  busses are electrically shorted on chip by the substrate resistance. The lead frame inductance forms a voltage divider such that the input only sees a percentage of the output ground noise. Secondly, a proprietary GTO technology, shown in Figure 9c, is used to shape the output edge. This then yields an output voltage waveform shown in Figure 9d. The soft turn-on of the output attenuates the  $dv/dt$ , and therefore the  $di/dt$  presented to the ground inductance is reduced, yielding a reduction in the ground noise.



**Figure 9. Noise Reduction Techniques**


## How Does ON Semiconductor Compare with Other Vendors?

The characteristics of ON Semiconductor's FACT Quiet Series ensure superior dynamic threshold performance in conventional corner pin packaging. The split power rail technology used to isolate inputs and outputs addresses a noise issue which goes unresolved in multiple power pin ACL logic families, and most single pin families. Referencing the 74ACT534 already discussed, Figure 10 shows one of the dramatic differences created by the FACT Quiet Series technology.



**Figure 10. Inverting Function Data/Clock  $V_{IH}$  Noise Margin Competitor vs. ON Semiconductor 5.0 V  $V_{DD}$  at 25°C**

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