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AN-6609

Selecting the Best JFET for Your Application

Introduction

This application note contains design curves for all of Fairchild Semiconductor discrete JFET processes. JFET process characteristics provide complete information on all processes, including all parts manufactured from a particular process. This can greatly aid device selection or substitution. In all cases, temperature and V_{GS}(off) distribution data is provided to facilitate worst-case design. In addition, a complete list of all device types supplied from this process is included to aid in cross reference searches and the selection of preferred device types. Preferred parts are shown with gray overprinting. The curves in this section should be considered typical of the process supplied by Fairchild Semiconductor. Every effort is made to keep the process in tolerance with the published graphs, but the exact distribution of any specific lot of material is not guaranteed.

How to use the Application Note

The following suggested procedure will help you find the device you need.

Part Number Known: Go to the Fairchild web site and type in the part number. If alternate type is required, refer to the online cross reference guide.

Specification Known: Refer to Figure 2, "JFET Process Family Tree" on page 4 of this application note to find the most compatible process. Then turn to Figure 3, “JFET Process Comparison Curves”, on page 6 to compare the specifications of each process type. Finally, turn to page 16 for a detailed listing of process characteristics and specific device type numbers available in that process. Take special note of preferred part types. Full data sheets are available on line.

Application Known: Turn to "Choose the Proper FET" and Figure 2, "JFET Process Tree" on page 4. Also Table 2, “Advantages of Using JFET by Application on page 3. Finally, refer to 0, “Applications and Their Parameters in Approximate Order of Importance” on page 2 as needed.

None of the Above: Contact local representative or regional office for assistance.

JFET Application Guide

Fairchild Semiconductor manufactures a broad line of silicon junction field effect transistors (JFETs). Fairchild’s JFETs provide excellent performance in many application areas such as RF amplifiers, analog switching low input current amplifiers, ultra low noise amplifiers and outstanding matched duals for operational amplifiers input applications.

Table 1 is a guide to enable the user to determine what parameters are important in each application. This followed by a listing of JFET Parameter Relationships in Figure 1. Table 2 lists many application advantages of JFETs by application.

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Table 1. Applications and Their Parameters in Approximate Order of Importance

LOW FREQUENCY AMPLIFIER	SOURCE FOLLOWER	ELECTROMETER AMPLIFIERS	LOW DRIFT AMPLIFIER	LOW NOISE AMPLIFIER	HIGH FREQUENCY AMPLIFIER	OSCILLATOR	DIFFERENTIAL AMPLIFIER	ANALOG AND DIGITAL SWITCHING
Y_{fs}	Y_{fs}	I_G	I_{DZ}	e_n	$Re(Y_{fs})$	Y_{fs}	$\lvert V_{GS1}-V_{GS2}\rvert$	$r_{DS(ON)}$
I_{DSS}	I_G	Y_{fs}	Y_{fs} @ I_{DZ}	I_G, i_n	$Re(Y_{is})$	I_{DSS}	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	$I_{D(OFF)}$
$V_{GS(OFF)}$	C_{rss}	I_{DZ}	V_{GS} @ I_{DZ}	Y_{fs}	NF	C_{rss}		C_{iss}
C_{iss}	C_{iss}	e_n	I_G	I_{DSS}	C_{rss}	C_{iss}	$\lvert I_{G1}-I_{G2}\rvert$	C_{rss}
C_{rss}	I_{DSS}	g_{os}	BV_{GSS}	$V_{GS(OFF)}$	$Re(Y_{os})$	$V_{GS(OFF)}$	I_G	$V_{GS(OFF)}$
e_n	$V_{GS(OFF)}$				I_{DSS}	BV_{GSS}	Y_{fs}	BV_{GSS}
BV_{GSS}	BV_{GSS}				$V_{GS(OFF)}$		Y_{fs1}/Y_{fs2}	
							$\lvert Y_{os1}-Y_{os2}\rvert$	
							CMRR	
							$V_{GS(OFF)}$	

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

Variation of drain current with gate bias. Square low transfer characteristic.

$$V_{GS(OFF)} = \frac{2\,I_{DSS}}{g_{fso}}$$

Gate-source cutoff voltage in terms of I_{DSS} and g_{fso}.

$$V_{GS}=V_{GS(OFF)}\left(1-\left(\frac{I_D}{I_{DSS}}\right)^{1/2}\right)$$

Gate-source voltage in terms of operating current I_D, I_{DSS}, and $V_{GS(OFF)}$.

$$g_{fso} = K\,\frac{I_{DSS}}{V_{GS(OFF)}}$$

Transconductance at zero gate voltage in terms of I_{DSS} and $V_{GS(off)}$. $K = 1.1$ to 2.5. Typically 2 for N-channel JFETs.

$$g_{fs} = g_{fso}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)$$

Variation in transconductance with gate bias.

$$g_{fs} = g_{fso}\sqrt{I_D/I_{DSS}}$$

Variation in transconductance with drain current.

$$r_{DS} \approx \frac{1}{g_{fs}}$$

Relationship between r_{DS} and g_{fs} in the triode region (i.e., $V_{DS} < V_{GS(OFF)}$).

$$r_{DS} \approx \frac{r_{DS(0)}}{1-\frac{V_{GS}}{V_{GS(OFF)}}}$$

Variation of drain resistance with gate bias in terms zero bias resistance (r_{DSO}) and $V_{GS(OFF)}$.

$$r_{DS} \approx \frac{K\,V_{GS(OFF)}^2}{I_{DSS}(V_{GS(OFF)}-V_{GS})}$$

$$K = 0.5 - 0.9$$

Variation of drain resistance in terms of V_{GS}, and $V_{GS(OFF)}$ I_{DSS}.

$$r_{DST} \approx r_{DS} @ 25^\circ C\ (1 + 0.007\,(\Delta T))$$

Variation of ON resistance as a function of temperature.

Figure 1. JFET Parameter Relationships

Table 2. Advantages of JFET by Application

APPLICATION	ADVANTAGES	FINAL ASSEMBLY WHERE USED
DC Amplifiers	High Z_{in} Low drift duals Low noise	Transducers, military guidance systems, control systems, temp indicators, multimeters
Low frequency amplifiers	Small coupling capacitors Low noise, distortion High input impedance	Sound detection, microphones, inductive transducers, hearing aids, high impedance transducers
Operational amplifiers	Summing point essentially zero. Low device noise. Less loading of transducers	Control systems, potted op amps, test equipment, medical electronics
Medium and high frequency amplifiers	Low cross modulation Low device noise Simplified circuitry	FM tuners, communication received scope inputs, most instrumentation equipment, high impedance inputs
Mixers – 100 MHz and up	Low mixing noise Low cross modulation	FM tuners, communication receivers
Oscillators	Low drift	Transmitters, receivers, organ
Logic gates	Virtually infinite fan in Simplified circuitry Zero storage time Symmetrical	Guidance controls, computer market mini military teaching aids, traffic control, telemetry
Choppers	Zero offset Low leakage currents Simplified circuitry Eliminates input transformers	Op amp modules guidance controls instrumentation equipment
AD Converters Multiplex switching (arrays) and sample hold	Improved isolation of input and output. Zero offset. Symmetrical. Low resistance Simplified circuitry	Control system, DVM's and any read-out equipment, medical electronics
Relay contact replacement	Solid state reliability Zero offset, High isolation Symmetrical No inductive spring No contact bounce High repetition rate	Test equipment, airborne equipment instrumentation market
Voltage variable resistor	Symmetrical Solid state reliability Functions as variable resistor. Low noise. High isolation Improved resolution	Organ, tone controls, control ckts to input operational amplifiers
Current limiters Sources	Two lead simplicity Wide selection range Low voltage operation	Hybrid circuits, amplifiers, power supply protection, timing ckts, voltage regulators

Choose the Proper JFET

Fairchild Semiconductor utilizes 17 different JFET geometries to cover, without compromise, the full spectrum of applications. Specific part number characteristics are summarized into application areas further on within this app note. In addition, this app note includes process comparison charts which graphically indicate the typical values of a given parameter for all geometries under identical test conditions. Detailed data on each process, along with a list of all part numbers manufactured from each process, is also supplied.

Figure 2, gives a look at the characteristics for each process type to help the designer select the process that best meets his requirements. Table 3 shows which application the process was designed to best serve. After narrowing down the process types, it is suggested that the process sheets and specific part number characteristics be consulted.

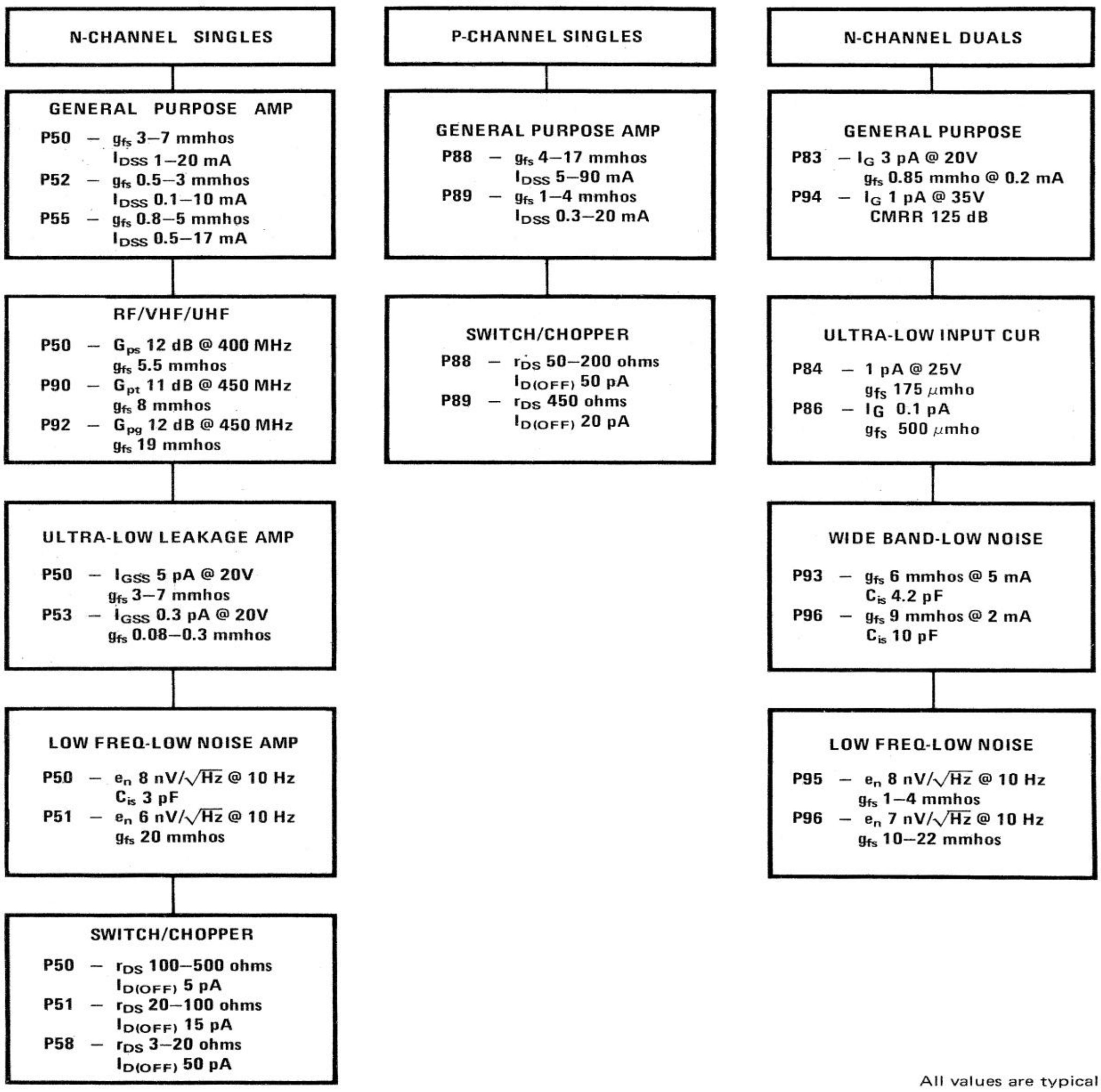


Figure 2. The JFET Process Family Tree

Table 3. Part Number and Process Application Recommendations

POPULAR PRODUCT TYPES	2N4416, 2N5485, 6 PN4416, PN4302–4	2N4856–61, 2N4391–3 PN4856–61, PN4391–3	2N4338–41, 2N3684–7	2N4117–9, 2N3452–4 2N4117A–19A	2N3821–2, 2N4221–2 2N5457–9	2N5432–4	2N5196–9, 2N5545–7 2N3954–8	2N5902–9	U421–U426	2N5018–21, P1086–7E 2N5114–6	2N2608–9, 2N5460–62	2N5397, J300	U308–10, J308–10	2N5911–12	NDF9401–10	2N5515–24, 2N6483–5	2N5564–6	2N5561–63
PROCESS DESIGNATION	**50**	**51**	**52**	**53**	**55**	**58**	**83**	**84**	**86**	**88**	**89**	**90.**	**92**	**93**	**94**	**95**	**96**	**98**
Low Current Amplifier			S	P	S		P	P	P		P				P	P		P
Low Freq Ampli $\leq$ 100 Hz			S		S		P			S	S				P	P		P
High Freq Ampli $>$ 100 MHz	P											P	P	P			P	
General Purpose Amplifier	P		P		P						P							
Low Noise Amp (10 Hz $\overline{e}_n$)	S	S			S	S	P								P	P	P	P
Low Noise Amp $>$ 50 MHz	P				S							P	P	P			P	
High Frequency Mixer	P											P	P					
Dual Diff Pair							P	P	P					P	P	S	P	P
AGC Amplifier	P				P													
Electrometer Preamp				P				P	P						P			S
Microvolt Amplifier				P				P	P						P			P
Low Leakage Diode				P														
Diff/Angle Ended Inp. Stag.							P	P	P					P	P		P	P
Active Filter	P		S		P						S							
Oscillator	P		S		P						S	P	P					
Voltage Variable Resistor	P	P	S		P					P	P							P
Hybrid Chips	P	P		P	P		P	P	P	P	P				P			
Analog/Digital Switch		P				P				P							S	S
Multiplexing	P	P			S	S				P								
Choppers		P				P				P							P	
Nixie Drivers																		
Reed Relay Replacement						P												
Sub pA Dual Diff Pair								P	P									
Sample-Hold	P	P			S				S	P								P
Buffer Interface to CMOS										P	P							
Matched Switch							S							S	S		P	P
HF $\geq$ 400 MHz Prime												P	P					
Current Limiter		P								P								
Current Source			P	S	P						S							

P — Prime Choice S — Secondary (Alternate) Choice

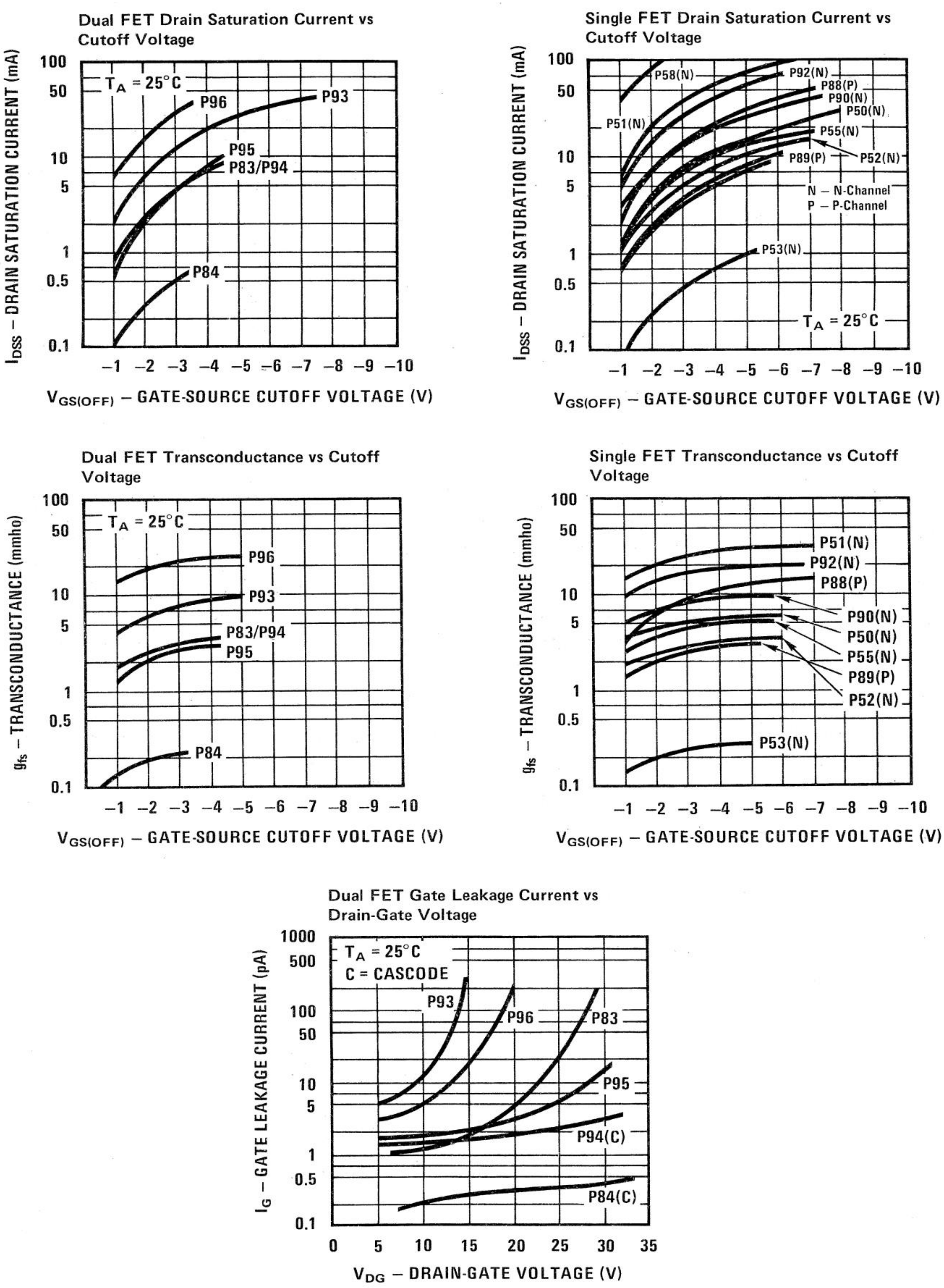
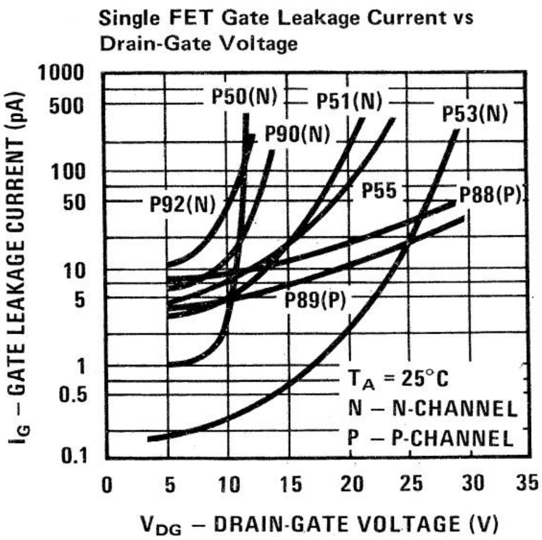
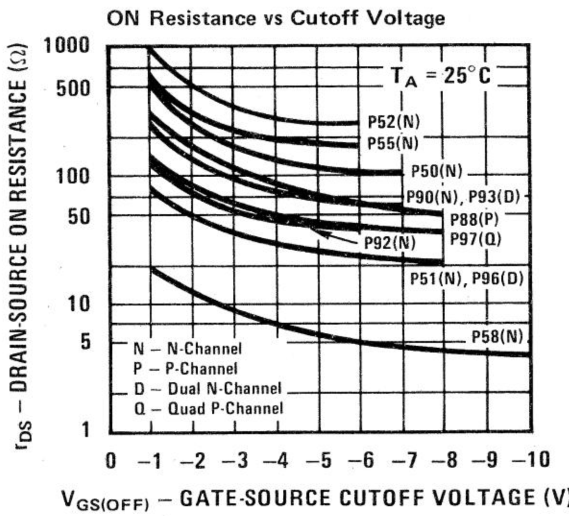
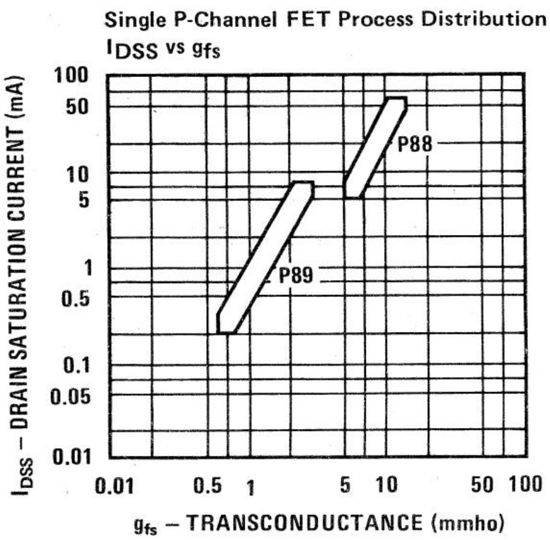
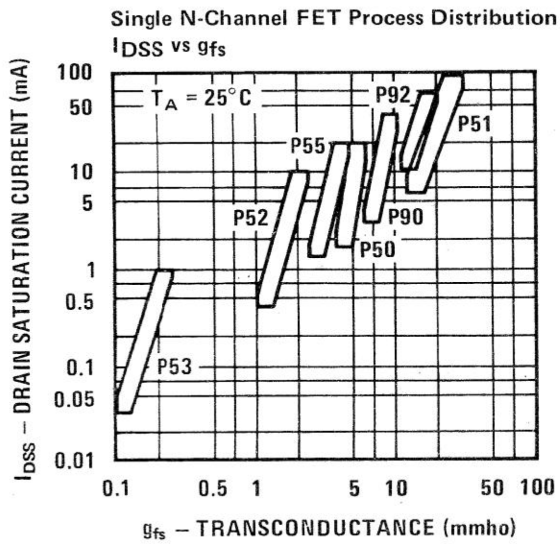


Figure 3. JFET Process Comparison Curves









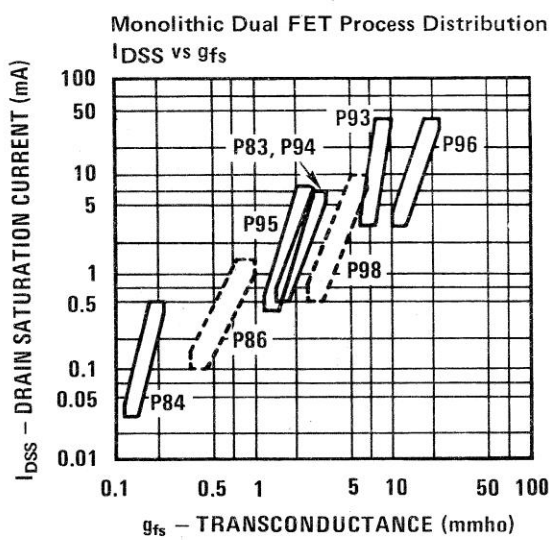


Figure 4. JFET Process Comparison Curves (Continued)

JFET Characteristic Selection Guide

Table 4. N-Channel Selection Guide: Switches and Choppers

Type No.	BV_{GSS} BV_{GDO} (V) Min	@ I_G (μA)	I_{GSS} *I_{DGO} (nA) Max	@ V_{DG} (V)	$I_{D(off)}$ (nA) Max	@ V_{DS} (V)	V_{GS} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	$r_{ds(on)}$ (Ω) Max	@ I_D (mA)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	t_{on} (ns) Max	t_{off} (ns) Max	Process No.
2N3824	50	1	0.1	30	0.1	15	−8		8	15	1				250		6	15	0	3	0	−8			55
2N3966	30	1	1	20	0.1	10	−7	4	6	10	10	2		20	220		6	20	0	1.5	0	−7			50
2N3970	40	1	0.25*	20	0.25	20	−12	4	10	20	1	50	150	20	30	1	25	20	0	6	0	−12	20	30	51
2N3971	40	1	0.25*	20	0.25	20	12	2	5	20	1	25	75	20	60	1	25	20	0	6	0	−12	30	60	51
2N3972	40	1	0.25*	20	0.25	20	−12	0.5	3	20	1	5	30	20	100	1	25	20	0	6	0	−12	80	100	51
•2N4091	40	1	0.2*	20	0.2	20	−12	5	10	20	1	30		20	30	1	16	20	0	5	0	−20	25	40	51
•2N4092	40	1	0.2*	20	0.2	20	−8	2	7	20	1	15		20	50	1	16	20	0	5	0	−20	35	60	51
•2N4093	40	1	0.2*	20	0.2	20	−6	1	5	20	1	8		20	80	1	16	20	0	5	0	−20	60	80	51
2N4391	40	1	0.1	20	0.1	20	−12	4	10	20	1	50	150	20	30	1	14	20	0	3.5	0	−12	20	35	51
2N4392	40	1	0.1	20	0.1	20	−7	2	5	20	1	25	75	20	60	1	14	20	0	3.5	0	−7	20	55	51
2N4393	40	1	0.1	20	0.1	20	−5	0.5	3	20	1	5	30	20	100	1	14	20	0	3.5	0	−5	20	80	51
•2N4856	40	1	0.25	20	0.25	15	−10	4	10	15	.5	50		15	25		18	0	−10	8	0	−10	9	25	51
2N4856A	40	1	0.25	20	0.25	15	−10	4	10	15	.5	50		15	25		10	0	−10	4	0	−10	8	20	51
•2N4857	40	1	0.25	20	0.25	15	−10	2	6	15	.5	20	100	15	40		18	0	−10	8	0	−10	10	50	51
2N4857A	40	1	0.25	20	0.25	15	−10	2	6	15	.5	20	100	15	40		10	0	−10	3.5	0	−10	10	40	51
•2N4858	40	1	0.25	20	0.25	15	−10	0.8	4	15	.5	8	80	15	60		18	0	−10	8	0	−10	20	100	51
2N4858A	40	1	0.25	20	0.25	15	−10	0.8	4	15	.5	8	80	15	60		10	0	−10	3.5	0	−10	16	80	51
•2N4859	30	1	0.25	15	0.25	15	−10	4	10	15	.5	50		15	25		18	0	−10	8	0	−10	9	25	51
2N4859A	30	1	0.25	15	0.25	15	−10	4	10	15	.5	50		15	25		10	0	−10	4	0	−10	8	20	51
•2N4860	30	1	0.25	15	0.25	15	−10	2	6	15	.5	20	100	15	40		18	0	−10	8	0	−10	10	50	51
2N4860A	30	1	0.25	15	0.25	15	−10	2	6	15	.5	20	100	15	40		10	0	−10	3.5	0	−10	10	40	51
•2N4861	30	1	0.25	15	0.25	15	−10	0.8	4	15	.5	8	80	15	60		18	0	−10	8	0	−10	20	100	51
2N4861A	30	1	0.25	15	0.25	15	−10	0.8	4	15	.5	8	80	15	60		10	0	−10	3.5	0	−10	16	80	51
2N5432	25	1	0.2	15	0.2	5	−10	4	10	5	3	150		15	5	10	30	0	−10	15	0	−10	5	36	58
2N5433	25	1	0.2	15	0.2	5	−10	3	9	5	3	100		15	7	10	30	0	−10	15	0	−10	5	36	58
2N5434	25	1	0.2	15	0.2	5	−10	1	4	5	3	30		15	10	10	30	0	−10	15	0	−10	5	36	58
2N5555	25	10	1	15	10	12	−10		(10)			15		15	150		5	15	0	1.2	0	−10	10	25	50

• **Note.** JAN qualified per applicable MIL-S-19500 specification.

Type No.	BV_{GSS} BV_{GDO} (V) Min	@ I_G (μA)	I_{GSS} *I_{DGO} (nA) Max	@ V_{DG} (V)	$I_{D(off)}$ (nA) Max	@ V_{DG} (V)	V_{GS} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	$r_{ds(on)}$ (Ω) Max	@ I_D (mA)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	t_{on} (ns) Max	t_{off} (ns) Max	Process No.
2N5638	30	10	1	15	1	15	−12		(12)			50		20	30	1	10	0	−12	4	0	−12			51
2N5639	30	10	1	15	1	15	−8		(8)			25		20	60	1	10	0	−12	4	0	−8			51
2N5640	30	10	1	15	1	15	−6		(6)			5		20	100	1	10	0	−12	4	0	−6			51
2N5653	30	10	1	15	1	15	−12		(12)			40		20	50	1	10	0	−12	3.5	0	−12	9	15	51
2N5654	25	10	1	15	10	15	−8		(8)			15		20	100	1	10	0	−12	3.5	0	−8	14	30	51
J108	25	1	3	15	3	5	−10	3	10	5	1000	80		15	8	10	t30	0	−10	t15	0	−10	t5	t36	58
J109	25	1	3	15	3	5	−10	2	6	5	1000	40		15	12	10	t30	0	−10	t15	0	−10	t5	t36	58
J110	25	1	3	15	3	5	−10	.5	4	5	1000	10		15	18	10	t30	0	−10	t15	0	−10	t5	t36	58
J111	35	1	1	15	1	5	−10	3	10	5	1000	20		15	30	1	t10	0	−10	t5	0	−10	t13	t35	51
J112	35	1	1	15	1	5	−10	1	5	5	1000	5		15	50	1	t10	0	−10	t5	0	−10	t13	t35	51
J113	35	1	1	15	1	5	−10	.5	3	5	1000	2		15	100	1	t10	0	−10	t5	0	−10	t13	t35	51
J114	25	1	1	15	1	5	−10	3	10	5	1000	15		15	150	1	t4	0	−10	t2	0	−10	t6	t20	90
PN4091	40	1	1*	20	1	20	−12	5	10	20	1	30		20	30		16	20	0	5	20	0	25	40	51
PN4092	40	1	1*	20	1	20	−8	2	7	20	1	15		20	50		16	20	0	5	20	0	35	60	51
PN4093	40	1	1*	20	1	20	−6	1	5	20	1	8		20	80		16	20	0	5	20	0	60	80	51
PN4391	40	1	1	20	1	20	−12	4	10	20	1	50	150	20	30		14	20	0	3.5	0	−12	20	35	51
PN4392	40	1	1	20	1	20	−7	2	5	20	1	25	75	20	60		14	20	0	3.5	0	−7	40	80	51
PN4393	40	1	1	20	1	20	−5	0.5	3	20	1	5	30	20	100		14	20	0	3.5	0	−5	55	130	51
PN4856	40	1	1	20	1	15	−10	4	10	15	.5	50		15	25		18	0	−10	8	0	−10	9	25	51
PN4857	40	1	1	20	1	15	−10	2	6	15	.5	20	100	15	40		18	0	−10	8	0	−10	10	50	51
PN4858	40	1	1	20	1	15	−10	0.8	4	15	.5	8	80	15	60		18	0	−10	8	0	−10	20	100	51
PN4859	30	1	1	15	1	15	−10	4	10	15	.5	50		15	25		18	0	−10	8	0	−10	9	25	51
PN4860	30	1	1	15	1	15	−10	2	6	15	.5	20	100	15	40		18	0	−10	8	0	−10	10	50	51
PN4861	30	1	1	15	1	15	−10	0.8	4	15	.5	8	80	15	60		18	0	−10	8	0	−10	20	100	51
TIS73	30	1	2	15	2	15	−10	4	10	15	4	50		15	25		18	0	−10	8	0	−10	9	25	51
TIS74	30	1	2	15	2	15	−10	2	6	15	4	20	100	15	40		18	0	−10	8	0	−10	10	50	51
TIS75	30	1	2	15	2	15	−10	0.8	4	15	4	8	80	15	60		18	0	−10	8	0	−10	20	100	51
U1897E	40	1	0.2*	20				5	10	20	1	30		20	30	1	16	20	0	5	0	−20	25	40	51
U1898E	40	1	0.2*	20				2	7	20	1	15		20	50	1	16	20	0	5	0	−20	35	60	51
U1899E	40	1	0.2*	20				1	5	20	1	8		20	80	1	16	20	0	5	0	−20	60	80	51

Table 5. N-Channel Selection Guide: RF, VHF, UHF Amplifiers

Type No.	BV_{GSS} BV_{GDO} (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (pA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	$R_e\|Y_{fs}\|$ (mmho) Min	@ Freq (MHz)	$R_e(Y_{os})$ (µmho) Max	@ f (MHz)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	NF (dB) @ R_G = 1k Max	Freq (MHz)	Process No.
2N3819	25	1	2	15		8	15	2	2	20	15	1.6	100			8	15	0	4	15	0			50
2N3823	30	1	0.5	20		8	15	.5	4	20	15	3.2	200	200	200	6	15	0	2	15	0	2.5	100	50
2N4223	30	10	0.25	20	0.1	8	15	.25	3	18	15	2.7	200	200	200	6	15	0	2	15	0	5	200	50
2N4224	30	10	0.5	20	0.1	8	15	.5	2	20	15	1.7	200	200	200	6	15	0	2	15	0			50
2N4416	30	1	0.1	20		6	15	1	5	15	15	4	400	100	400	4	15	0	0.8	15	0	4	400	50
•2N4416A	35	1	0.1	20	2.5	6	15	1	5	15	15	4	400	100	400	4	15	0	0.8	15	0	4	400	50
2N5078	30	1	0.25	20	0.5	8	15		4	25	15	4	200	150	200	6	15	0	2	15	0	3	200	50
2N5245	30	1	1	20	1	6	15	10	5	15	15	4	400	100	400	4.5	15	0	1	15	0	4	400	90
2N5246	30	1	1	20	0.5	4	15	10	1.5	7	15	2.5	400	100	400	4.5	15	0	1	15	0			90
2N5247	30	1	1	20	1.5	8	15	10	8	24	15	4	400	150	400	4.5	15	0	1	15	0			90
2N5248	30	1	5	20	1	8	15	10	4	20	15	3	200	200	200	6	15	0	2	15	0			50
2N5397	25	1	0.1	15	1	6	10	1	10	30	10	5.5	450	200	450	5	10	10m	1.2	10	10m	3.5	450	90
2N5398	25	1	0.1	15	1	6	10	1	5	40	10	5.0	450	400	450	5.5	10	0	1.3	10	0	3.2	450	90
2N5484	25	1	1	20	0.3	3	15	10	1	5	15	2.5	100	75	100	5	15	0	1	15	0	3	100	50
2N5485	25	1	1	20	1	4	15	10	4	10	15	3	400	100	400	5	15	0	1	15	0	4	400	50
2N5486	25	1	1	20	2	6	15	10	8	20	15	3.5	400	100	400	5	15	0	1	15	0	4	400	50
2N5668	25	10	2	15	0.2	4	15	10	1	5	15	1	100	50	100	7	15	0	3	15	0	2.5	100	50
2N5669	25	10	2	15	1	6	15	10	4	10	15	1.6	100	100	100	7	15	0	3	15	0	2.5	100	50
2N5670	25	10	2	15	2	8	15	10	8	20	15	2.5	100	150	100	7	15	0	3	15	0	2.5	100	50
2N5949	30	1	1	15	3	7	15	100	12	18	15	3.0	100	75	100	6	15	0	2	15	0	5	100	50
2N5950	30	1	1	15	2.5	6	15	100	10	15	15	3.0	100	75	100	6	15	0	2	15	0	5	100	50
2N5951	30	1	1	15	2	5	15	100	7	13	15	3.0	100	75	100	6	15	0	2	15	0	5	100	50
2N5952	30	1	1	15	1.3	3.5	15	100	4	8	15	1.0	100	75	100	6	15	0	2	15	0	5	100	50
2N5953	30	1	1	15	.8	3	15	100	2.5	5	15	1.0	100	50	100	6	15	0	2	15	0	5	100	50
J300	25	1	0.5	15	1	6	10	1	6	30	10	4.5	.001	200	.001	5.5	10	5m	1.7	10	5m	t2	100	90
J304	30	1	0.1	20	2	6	15	1	5	15	15	t4.2	400	t80	100	t3	15	0	t.8	15	0	t4	400	50
J305	30	1	0.1	20	.5	3	15	1	1	8	15	t3.0	400	t80	100	t3	15	0	t.8	15	0	t4	400	50
J308	25	1	1	15	1	6.5	10	1	12	60	10	8	.001	200	.001	7.5	0	−10	2.5	0	−10	t1.5	100	92
J309	25	1	1	15	1	4.0	10	1	12	30	10	10	.001	200	.001	7.5	0	−10	2.5	0	−10	t1.5	100	92
J310	25	1	1	15	2	6.5	10	1	24	60	10	8	.001	200	.001	7.5	0	−10	2.5	0	−10	t1.5	100	92

• **Note.** JAN qualified per applicable MIL-S-19500 specification.

Type No.	BV_{GSS} BV_{GDO} (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (pA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	$R_e Y_{fs}$ (mMho) Min	@ Freq (MHz)	$R_e(Y_{os})$ (µMho) Max	@ f (MHz)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	NF (dB) @ R_G = 1k Max	Freq (MHz)	Process No.
MPF102	25	1	2	15		8	15	2	2	20	15	1.6	100	100	200	7	15	0	3	15	0			50
MPF106	25	1	1	20	0.5	4	15	.5	4	10	15	2.5	0.001			5	15	0	2	15	0	4	400	50
MPF107	25	1	1	20	2	6	15	.5	8	20	15	4	0.001			5	15	0	1.2	15	0	4	400	50
MPF108	25	10	1	15	0.5	8	15	10µ	1.5	24	15	1.6	100	200	100	6.5	15	0	2.5	15	0	3	100	50
PN4223	30	1	0.25	20	0.1	8	15	1	3	18	15	2.7	200	200	200	6	15	0	2	15	0	5	200	50
PN4224	30	1	0.25	20	0.1	8	15	5	2	20	15	1.7	200	200	200	6	15	0	2	15	0			50
PN4416	30	1	0.1	20		6	15	1	5	15	15	4	400	100	400	4	15	0	0.8	15	0	4	400	50
U308	25	1	0.15	15	1	6	10	1	12	60	10	10	0.001	150	100	5	0	10m	2.5	0	10mA	t3	450	92
U309	25	1	0.15	15	1	4	10	1	12	30	10	10	0.001	150	100	5	0	10m	2.5	0	10mA	t3	450	92
U310	25	1	0.15	15	2.5	6	10	1	24	60	10	10	0.001	150	100	5	10	10m	2.5	10	10mA	t3	450	92
U312	25	1	0.1	15	1	6	10	1	10	30	10	6	0.001			3.8	10	10m	1.2	10	10mA	t3.5	450	90
U320	20	1	3	15	2	10	5	1m	100	500	15	75	0.001			30	0	10	15	0	10	t2.5	30	58
U321	25	1	3	15	1	4	5	1m	80	250	15	75	0.001			30	0	10	15	0	10	t2.5	30	58
U322	25	1	3	15	3	10	5	1m	200	700	15	75	0.001			30	0	10	15	0	10	t2.5	30	58

Table 6. N-Channel Selection Guide: Low Frequency – Low Noise Amplifiers

Type No.	BV_{GSS} (V) Min	@ I_G (μA)	I_{GSS} (nA) Max	@ V_{DG} (V)	$V_{GS(OFF)}$ (V) Min	$V_{GS(OFF)}$ (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	g_{fs} (Re|Y_{fs}) (mmho) Min	g_{fs} (mmho) Max	V_{DS} (V)	f (MHz)	G_{oss} (μmho) Max	V_{DS} (V)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	e_n nV/√Hz Max	@ f (Hz)	Process No.
2N4393	40	1.0	0.1	20	0.5	3.0	20	1.0	5.0	30	20	t12		20	0.001			14	20	0	3.5	5.0(GS)	t8.0	10	51
2N5556	30	10	0.1	15	0.2	4.0	15	1.0	0.5	2.5	15	1.5	6.5	15	0.001	20	15	6.0	15	0	3.0	15	35	10	50
2N5557	30	10	0.1	15	0.8	5.0	15	1.0	2.0	5.0	15	1.5	6.5	15	0.001	20	15	6.0	15	0	3.0	15	35	10	50
2N5558	30	10	0.1	15	1.5	6.0	15	1.0	4.0	10	15	1.5	6.5	15	0.001	20	15	6.0	15	0	3.0	15	35	10	50
NF5101	40	1	0.2	15	0.5	1.1	15	1.0	1.0	12	15	3.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51
NF5102	40	1	0.2	15	0.7	1.6	15	1.0	4.0	20	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51
NF5103	40	1	0.2	15	1.2	2.7	15	1.0	10	40	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51
PF5101	40	1	0.2	15	0.5	1.1	15	1.0	1.0	12	15	3.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51
PF5102	40	1	0.2	15	0.7	1.6	15	1.0	4.0	20	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51
PF5103	40	1	0.2	15	1.2	2.7	15	1.0	10	40	15	7.5		15	0.001	25	15	t12	15	0	t4	15	3.5	1k	51
PN4393	40	1.0	0.1	20	0.5	3.0	20	1.0	5.0	30	20	t12		20	0.001			14	20	0	3.5	5.0(GS)	t8.0	10	51

Table 7. N-Channel Selection Guide: Ultra Low Current Amplifiers

Transistor Type	BV_{GSS} BV_{GDO} (V) Min	@ I_G (μA)	I_{GSS} I_{DGO} (pA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (μA) Min	I_{DSS} (μA) Max	@ V_{DS} (V)	G_{fs} (μmho) Min	G_{fs} (μmho) Max	@ V_{DS} (V)	G_{oss} (μmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ f (Hz)	Process No.
2N4117	40	1	10	20	0.6	1.8	10	1	30	90	10	20	210	10	3	10	3	10	0	1.5	10	0			53
2N4117A	40	1	1	20	0.6	1.8	10	1	30	90	10	70	210	10	3	10	3	10	0	1.5	10	0			53
2N4118	40	1	10	20	1	3	10	1	80	240	10	80	250	10	5	10	3	10	0	1.5	10	0			53
2N4118A	40	1	1	20	1	3	10	1	80	240	10	80	250	10	5	10	3	10	0	1.5	10	0			53
2N4119	40	1	10	20	2	6	10	1	200	600	10	100	330	10	10	10	3	10	0	1.5	10	0			53
2N4119A	40	1	1	20	2	6	10	1	200	600	10	100	330	10	10	10	3	10	0	1.5	10	0			53

Table 8. N-Channel Selection Guide: General Purpose Amplifiers

Transistor Type	BV_{GSS} $^*BV_{GDO}$ (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (nA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ VDS (V)	G_{fs} (mmho) Min	G_{fs} (mmho) Max	@ V_{DS} (V)	G_{oss} (µmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ Freq (Hz)	Process No.
2N3069	*50	1	1	30		9.5	30	1000	2	10	30	1	2.5	30	80	30	15	0	−12	1.5	30	0	125	1000	52
2N3070	*50	1	1	30		4.5	30	1000	0.5	2.5	30	0.75	2.5	30	30	30	15	0	−8	1.5	30	0	125	1000	52
2N3368	*40	1	5	30		11.5	20	1000	2	12	30	1	4	30	80	30	20	8	0	3	30	0			52
2N3369	*40	1	5	30		6.5	20	1000	0.5	2.5	30	0.6	2.5	30	30	30	20	8	0	3	30	0			52
2N3370	*40	1	5	30		3.2	20	1000	0.1	0.6	30	0.3	2.5	30	15	30	20	8	0	3	30	0			52
2N3436	*50	1	0.5	30		9.8	20	1000	3	15	20	2.5	10	20	35	30	18	0	−10	6	30	0	100	1000	55
2N3437	*50	1	0.5	30		4.8	20	1000	0.8	4	20	1.5	6	20	20	30	18	0	−6	6	30	0	100	1000	55
2N3438	*50	1	0.5	30		2.3	20	1000	0.2	1	20	0.8	4.5	20	5	30	18	0	−4	6	30	0	100	1000	55
2N3458	*50	1	0.25	30		7.8	20	1000	3	15	20	2.5	10	20	35	30	18	0	−10	5	30	0	225	20	52
2N3459	*50	1	0.25	30		3.4	20	1000	0.8	4	20	1.5	6	20	20	30	18	0	−6	5	30	0	155	20	52
2N3460	*50	1	0.25	30		1.8	20	1000	0.2	1	20	0.8	4.5	20	5	30	18	0	−4	5	30	0	155	20	52
2N3684	50	1	0.1	30	2	5	20	1	2.5	7.5	20	2	3	20	50	20	4	20	0	1.2	20	0	150	100	52
2N3685	50	1	0.1	30	1	3.5	20	1	1	3	20	1.5	2.5	20	25	20	4	20	0	1.2	20	0	150	100	52
2N3686	50	1	0.1	30	0.6	2	20	1	0.4	1.2	20	1	2	20	10	20	4	20	0	1.2	20	0	150	100	52
2N3687	50	1	0.1	30	0.3	1.2	20	1	0.1	0.5	20	0.5	1.5	20	5	20	4	20	0	1.2	20	0	150	100	52
2N3821	50	1	0.1	30		4	15	.5	0.5	2.5	15	1.5	4.5	15	10	15	6	15	0	3	15	0	200	10	55
2N3822	50	1	0.1	30		6	15	.5	2	10	15	3	6.5	15	20	15	6	15	0	3	15	0	200	10	55
2N3967	30	1	0.1	20	2	5	20	1	2.5	10	20	2.5		20	35	20¶	5	20	¶	1.3	20	♠	84	100	50
2N3967A	30	1	0.1	20	2	5	20	1	2.5	10	20	2.5		20	35	20¶	5	20	¶	1.3	20	♠	160	10	50
2N3968	30	1	0.1	20		3	20	1	1	5	20	2		20	15	20**	5	20	**	1.3	20	†	84	100	50
2N3968A	30	1	0.1	20		3	20	1	1	5	20	2		20	15	20**	5	20	**	1.3	20	†	160	10	50
2N3969	30	1	0.1	20		1.7	20	1	0.4	2	20	1.3		20	5	20††	5	20	††	1.3	20	¶	84	100	50
2N3969A	30	1	0.1	20		1.7	20	1	0.4	2	20	1.3		20	5	20††	5	20	††	1.3	20	¶	160	10	50

♠I_D = 1 mA †I_D = 500µA ¶I_D = 250µA δI_D = 100µA **I_D = 100µA ††I_D = 40µA

Transistor Type	BV_{GSS} $^*BV_{GDO}$ (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (nA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ VDS (V)	G_{fs} (mmho) Min	G_{fs} (mmho) Max	@ V_{DS} (V)	G_{oss} (µmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ Freq (Hz)	Process No.
2N4220	30	10	0.1	15		4	15	.1	0.5	3	15	1	4	15	10	15	6	15	0	2	15	0			55
2N4220A	30	10	0.1	15		4	15	.1	0.5	3	15	1	4	15	10	15	6	15	0	2	15	0	115	100	55
2N4221	30	10	0.1	15		6	15	.1	2	6	15	2	5	15	20	15	6	15	0	2	15	0			55
2N4221A	30	10	0.1	15		6	15	.1	2	6	15	2	5	15	20	15	6	15	0	2	15	0	115	100	55
2N4222	30	10	0.1	15		8	15	.1	5	15	15	2.5	6	15	40	15	6	15	0	2	15	0			55
2N4222A	30	10	0.1	15		8	15	.1	5	15	15	2.5	6	15	40	15	6	15	0	2	15	0	115	100	55
2N4338	50	1	0.1	30	0.3	1	15	100	0.2	0.6	15	0.6	1.8	15	5	15	7	15	0	3	15	0	68	1000	52
2N4339	50	1	0.1	30	0.6	1.8	15	100	0.5	1.5	15	0.8	2.4	15	15	15	7	15	0	3	15	0	68	1000	52
2N4340	50	1	0.1	30	1	3	15	100	1.2	3.6	15	1.3	3	15	30	15	7	15	0	3	15	0	68	1000	52
2N4341	50	1	0.1	30	2	6	15	100	3	9	15	2	4	15	60	15	7	15	0	3	15	0	68	1000	55
2N5103	25	10	0.1	15	0.5	4	15	1	1	8	15	2	8	15	100	15	5	15	0	1	15	0	100	10	50
2N5104	25	1	0.1	15	0.5	4	15	1	2	6	15	3.5	7.5	15	100	15	5	15	0	1	15	0	50	10	50
2N5105	25	1	0.1	15	0.5	4	15	1	5	15	15	5	10	15	100	15	5	15	0	1	15	0			50
2N5358	40	1	0.1	20	0.5	3	15	100	0.5	1	15	1	3	15	10	15	6	15	0	2	15	0	115	100	55
2N5359	40	1	0.1	20	0.8	4	15	100	0.6	1.6	15	1.2	3.6	15	10	15	6	15	0	2	15	0	115	100	55
2N5360	40	1	0.1	20	0.8	4	15	100	0.5	2.5	15	1.4	4.2	15	20	15	6	15	0	2	15	0	115	100	55
2N5361	40	1	0.1	20	1	6	15	100	2.5	5	15	1.5	4.5	15	20	15	6	15	0	2	15	0	115	100	55
2N5362	40	1	0.1	20	2	7	15	100	4	8	15	2	5.5	15	40	15	6	15	0	2	15	0	115	100	55
2N5363	40	1	0.1	20	2.5	8	15	100	7	14	15	2.5	6	15	40	15	6	15	0	2	15	0	115	100	55
2N5364	40	1	0.1	20	2.5	8	15	100	9	18	15	2.7	6.5	15	60	15	6	15	0	2	15	0	115	100	55
2N5457	25	1	1	15	0.5	6	15	10	1	5	15	2	5	15	50	15	7	15	0	3	15	0			55
2N5458	25	1	1	15	1	7	15	10	2	9	15	1.5	5.5	15	50	15	7	15	0	3	15	0			55
2N5459	25	1	1	15	2	8	15	10	4	16	15	2	6	15	50	15	7	15	0	3	15	0			55
2N5556	30	1	0.1	15	0.2	4	15	1	0.5	2.5	15	1.5	6.5	15	20	15	6	15	0	3	15	0	35	10	50
2N5557	30	1	0.1	15	0.8	5	15	1	2.0	5.0	15	1.5	6.5	15	20	15	6	15	0	3	15	0	35	10	50
2N5558	30	1	0.1	15	1.5	6	15	1	4	10	15	1.5	6.5	15	20	15	6	15	0	3	15	0	35	10	50
J201	40	1	0.1	20	0.3	1.5	20	10	0.2	1.0	20	0.5		20	t1	20	t5	20	0	t2	20	0	t10	1k	52
J202	40	1	0.1	20	0.8	4.0	20	10	0.9	4.5	20	1.0		20	t3.5	20	t5	20	0	t2	20	0	t10	1k	52
J203	40	1	0.1	20	2.0	10.0	20	10	4.0	20	20	1.5		20	t10	20	t5	20	0	t2	20	0	t10	1k	52
J210	25	1	0.1	15	1	3	15	1	2	15	15	4.0	12.0	15	150	15	t5	15	0	t1.5	15	0	t10	1k	90
J211	25	1	0.1	15	2.5	4.5	15	1	7	20	15	7.0	12.0	15	200	15	t5	15	0	t1.5	15	0	t10	1k	90
J212	25	1	0.1	15	4	6	15	1	15	40	15	7.0	12.0	15	200	15	t5	15	0	t1.5	15	0	t10	1k	90
MPF103	25	1	1	15		6	15	1	1	5	15	1	5	15	50	15	7	15	0	3	15	0			55
MPF104	25	1	1	15		7	15	1	2	9	15	1.5	5.5	15	50	15	7	15	0	3	15	0			55
MPF105	25	1	1	15		8	15	1	4	16	15	2	6	15	50	15	7	15	0	3	15	0			55
MPF109	25	10	1	15	0.2	8	15	10	0.5	24	15	0.8	6	15	75	15	7	15	0	3	15	0	115	1000	55

Table 8. N-Channel Selection Guide: General Purpose Amplifiers (Continued)

Transistor Type	BV_{GSS} BV_{GDO} (V) Min	@ I_G (μA)	I_{GSS} I_{DGO} (nA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (nA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ VDS (V)	G_{fs} (mmho) Min	G_{fs} (mmho) Max	@ V_{DS} (V)	G_{oss} (μmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ Freq (Hz)	Process No.
MPF111	20	10	100	10	0.5	10	10	1000	0.5	20	10	0.5		10	200	10									50
MPF112	25	10	100	10	0.5	10	10	1000	1	25	10	1	7.5	10											55
PN3684	50	1	1	30	2	5	20	1	2.5	7.5	20	2	3	20	50	20	4	20	0	1.2	20	0	150	20	52
PN3685	50	1	1	30	1	3.5	20	1	1	3	20	1.5	2.5	20	25	20	4	20	0	1.2	20	0	150	20	52
PN3686	50	1	1	30	0.6	2	20	1	0.4	1.2	20	1	2	20	10	20	4	20	0	1.2	20	0	150	20	52
PN3687	50	1	1	30	0.3	1.2	20	1	0.1	0.5	20	0.5	1.5	20	5	20	4	20	0	1.2	20	0	150	20	52
PN4220	30	10	1	15		4	15	1	0.5	3	15	1	4	15	10	15	6	15	0	2	15	0			55
PN4221	30	10	1	15		6	15	1	2	6	15	2	5	15	20	15	6	15	0	2	15	0			55
PN4222	30	10	1	15		8	15	1	5	15	15	2.5	6	15	40	15	6	15	0	2	15	0			55
PN4302	30	1	1	10		4	20	10	0.5	5	20	1		20	50	20	6	20	0	3	20	0	100	1000	52
PN4303	30	1	1	10		6	20	10	4	10	20	2		20	50	20	6	20	0	3	20	0	100	1000	52
PN4304	30	1	1	10		10	20	10	0.5	15	20	1		20	50	20	6	20	0	3	20	0	125	1000	52
PN5163	25	1	10	15	0.4	8	15	1000	1	40	15	2	9	15	200	15	12	15	0	3	15	0	50	1000	50
TIS58	25	1	4	15	0.5	5	15	20	2.5	8	15	1.3	4	15			6	15	2 mA	3	15	2 mA			50
TIS59	25	1	4	15	1	9	15	20	6	25	15	1.3		15			6	15	2 mA	3	15	2 mA			50

Table 9. N-Channel Selection Guide: General Purpose Dual JFETs

Type No.	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (μA)	$\|V_{GS1-2}\|$ V_{OS} (mV) Max	DRIFT (μV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} μmhos Min	G_{fs} μmhos Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (mmho) Min	G_{fs} (mmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) Max	@ V_{DG} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	e_n (nV/√Hz) Max	@ f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.
2N3921	10	700	5.0	10	250	1500		20					−3.0	1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0			83
2N3922	10	700	5.0	25	250	1500		20					−3.0	1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0			83
2N3934	10	200	5.0	10	100	300		5.0				See 2N3954-6 as an improved replacement																		
2N3935	10	200	5.0	25	100	300		5.0				See 2N3954-6 as an improved replacement																		
2N3954A	20	200	5.0	5.0	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	3.0		10	83
2N3954	20	200	5.0	10	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	3.0		10	83
2N3955A	20	200	5.0	15	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	3.0		10	83
2N3955	20	200	10	25	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	5.0		10	83
2N3956	20	200	15	50	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	5.0	5.0		10	83
2N3957	20	200	20	75	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	10	10		10	83
2N3958	20	200	25	100	50					0.5	4.0	1.0	4.5	0.5	5.0	1.0	3.0	35	100	30	4.0	1.2	50	150	100	15	15		10	83
2N4082	10	200	15	10	100	300		10				See 2N3954-6 as an improved replacement																		
2N4083	10	200	15	25	100	300		10				See 2N3954-6 as an improved replacement																		
2N4084	10	700	15	10	250	1500		20		0.5	4.0		3.0	1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0			83
2N4085	10	700	15	25	250	1500		20					3.0	1.0	10	1.5	7.5	35	1000	30	18	6.0	50	100	1.0k		5.0			83

Type No.	OPERATING CONDITIONS FOR THESE CHARACTERISTICS: OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (μA)	$\|V_{GS1-2}\|$ V_{OS} (mV) Max	DRIFT (μV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} μmhos Min	G_{fs} μmhos Max	G_{oss} (μmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	V_p (V) Min	V_p (V) Max	I_{DSS} (mA) Min	I_{DSS} (mA) Max	G_{fs} (mmho) Min	G_{fs} (mmho) Max	G_{oss} (μmho) Max	I_{GSS} (pA) Max	@ V_{DG} (V)	C_{iss} (pF) Max	C_{rss} (pF) Max	BV (V) Min	$\tilde{e}_n$ (nV/√Hz) Max	@ f (Hz)	I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (μmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.
2N5045	15	200	5.0	67								0.5	4.5	0.5	8.0	1.5	6.0	25	250	30	8.0	4.0	50	200	10		5.0	1.0		83
2N5046	15	200	10	133								0.5	4.5	0.5	8.0	1.5	6.0	25	250	30	8.0	4.0	50	200	10		10	2.0		83
2N5047	15	200	15	200								0.5	4.5	0.5	8.0	1.5	6.0	25	250	30	8.0	4.0	50	200	10		20	3.0		83
2N5196	20	200	5.0	5.0	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	3.0	1.0	5.0	83
2N5197	20	200	5.0	10	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	3.0	1.0	5.0	83
2N5198	20	200	10	20	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	5.0	1.0	5.0	83
2N5199	20	200	15	40	15	700	1500	4.0		0.2	3.8	0.7	4.5	0.7	7.0	1.0	4.0	50	25	30	6.0	2.0	50	20	1.0k	5.0	5.0	1.0	5.0	83
2N5452	20	200	5.0	5.0				1.0		0.2	4.2	1.0	4.5	0.5	5.0	1.0	3.0	3.0	100	30	4.0	1.2	50	20	1.0k	5.0	3.0	0.25		83
2N5453	20	200	10	10				1.0		0.2	4.2	1.0	4.5	0.5	5.0	1.0	3.0	3.0	100	30	4.0	1.2	50	20	1.0k	5.0	3.0	0.25		83
2N5454	20	200	15	25				1.0		0.2	4.2	1.0	4.5	0.5	5.0	1.0	3.0	3.0	100	30	4.0	1.2	50	20	1.0k	5.0	5.0	0.25		83
2N5545	15	200	5.0	10	50							0.5	4.5	0.5	8.0	1.5	6.0	25	100	30	6.0	2.0	50	180	10	5.0	3.0	1.0	5.0	83
2N5546	15	200	10	20	50							0.5	4.5	0.5	8.0	1.5	6.0	25	100	30	6.0	2.0	50	200	10	10	5.0	2.0	5.0	83
2N5547	15	200	15	40	50							0.5	4.5	0.5	8.0	1.5	6.0	25	100	30	6.0	2.0	50			10	10	3.0	5.0	83
J410	20	200	10	10	250	600	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	250	20	4.5	1.2	40	50	100					98
J411	20	200	25	25	250	600	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	250	20	4.5	1.2	40	50	100					98
J412	20	200	40	80	250	600	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	250	20	4.5	1.2	40	50	100					98
NPD8301	20	200	5	10	100	700	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	100	20	4.5	1.2	40	50	100					83
NPD8302	20	200	10	15	100	700	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	100	20	4.5	1.2	40	50	100					83
NPD8303	20	200	15	25	100	700	1200	5.0		0.3	4.0	0.5	3.5	0.5	6	1	4	20	100	20	4.5	1.2	40	50	100					83
U231	20	200	5.0	10	50	600		10		0.3	4.0	See 2N3954 as an improved replacement																		83
U232	20	200	10	25	50	600		10		0.3	4.0	See 2N3955 as an improved replacement																		83
U233	20	200	15	50	50	600		10		0.3	4.0	See 2N3956 as an improved replacement																		83
U234	20	200	20	75	50	600		10		0.3	4.0	See 2N3957 as an improved replacement																		83
U235	20	200	25	100	50	600		10		0.3	4.0	See 2N3958 as an improved replacement																		83

Table 10. N-Channel Selection Guide: Low Frequency – Low Noise Dual JFETs

Type No.	OPERATING CONDITIONS FOR THESE CHARACTERISTICS											V_p (V)		I_{DSS} (mA)		G_{fs} (µmho)		G_{oss} (µmho)	I_{GSS} (pA) @ V_{DG}		C_{iss} (pF)	C_{rss} (pF)	BV (V)	e_n (nV/√Hz) @ f		I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (µmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.
	OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (µA)	$\|V_{GS1-2}\|$ V_{OS} (mV) Max	DRIFT (µV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} µmhos Min	G_{fs} µmhos Max	G_{oss} (µmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	Min	Max	Min	Max	Min	Max	Max	Max	(V)	Max	Max	Min	Max	(Hz)					
2N5515	20	200	5.0	5.0	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	30	10	5.0	3.0	0.1	10	95
2N5516	20	200	5.0	10	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	5.0	3.0	0.1	10	95
2N5517	20	200	10	20	100	500	1000	1.0	90	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	5.0	5.0	0.1	10	95
2N5518	20	200	15	40	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	5.0	5.0	0.1	10	95
2N5519	20	200	15	80	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	10	10	0.1	10	95
2N5520	20	200	5.0	5.0	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40	15	10	5.0	3.0	0.1	10	95
2N5521	20	200	5.0	10	100	500	1000	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	5.0	3.0	0.1	10	95
2N5522	20	200	10	20	100	500	1000	1.0	90	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	5.0	5.0	0.1	10	95
2N5523	20	200	15	40	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	5.0	5.0	0.1	10	95
2N5524	20	200	15	80	100	500	1000	1.0		0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	250	30	+25	+5.0	40		10	10	10	0.1	10	95
2N6483	20	200	5.0	5.0	100	500	1500	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	200	30	20	3.5	50	10	10	5.0	3.0	0.1	10	95
2N6484	20	200	10	10	100	500	1500	1.0	100	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	200	30	20	3.5	50		10	5.0	3.0	0.1	10	95
2N6485	20	200	15	25	100	500	1500	1.0	90	0.2	3.8	0.7	4.0	0.5	7.5	1.0	4.0	10	200	30	20	3.5	50		10	5.0	5.0	0.1	10	95

Table 11. N-Channel Selection Guide: Wide Band – Low Noise Dual JFETs

Type No.	OPERATING CONDITIONS FOR THESE CHARACTERISTICS											V_p (V)		I_{DSS} (mA)		G_{fs} (µmho)		G_{oss} (µmho)	I_{GSS} (pA) @ V_{DG}		C_{iss} (pF)	C_{rss} (pF)	BV (V)	e_n (nV/√Hz) @ f		I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (µmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.
	OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (µA)	$\|V_{GS1-2}\|$ V_{OS} (mV) Max	DRIFT (µV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} µmhos Min	G_{fs} µmhos Max	G_{oss} (µmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	Min	Max	Min	Max	Min	Max	Max	Max	(V)	Max	Max	Min	Max	(Hz)					
2N5564	15	2000	5.0	10		7500		45				0.5	3.0	5.0	30				100	20	12	3.0	40	50	10	5.0	5.0			96
2N5565	15	2000	10	25		7500		45				0.5	3.0	5.0	30				100	20	12	3.0	40	50	10	5.0	10			96
2N5566	15	2000	20	50		7500		45				0.5	3.0	5.0	30				100	20	12	3.0	40	50	10	5.0	10			96
2N5911	10	5000	10	20	100	5000	10,000	100		0.3	4.0	1.0	5.0	7.0	40				100	15	5.0	1.2	25	20	10k	5.0	5.0	20	20	93
2N5912	10	5000	15	40	100	5000	10,000	100		0.3	4.0	1.0	5.0	7.0	40				100	15	5.0	1.2	25	20	10k	5.0	5.0	20	20	93
NPD5564	15	2000	5.0	10		7500		45				0.5	3.0	5.0	30				100	20	12	3.0	40	50	10	5.0	5.0			96
NPD5565	15	2000	10	25		7500		45				0.5	3.0	5.0	30				100	20	12	3.0	40	50	10	5.0	10			96
NPD5566	15	2000	20	50		7500		45				0.5	3.0	5.0	30				100	20	12	3.0	40	50	10	5.0	10			96
U257	10	5000	100			5000	10,000	150				1.0	5.0	5.0	40				100	15	5.0	1.2	25	30	10k	15	15	20		93
U430	10	10,000				10,000	20,000	150				1.0	4.0	12	30				150	15			25	10	100	10	10			92
U431	10	10,000				10,000	20,000	150				2.0	6.0	24	60				150	15			25	10	100	10	10			

Table 12. N-Channel Selection Guide: Low Leakage – High CMRR Wide Band Dual JFETs

Type No.	OPERATING CONDITIONS FOR THESE CHARACTERISTICS											V_p (V)		I_{DSS} (mA)		G_{fs} (µmho)		G_{oss} (µmho)	I_{GSS} (pA) @ V_{DG}		C_{iss} (pF)	C_{rss} (pF)	BV (V)	e_n (nV/√Hz) @ f		I_{DSS} Match %	G_{fs} Match %	G_{oss1-2} (µmho)	I_{G1}-I_{G2} 125°C (nA)	Process No.
	OP. CHAR. V_{DG} (V)	OP. CHAR. I_D (µA)	$\|V_{GS1-2}\|$ V_{OS} (mV) Max	DRIFT (µV/°C) ΔV_{GS} Max	I_G (pA) Max	G_{fs} µmhos Min	G_{fs} µmhos Max	G_{oss} (µmho) Max	CMRR (dB) Min	V_{gs} (V) Min	V_{gs} (V) Max	Min	Max	Min	Max	Min	Max	Max	Max	(V)	Max	Max	Min	Max	(Hz)					
NDF9401	20	200	5.0	5.0	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1	1.0	94
NDF9402	20	200	5.0	10	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1		94
NDF9403	20	200	10	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94
NDF9404	20	200	15	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94
NDF9405	20	200	25	25	5.0¶	950	2000	0.1	100	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	10	10	0.1	1.0	94
NDF9406	20	200	5.0	5.0	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1	1.0	94
NDF9407	20	200	5.0	10	5.0¶	950	2000	0.1	120	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	3.0	0.1	1.0	94
NDF9408	20	200	10	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94
NDF9409	20	200	15	10	5.0¶	950	2000	0.1	110	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	5.0	5.0	0.1	1.0	94
NDF9410	20	200	25	25	5.0¶	950	2000	0.1	100	0.1	4.0	0.5	4.0	0.5	10				10	30	5.0	0.02	50	30	10	10	10	0.1	1.0	94

¶ V_{DG} = 35V

Table 13. N-Channel Selection Guide: Ultra Low Leakage Dual JFETs

Type No.	OPERATING CONDITIONS FOR THESE CHARACTERISTICS									V_p (V)		I_{DSS} (mA)		G_{fs} (mmho)		G_{oss} (µmho)	I_{GSS} (pA) @ V_{GS}		C_{iss} (pF)	C_{rss} (pF)	BV_{GSS} (V)	I_{G1}-I_{G2} @ 125°C (nA)	Process No.
	Oper. Cond. V_{DG} (V)	Oper. Cond. I_D (µA)	V_{GS1-2} V_{OS} (mV) Max	ΔV_{GS} DRIFT (µV/°C) Max	I_G (pA) Max	G_{fs} (mMho) Min	G_{oss} (µMho) Max	V_{GS} (V) Min	V_{GS} (V) Max	Min	Max	Min	Max	Min	Max	Max	Max	(V)	Max	Max	Min	Max	
2N5902	10	30	5	5	3	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	5	20	3	1.5	40	2	84
2N5903	10	30	5	10	3	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	5	20	3	1.5	40	2	84
2N5904	10	30	10	20	3	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	5	20	3	1.5	40	2	84
2N5905	10	30	15	40	3	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	5	20	3	1.5	40	2	84
2N5906	10	30	5	5	1	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	2	20	3	1.5	40	0.2	84
2N5907	10	30	5	10	1	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	2	20	3	1.5	40	0.2	84
2N5908	10	30	10	20	1	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	2	20	3	1.5	40	0.2	84
2N5909	10	30	15	40	1	50µ	1		4	0.6	4.5	30µ	0.5	70µ	0.25	5	2	20	3	1.5	40	0.2	84

Table 14. P-Channel Selection Guide: Switches

Transistor Type	BV_{GSS} BV_{GDO} (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (nA) Max	@ V_{DG} (V)	$I_{D(off)}$ (nA) Max	@ V_{DS} (V)	V_{GS} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (µA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	r_{ds} (Ω) Max	@ I_D (mA)	C_{iss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	@ V_{DS} (V)	V_{GS} (V)	t_{on} (ns) Max	t_{off} (ns) Max	Process No.
2N3382	30	1	15	30	2	−5	6	1	5	−5	1	3	30	10	300										88
2N3384	30	1	15	30	2	−5	6	4	5	−5	1	15	30	10	180										88
2N3386	30	1	15	30	2.5	−5	10	4	9.5	−5	1	15	50	10	150										88
2N3993	25	1	1.2*	15	1.2	−10	10	4	9.5	−10	1	10		10	150		16	−10	0	4.5	0	10			88
2N3993A	25	1	1.2*	15	1.2	−10	10	4	9.5	−10	1	10		10	150		12	−10	0	3	0	10			88
2N3994	25	1	1.2*	15	1.2	−10	6	1	5.5	−10	1	2		10	300		16	−10	0	4.5	0	10			88
2N3994A	25	1	1.2*	15	1.2	−10	6	1	5.5	−10	1	2		10	300		12	−10	0	3	0	10			88
2N5018	30	1	2	15	10	−15	12		10	−15	1	10		20	75		45	−15	0	10	0	12	35	65	88
2N5019	30	1	2	15	10	−15	7		5	−15	1	5		20	150		45	−15	0	10	0	7	90	125	88
•2N5114	30	1	0.5	20	0.5	−15	12	5	10	−15	.001	30	90	18	75	1	25	−15	0	7	0	12	16	21	88
•2N5115	30	1	0.5	20	0.5	−15	7	3	6	−15	.001	16	60	15	100	1	25	−15	0	7	0	7	30	38	88
•2N5116	30	1	0.5	20	0.5	−15	5	1	4	−15	.001	5	25	15	150	1	25	−15	0	7	0	5	42	60	88
J174	30	1	1	20	1	−15	10	5	10	−15	.01	20	100	15	85	1	11	0	10	5.5	0	10	2	5	88
J175	30	1	1	20	1	−15	10	3	6	−15	.01	7	60	15	125	.5	11	0	10	5.5	0	10	5	10	88
J176	30	1	1	20	1	−15	10	1	4	−15	.01	2	25	15	250	.25	11	0	10	5.5	0	10	15	15	88
J177	30	1	1	20	1	−15	10	.8	2.25	−15	.01	1.5	20	15	300	.1	11	0	10	5.5	0	10	20	20	88
P1086E	30	1	2	20	10	−15	10		10	−15	.01	10		15	75	1	45	−15	0	10	15	0	35	50	88
P1087E	30	1	2	20	10	−15	5		5	−15	.01	5		15	150		45	−15	0	10	15	0	40	75	88
U304	30	1	0.5	20	0.5	−15	12	5	10	15	1	30	90	15	85		27	−15	0	7	0	12	35	35	88
U305	30	1	0.5	20			7	3	4	15	1	15	60	15	110		27	−15	0	7	0	7	50	45	88
U306	30	1	0.5	20			5	1	4	15	1	5	25	15	175		27	−15	0	7	0	5	60	80	88

• Note. JAN qualified per applicable MIL-S-19500 specification

Table 15. P-Channel Selection Guide: Amplifiers

Transistor Type	BV_{GSS} BV_{GDO} (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (nA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (µA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	G_{fs} (mmho) Min	G_{fs} (mmho) Max	@ V_{DS} (V)	G_{oss} (µmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ Freq (Hz)	Process No.
•2N2608	30	1	10	30	1	4	−5	1	0.9	4.5	5	1		5			17	−5	1				125	1000	89
2N2609	30	1	30	30	1	4	−5	1	2	10	5	2.5		5			30	−5	1				125	1000	88
2N3329	20	10	10	10		5	−15	10	1	3	10	1	2	10/1mA	20	10	20	−10	1				125	1000	89
2N3330	20	10	10	10		6	−15	10	2	6	10	1.5	3	10/2mA	40	10	20	−10	1				125	1000	89
2N3331	20	10	10	10		8	−15	10	5	15	10	2	4	10/5mA	100	10	20	−10	1				155	1000	89
2N3332	20	10	10	10		6	−15	10	1	6	10	1	2.2	10/1mA	20	10	20	−10	1				65	1000	89
2N4381	25	1	1	15	1	5	−15	1	3	12	15	2	6	15	75	15	20	−15	0	5	−15	0	20	1000	89
2N4382	25	1	1	15	2.5	9	−15	1	10	30	15	4	8	15	100	15	20	−15	0	5	−15	0	20	1000	88

• Note. JAN qualified per applicable MIL-S-19500 specification

Transistor Type	BV_{GSS} BV_{GDO} (V) Min	@ I_G (µA)	I_{GSS} I_{DGO} (nA) Max	@ V_{DG} (V)	V_p (V) Min	V_p (V) Max	@ V_{DS} (V)	I_D (µA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	G_{fs} (mmho) Min	G_{fs} (mmho) Max	@ V_{DS} (V)	G_{oss} (µmho) Max	@ V_{DS} (V)	C_{iss} (pF) Max	V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Max	V_{DS} (V)	V_{GS} (V)	e_n $\left(\frac{NV}{\sqrt{Hz}}\right)$ Max	@ Freq (Hz)	Process No.
2N5020	25	1	1	15	0.3	1.5	−15	1	0.3	1.2	15	1	3.5	15	20	15	25	−15	0	7	−15	0	30	1000	89
2N5021	25	1	1	15	0.5	2.5	−15	1	1	3.5	15	1.5	6	15	20	15	25	−15	0	7	−15	0	30	1000	89
2N5460	40	10	5	20	0.75	6	−15	1	1	5	15	1	4	15	50	15	7	−15	0	2	−15	0	115	100	89
2N5461	40	10	5	20	1	7.5	−15	1	2	9	15	1.5	5	15	50	15	7	−15	0	2	−15	0	115	100	89
2N5462	40	10	5	20	1.8	9	−15	1	4	16	15	2	6	15	50	15	7	−15	0	2	−15	0	115	100	89
J270	30	1	0.2	20	0.5	2.0	15	.001	2	15	15	6.0	15.0	15	200	15	t20	15	0	t5	15	0	t10	1k	88
J271	30	1	0.2	20	1.5	4.5	15	.001	6	50	15	8.0	18.0		500	15	t20	15	0	t5	15	0	t10	1k	88
PN4342	25	10	10	15		5.5	−10	1	4	12	10	2	6	10	75	10	20	−10	0	5	−10	0	80	100	89
PN4343	25	10	10	15		10	−10	1	10	30	10	4	8	10	100	10	20	−10	0	5	−10	0	80	100	88
PN4360	20	10	10	15	0.7	10	−10	1	3	30	10	2	8	10	100	10	20	−10	0	5	−10	0	190	100	89
PN5033	20	10	10	15	0.3	2.5	−10	1	0.3	3.5	10	1	5	10	20	10	25	−10	0	7	−10	0	100	1000	89
U300	40	1	0.1	20	5	10	−15	.001	30	90		8	12	15			20	−15	15 mA	5.5	−15	15 mA	40	1000	88
U301	40	1	0.1	20	2.5	60	−15	.001	15	60		7	11	15			20	−15	7 mA	5.5	−15	5.5 mA	40	1000	88

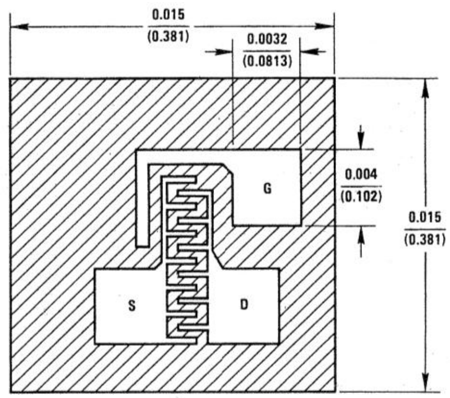
Table 16. Pro-Electron JFETs: Amplifiers

Type No.	BV_{GSS} / BV_{GDO} (V) Min	@ I_G (µA)	I_{GSS} / I_{DGD} (nA) Max	@ V_{GD} (V)	V_P (V) Min	V_P (V) Max	@ V_{DS} (V)	I_D (nA)	V_{GS} (V) Min	V_{GS} (V) Max	@ V_{DS} (V)	I_D (µA)	I_{DSS} (mA) Min	I_{DSS} (mA) Max	@ V_{DS} (V)	$R_e(Y_{FS})$ (mmho) Min	$R_e(Y_{FS})$ (mmho) Max	@ f (MHz)	C_{iss} (pF) Typ	@ V_{DS} (V)	V_{GS} (V)	C_{rss} (pF) Typ	@ V_{DS} (V)	V_{GS} (V)	NF (dB) @ R_G = 1k, e_n* Max	NF Typ	f (Hz)* (MHz)	Process No.
BF244A	30	1	5	20	.5	8	15	10	.4	2.2	15	200	2	6.5	15	3	6.5	.001	4	20	−1	1.1	20	−1		1.5	100	50
BF244B	30	1	5	20	.5	8	15	10	1.6	3.8	15	200	6	15	15	3	6.5	.001	4	20	−1	1.1	20	−1		1.5	100	50
BF244C	30	1	5	20	.5	8	15	10	3.2	7.5	15	200	12	25	15	3	6.5	.001	4	20	−1	1.1	20	−1		1.5	100	50
BF245A	30	1	5	20	.5	8	15	10	.4	2.2	15	200	2	6.5	15	3	6.5	.001	4	20	−1	1.1	20	−1				50
BF245B	30	1	5	20	.5	8	15	10	1.6	3.8	15	200	6	15	15	3	6.5	.001	4	20	−1	1.1	20	−1				50
BF245C	30	1	5	20	.5	8	15	10	3.2	7.5	15	200	12	25	15	3	6.5	.001	4	20	−1	1.1	20	−1				50
BF246A	25	1	5	15	.6	14.5	15	10	1.5	4.0	15	200	30	80	15	8		.001	11	15	0	3.5	15	0				51
BF246B	25	1	5	15	.6	14.5	15	10	3.0	7.0	15	200	60	140	15	8		.001	11	15	0	3.5	15	0				51
BF246C	25	1	5	15	.6	14.5	15	10	5.5	12	15	200	110	250	15	8		.001	11	15	0	3.5	15	0				51
BF247A	25	1	5	15	.6	14.5	15	10	1.5	4.0	15	200	30	80	15	8		.001	11	15	0	3.5	15	0				51
BF247B	25	1	5	15	.6	14.5	15	10	3.0	7.0	15	200	60	140	15	8		.001	11	15	0	3.5	15	0				51
BF247C	25	1	5	15	.6	14.5	15	10	5.5	12	15	200	110	250	15	8		.001	11	15	0	3.5	15	0				51
BF256A	30	1	5	20					.5	7.5	15	200	3	7	15	4.5		.001				.7	20	−1		7.5	800	50
BF256B	30	1	5	20					.5	7.5	15	200	6	13	15	4.5		.001				.7	20	−1		7.5	800	50
BF256C	30	1	5	20					.5	7.5	15	200	11	18	15	4.5		.001				.7	20	−1		7.5	800	50
BC264A	30	1	10	20	.5		15	10	.2	1.2	15	1000	2	4.5	15	2.5		.001	4.0	15	−1	1.2	15	−1		40*	10*	50
BC264B	30	1	10	20	.5		15	10	.4	1.4	15	1500	3.5	6.5	15	3.0		.001	4.0	15	−1	1.2	15	−1		40*	10*	50
BC264C	30	1	10	20	.5		15	10	.5	1.5	15	2500	5.0	8.0	15	3.5		.001	4.0	15	−1	1.2	15	−1		40*	10*	50
BC264D	30	1	10	20	.5		15	10	.6	1.6	15	3500	7.0	12.0	15	4.0		.001	4.0	15	−1	1.2	15	−1		40*	10*	50

JFET Process Characteristics

This section contains complete design curves for all of Fairchild Semiconductor's discrete JFET processes. Temperature and $V_{GS(off)}$ distribution data is provided to facilitate worst-case design. In addition a complete list of all device types supplied from this process is included to aid in cross reference searches and the selection of preferred device types. The curves in this section should be considered typical of the process supplied by Fairchild Semi-conductor. Every effort is made to keep the process in tolerance with the published graphs, but the exact distribution of any specific lot of material is not guaranteed.

Process 50 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

Process 50 is designed primarily for RF amplifier and mixer applications. It will operate up to 450 MHz with low noise figure and good power gain. These devices offer outstanding performance at VHF aircraft and communications frequencies. Their major advantage is low crossmodulation and intermodulation, low noise figure and good power gain. The device is also a good choice for analog switching where low capacitance is very important.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−25	−40		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0V	1.0	10	20	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	3.0	5.5	7.0	mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = 15V, I_D = 200 μA		1.1		mmhos
Reverse Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−5.0	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	100	175	500	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	−0.7	−3.5	−6.0	V
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 1 mA, f = 1 kHz		10		μmhos
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0		0.7	0.9	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0		3.5	4.0	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 1 mA, f = 100 Hz		8.0		$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 15V, I_D = 5 mA, R_G = 1 kΩ, f = 400 MHz		2.2	4.0	dB
Power Gain	G_{PS}	V_{DG} = 15V, I_D = 5 mA, f = 400 MHz		12		dB

Examples of process 50 part numbers are as follows. *Denotes preferred parts.

2N3823
2N3966
2N4223
2N4224
2N4416
*2N4416A
2N5078
2N5103
2N5104
2N5105
2N5556
2N5557
2N5558

*2N5484
*2N5485
*2N5486
2N5555
2N5668
2N5669
2N5670
*J304
*J305
PN4223
PN4224
*PN4416

PN5163
MPF102
MPF106
MPF107
MPF110
MPF111
2N3819
2N5248
BF244A
BF244B
BF244C
TIS58
TIS59

2N5949
2N5950
2N5951
2N5952
2N5953
BC264A
BC264B

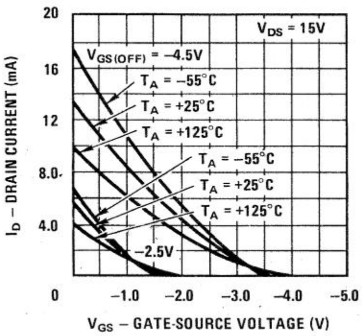
BC264C
BC264D
BF245A
BF245B
BF245C
BF256A
BF256B
BF256C

QUALIFIED PER MIL-S-19500

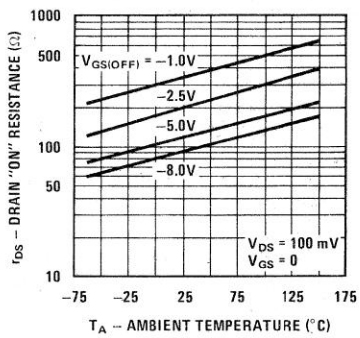
2N3823JAN, JANTX, JANTXV
2N4416AJAN, JANTX, JANTXV

Process 50

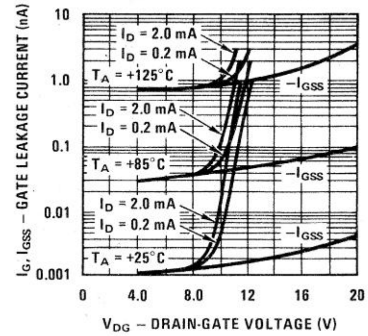
Transfer Characteristics



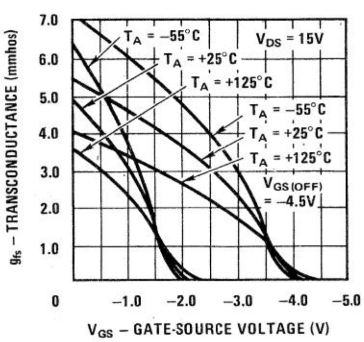
Channel Resistance vs Temperature



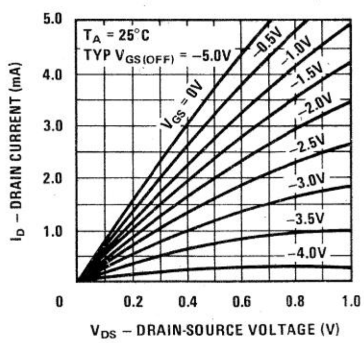
Leakage Current vs Voltage



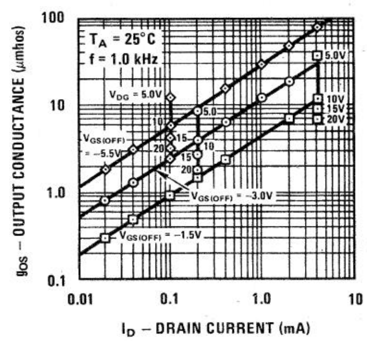
Transconductance Characteristics



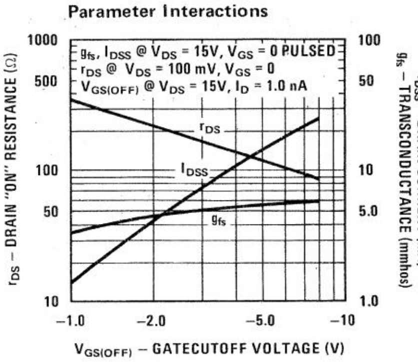
Common Drain-Source Characteristics



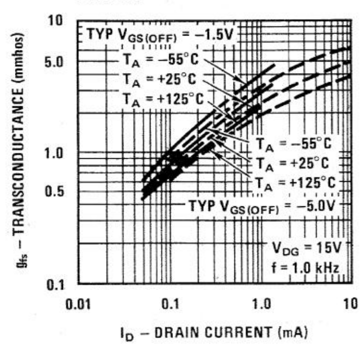
Output Conductance vs Drain Current



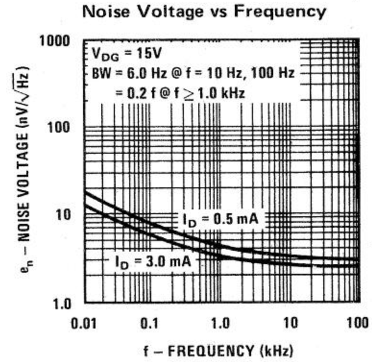
Parameter Interactions



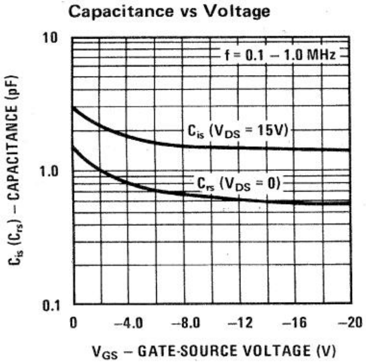
Transconductance vs Drain Current



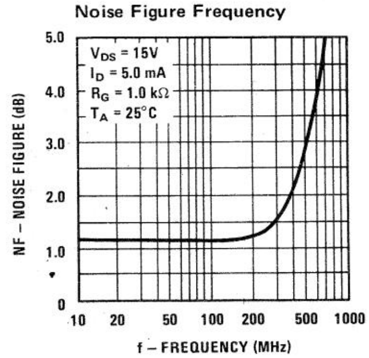
Noise Voltage vs Frequency



Capacitance vs Voltage



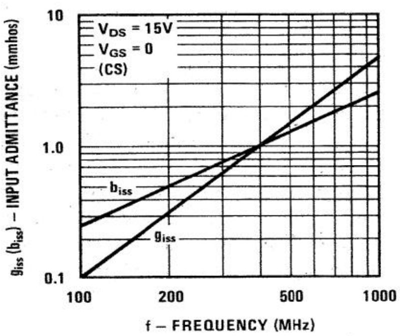
Noise Figure Frequency



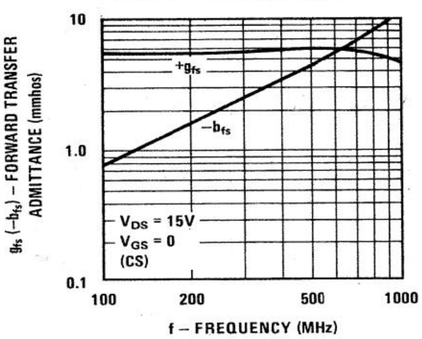
Process 50

COMMON SOURCE

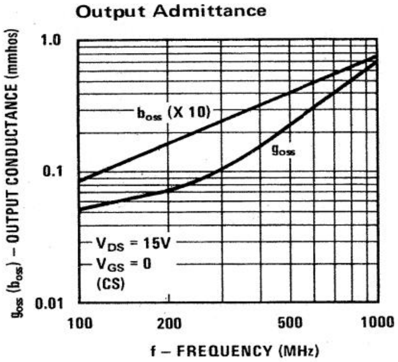
Input Admittance



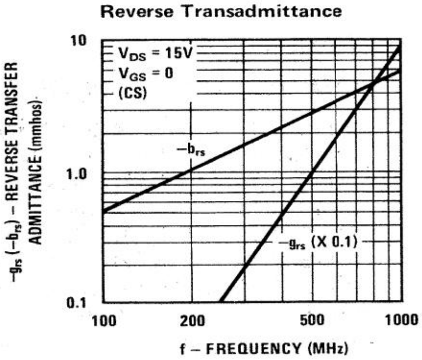
Forward Transadmittance



Output Admittance

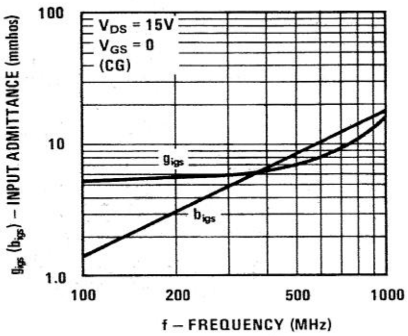


Reverse Transadmittance

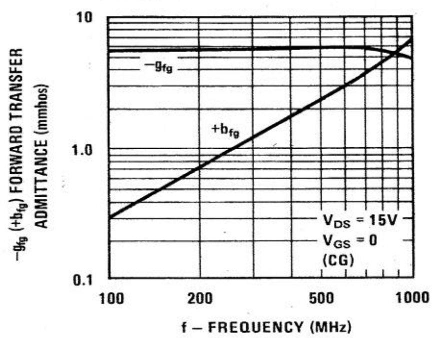


COMMON GATE

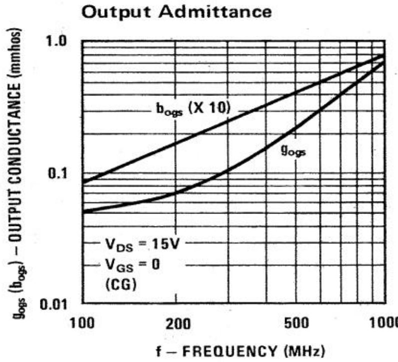
Input Admittance



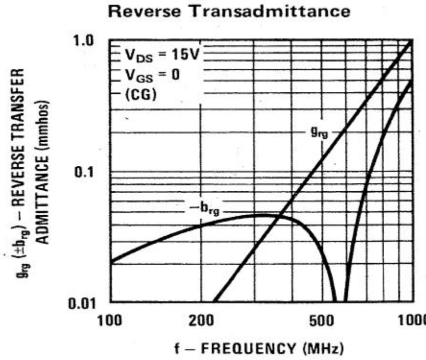
Forward Transadmittance



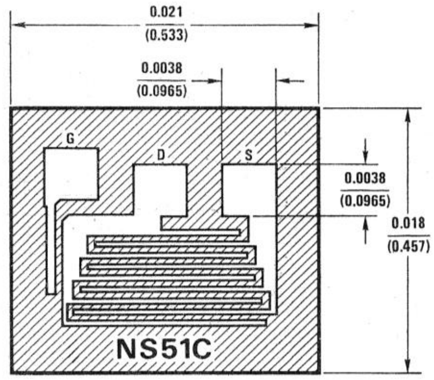
Output Admittance



Reverse Transadmittance



Process 51 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

Process 51 is designed primarily for electronic switching applications such as low ON resistance analog switching. It features excellent C_{iss} $R_{DS(ON)}$ time constant. The inherent zero offset voltage and low leakage current make these devices excellent for chopper stabilized amplifiers, sample and hold circuits, and reset switches. Low feed-through capacitance also allows them to handle video signals to 100 MHz.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−30	−50		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0 Pulse Test	5.0	65	170	mA
Reverse Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−15	−200	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	20	35	100	Ω
Forward Trans-conductance	g_{fs}	V_{DG} = 15V, I_D = 2 mA		8.5		mmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 20V, I_D = 1 nA	−0.5	−4.5	−9.0	V
Drain "OFF" Current	$I_{D(OFF)}$	V_{DS} = 20V, V_{GS} = −10V		15	200	pA
Feedback Capacitance	C_{rss}	V_{DG} = 15V, I_D = 5 mA, f = 1 MHz		3.5	4.0	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, I_D = 5 mA, f = 1 MHz		12	16	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 1 mA, f = 100 Hz		6.0		$nV/\sqrt{Hz}$
Turn-On Time	t_{on}	V_{DD} = 10V, I_D = 6.6 mA		12	20	ns
Turn-Off Time	t_{off}	V_{DD} = 10V, I_D = 6.6 mA		40	80	ns

Examples of process 51 part numbers are as follows. *Denotes preferred parts.

2N3970
2N3971
2N3972
*2N4091
*2N4092
*2N4093
*2N4391
*2N4392
*2N4393
*2N4856
2N4856A
*2N4857
2N4857A
*2N4858
2N4858A
2N4859
2N4859A
2N4860
2N4860A

2N4861
2N4861A

*NF5101
*NF5102
*NF5103
*2N5638
*2N5639
*2N5640
2N5653
2N5654
*J111
*J112
*J113
*PF5101
*PF5102
*PF5103
*PN4091

*PN4092
*PN4093
*PN4391
*PN4392
*PN4393
*PN4856
*PN4857
*PN4858
*PN4859
*PN4860
*PN4861
U1897E
U1898E
U1899E

BF246A
BF246B
BF246C

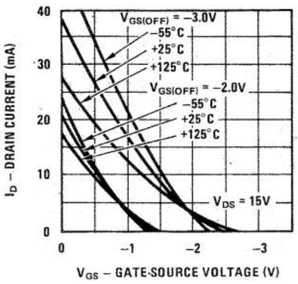
BF247A
BF247B
BF247C
TIS73
TIS74
TIS75

QUALIFIED PER MIL-S-19500

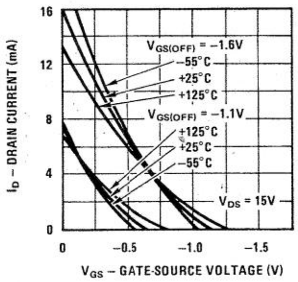
2N4091 JAN, JANTX, JANTXV
2N4092 JAN, JANTX, JANTXV
2N4093 JAN, JANTX, JANTXV
2N4856 JAN, JANTX, JANTXV
2N4857 JAN, JANTX JANTXV
2N4858 JAN, JANTX, JANTXV
2N4859 JAN, JANTX, JANTXV
2N4860 JAN, JANTX, JANTXV
2N4861 JAN, JANTX, JANTXV

Process 51

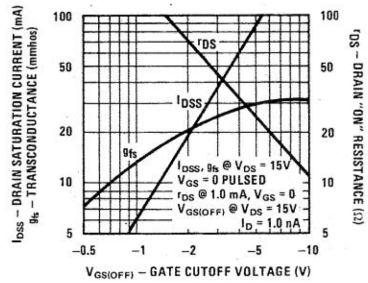
Transfer Characteristics



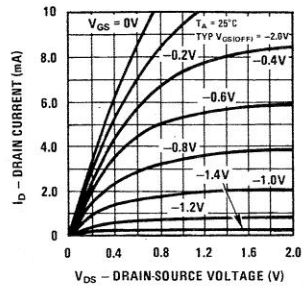
Transfer Characteristics



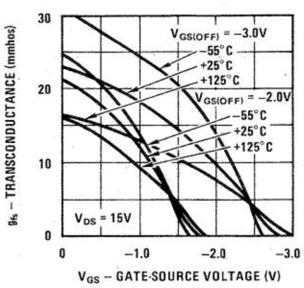
Parameter Interactions



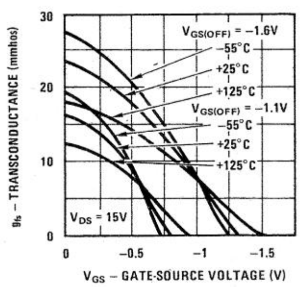
Common Drain-Source Characteristics



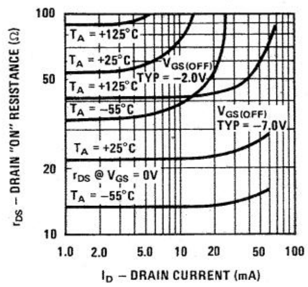
Transfer Characteristics



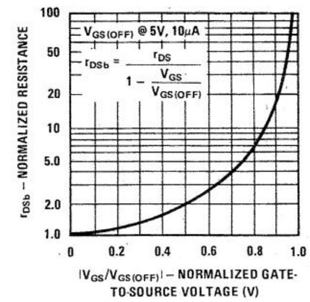
Transfer Characteristics



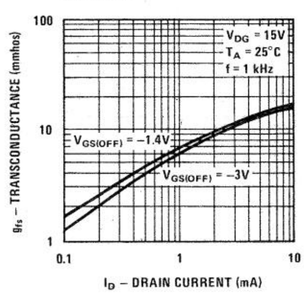
Resistance vs Drain Current



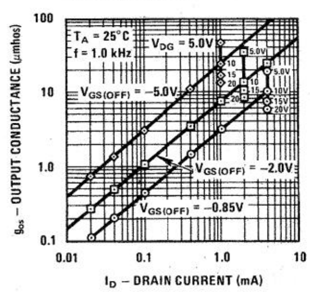
Normalized Drain Resistance vs Bias Voltage



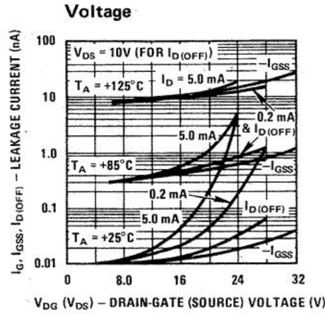
Transconductance vs Drain Current



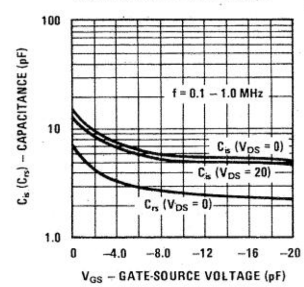
Output Conductance vs Drain Current



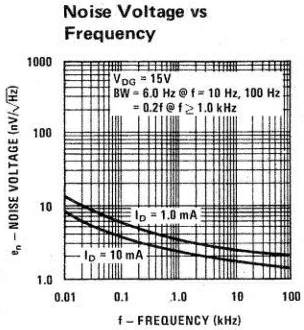
Leakage Current vs Voltage



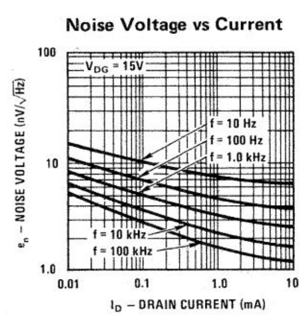
Capacitance vs Voltage



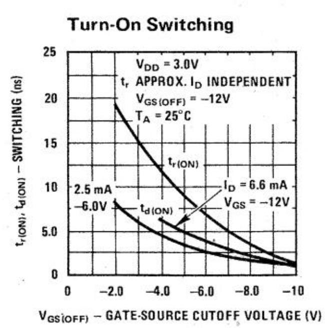
Noise Voltage vs Frequency



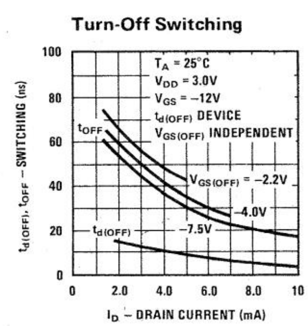
Noise Voltage vs Current



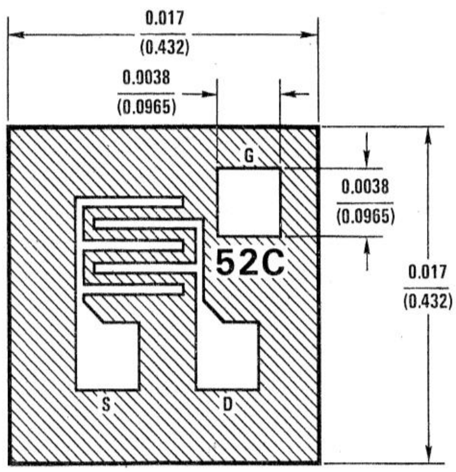
Turn-On Switching



Turn-Off Switching



Process 52 N-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

Process 52 is designed primarily for low level audio and general purpose applications. These devices provide excellent performance as input stages for piezo electric transducers or other high impedance signal sources. Their high output impedance and high voltage breakdown lend them to high gain audio and video amplifier applications. Source and drain are interchangeable.

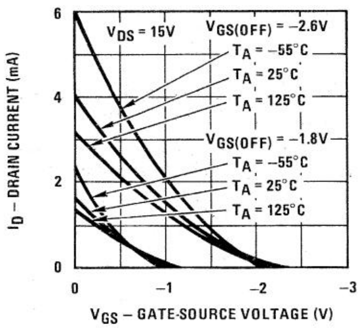
CHARACTERISTIC	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Drain Saturation Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	0.2	1.5	12	mA
Forward Transconductance	g_{fs}	V_{DS} = 20V, V_{GS} = 0V	1.0	2.5	5.0	mmho
Forward Transconductance	g_{fs}	V_{DS} = 20V, I_D = 200 μA		700		μmho
Reverse Gate Leakage Current	I_{GSS}	V_{GS} = −30V, V_{DS} = 0V		−10		pA
Drain ON Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0V	250	400	2000	Ω
Gate Cutoff Voltage	$V_{GS(OFF)}$, V_P	V_{DS} = 15V, I_D = 1 nA	−0.3	1.0	−8.0	V
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 200 μA		2.0		μmho
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0V, f = 1 MHz		1.3	1.8	pF
Input Capacitance	C_{iss}	V_{DG} = 15V, V_{GS} = 0V, f = 1 MHz		5	6	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 200 μA, f = 100 Hz		10		nV/√Hz

Examples of process 52 part numbers are as follows. *Denotes preferred parts.

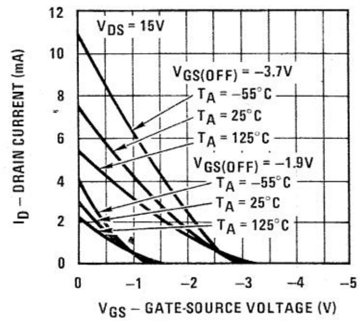
2N3069	*2N3684	*J201
2N3070	*2N3685	*J202
2N3071	*2N3686	*J203
2N3368	*2N3687	*PN3684
2N3369	2N3967	*PN3685
2N3370	2N3967A	*PN3686
2N3458	2N3968	*PN3687
2N3459	2N3968A	*PN4302
2N3460	2N3969	*PN4303
*2N4338	2N3969A	*PN4304
*2N4339		
*2N4340		
*2N4341		

Process 52

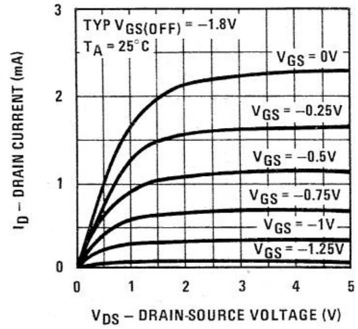
Transfer Characteristics



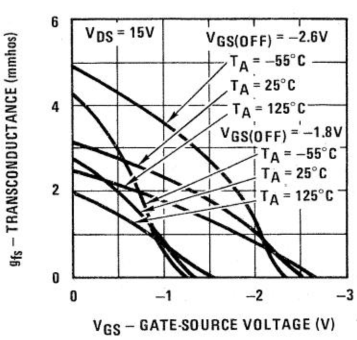
Transfer Characteristics



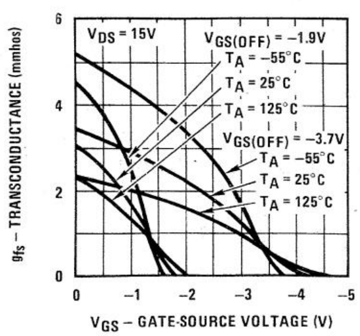
Common Drain-Source Characteristics



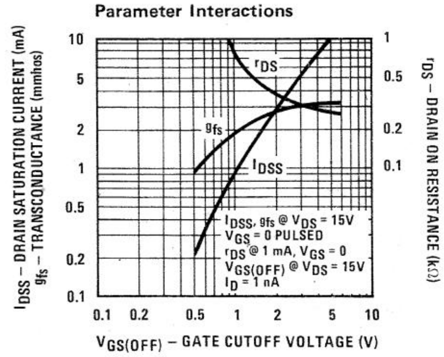
Transfer Characteristics



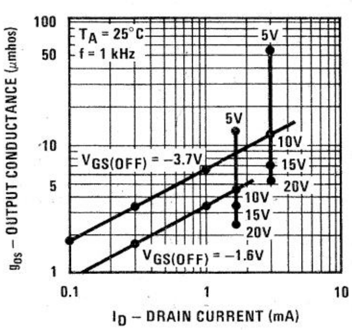
Transfer Characteristics



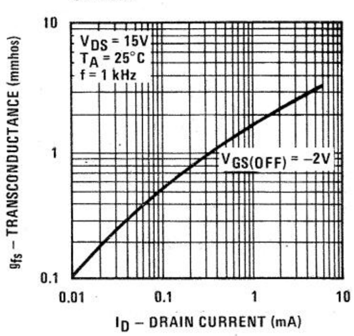
Parameter Interactions



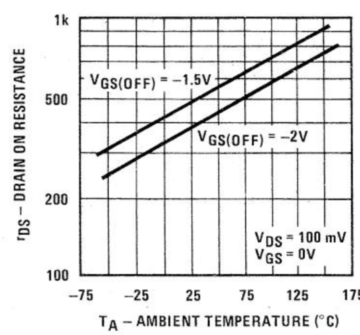
Output Conductance vs Drain Current



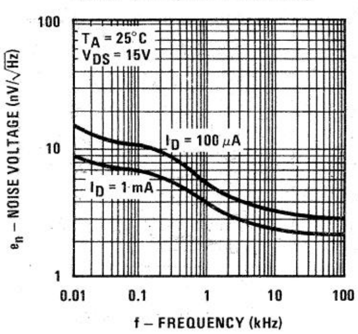
Transconductance vs Drain Current



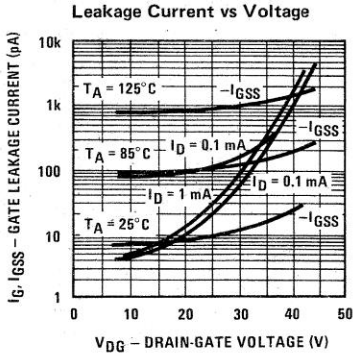
Channel Resistance vs Temperature



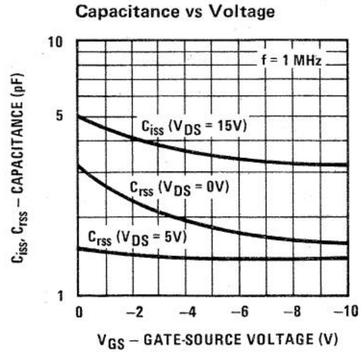
Noise Voltage vs Frequency



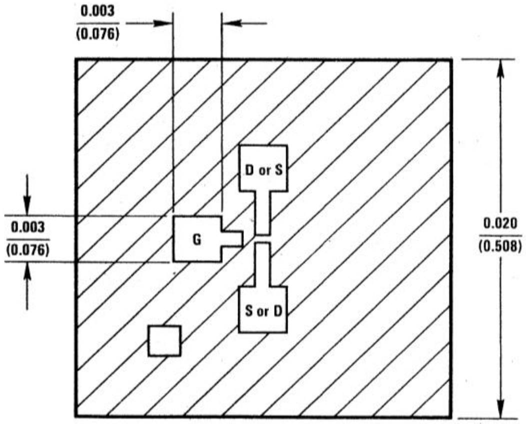
Leakage Current vs Voltage



Capacitance vs Voltage



Process 53 N-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 53 is designed primarily for low current DC and audio applications. These devices provide excellent performance as input stages for sub picoamp instrumentation or any high impedance signal sources.

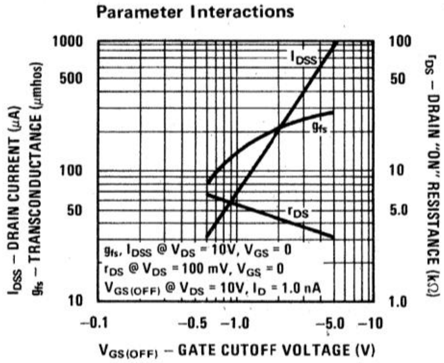
CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−60		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0	0.02	0.25	1.0	mA
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0	80	250	350	μmho
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 50 μA		120		μmho
Reverse Gate Leakage	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−0.3	−10	pA
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−0.5	−2.2	−6.0	V
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0, f = 1 MHz		0.85	1.0	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		2.0	2.5	pF
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 50 μA		0.9	5.0	μmhos
Noise Voltage	e_n	V_{DG} = 10V, I_D = 50 μA, f = 100 Hz		45	150	nV/√Hz

Examples of process 53 part numbers are as follows.

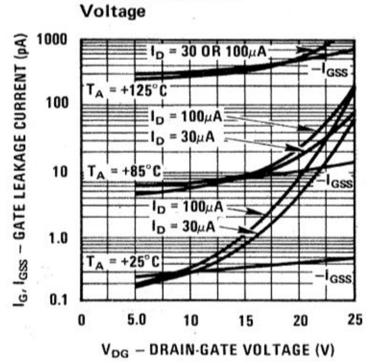
*Denotes preferred parts.

2N4117
*2N4117A
2N4118
*2N4118A
2N4119
*2N4119A

Parameter Interactions

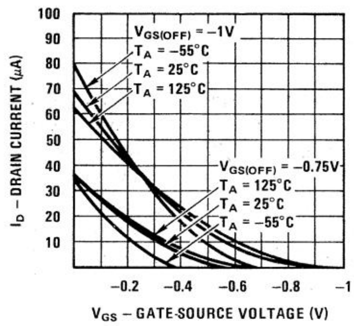


Leakage Current vs Voltage

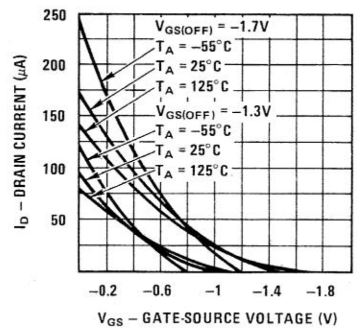


Process 53

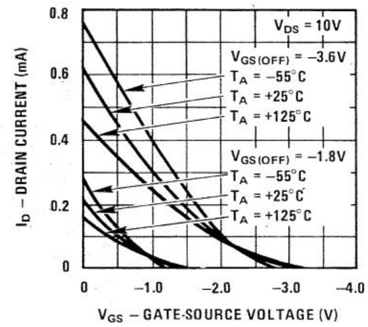
Transfer Characteristics



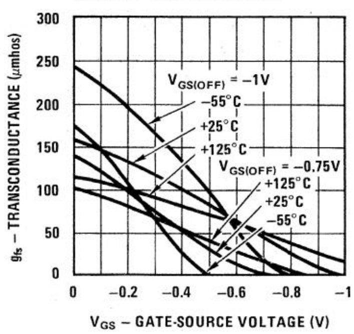
Transfer Characteristics



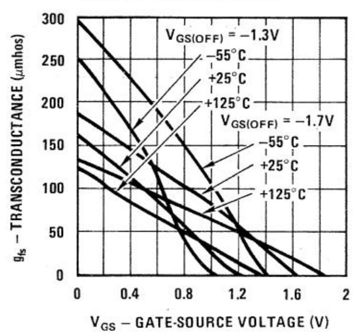
Transfer Characteristics



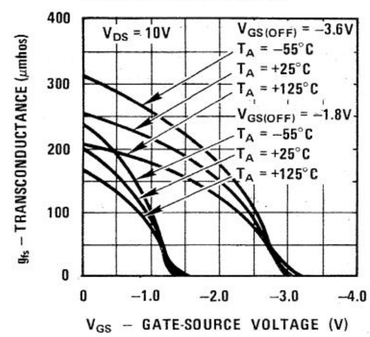
Transfer Characteristics



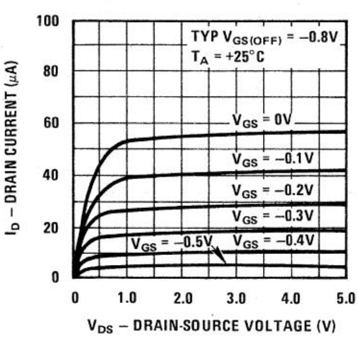
Transfer Characteristics



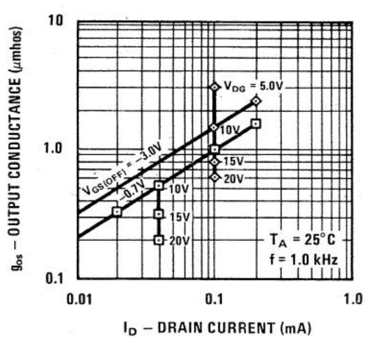
Transfer Characteristics



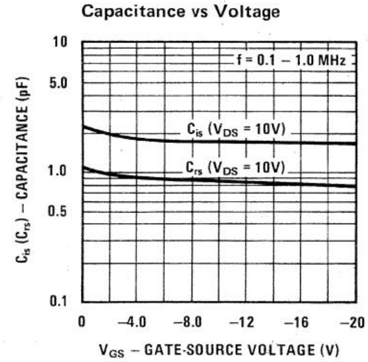
Common Drain-Source Characteristics



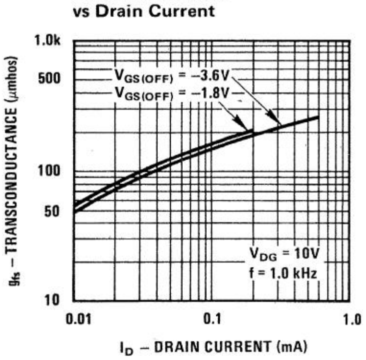
Output Conductance vs Drain Current



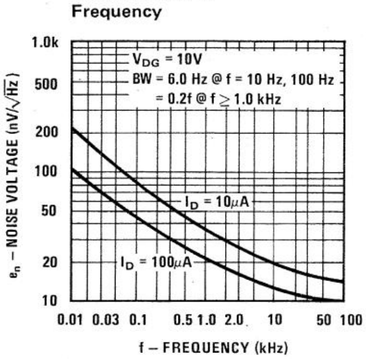
Capacitance vs Voltage



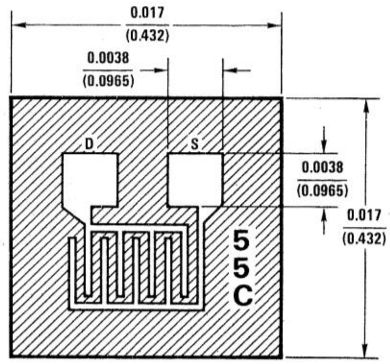
Transconductance vs Drain Current



Noise Voltage vs Frequency



Process 55 N-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 55 is a general purpose low level audio amplifier and switching transistor. Wafer processing is similar to process 52 but process 55 uses a larger geometry. This results in higher Y_{fs}, I_{DSS}, and capacitance and lower $R_{DS(ON)}$. It is useful for audio and video frequency amplifiers and RF amplifiers under 50 MHz. It may also be used for analog switching applications.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0	0.5	5.0	20	mA
Forward Transconductance	g_{fs}	V_{DS} = 20V, V_{GS} = 0	2.0	4.5	7.0	mmho
Forward Transconductance	g_{fs}	V_{DG} = 15V, I_D = 200 μA		1200		μmhos
Reverse Gate Leakage	I_{GSS}	V_{GS} = −30V, V_{DS} = 0		−10	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	140	250	600	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 20V, I_D = 1 nA	−0.5	−2.0	−8.0	V
Feedback Capacitance	C_{rss}	V_{DG} = 15V, V_{GS} = 0, f = 1 MHz		1.5	2.0	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		6.0	7.0	pF
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 200 μA		2		μmhos
Noise Voltage	e_n	V_{DG} = 15V, I_D = 200 μA, f = 100 Hz		10		$nV/\sqrt{Hz}$

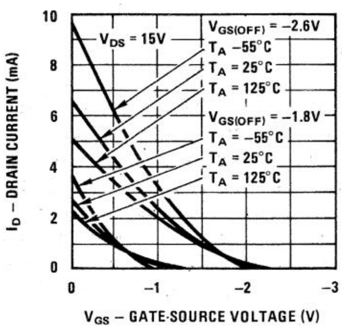
Examples of process 55 part numbers are as follows.

*Denotes preferred parts.

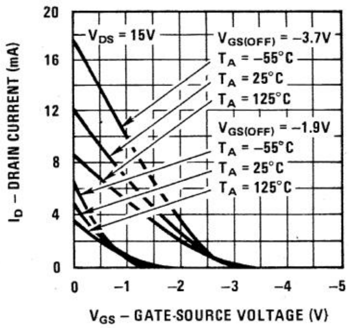
2N3436	*2N5361
2N3437	*2N5362
2N3438	*2N5363
	*2N5364
2N3821	
2N3822	*2N5457
2N3824	*2N5458
2N4220	*2N5459
2N4220A	MPF103
2N4221	MPF104
2N4221A	MPF105
2N4222	MPF108
2N4222A	MPF109
*2N5358	MPF112
*2N5359	PN4220
*2N5360	PN4221
	PN4222

Process 55

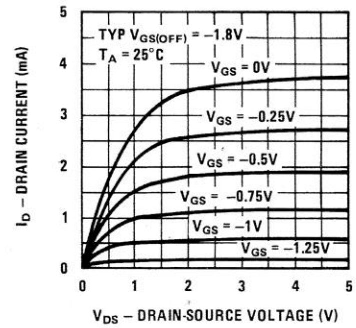
Transfer Characteristics



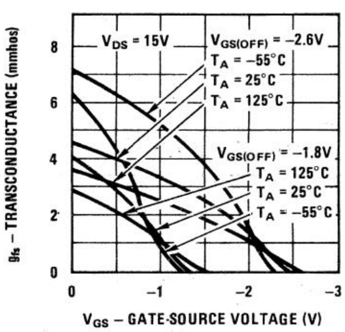
Transfer Characteristics



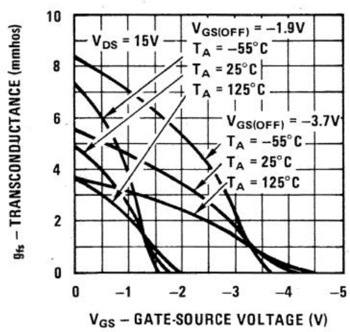
Common Drain-Source Characteristics



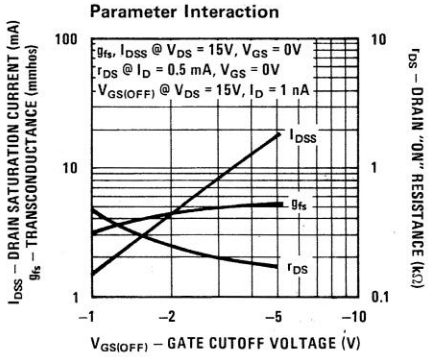
Transfer Characteristics



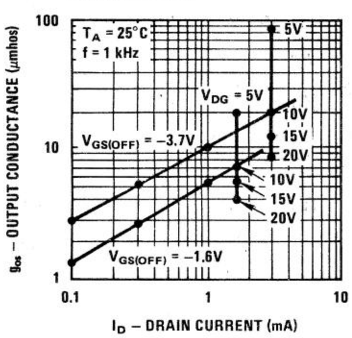
Transfer Characteristics



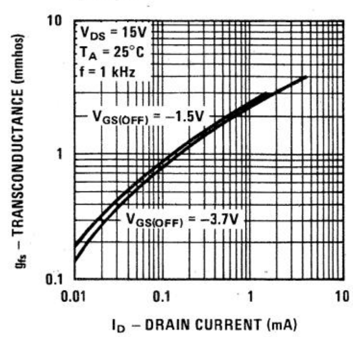
Parameter Interaction



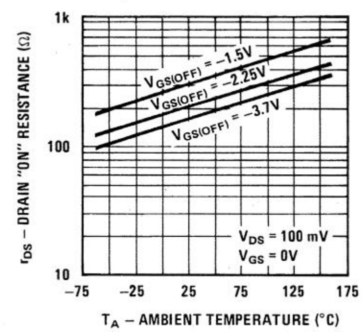
Output Conductance vs Drain Current



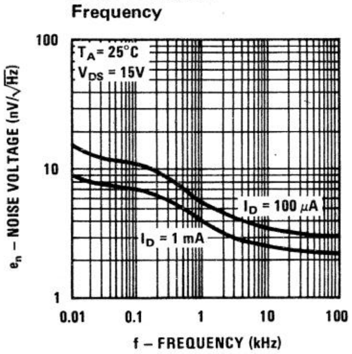
Transconductance vs Drain Current



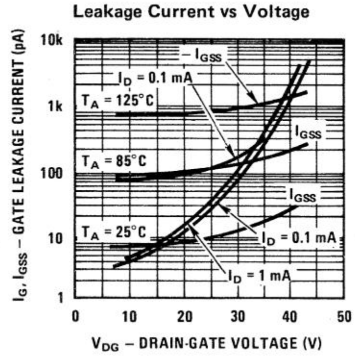
Channel Resistance vs Temperature



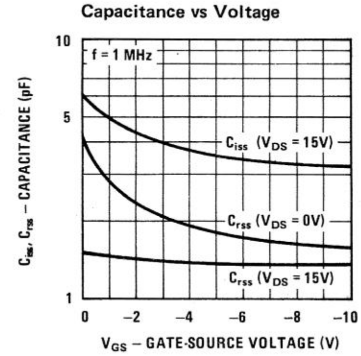
Noise Voltage vs Frequency



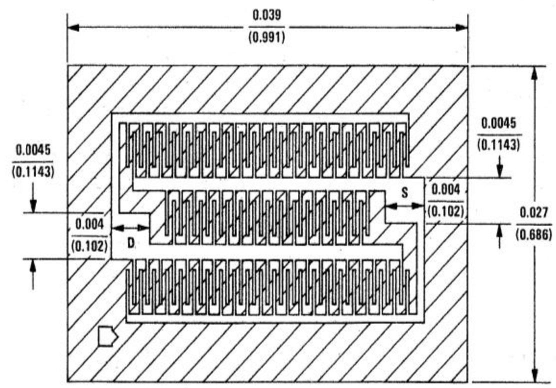
Leakage Current vs Voltage



Capacitance vs Voltage



Process 58 N-Channel JFET



GATE IS BACKSIDE CONTACT

DESCRIPTION

Process 58 was developed for analog or digital switching applications where very low $r_{DS(ON)}$ is mandatory. Switching times are very fast and $R_{DS(ON)}$ C_{iss} time constant is low. The 6Ω typical on resistance is very useful in precision multiplex systems where switch resistance must be held to an absolute minimum. With r_{DS} increasing only 0.7%/ °C, accuracy is retained over a wide temperature excursion.

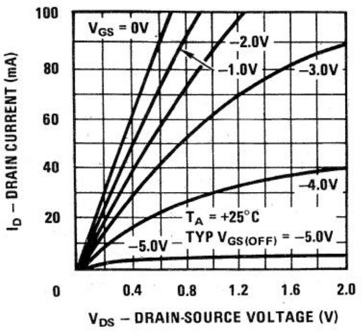
CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−25	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0 Pulse Test	100	400	1000	mA
Reverse Gate Leakage	I_{GSS}	V_{GS} = −15V, V_{DS} = 0		−50	−500	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	3.0	6.0	20	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 5V, I_D = 3 nA	−0.5	−5.0	−12	V
Drain "OFF" Current	$I_{D(OFF)}$	V_{DS} = 5V, V_{GS} = −10V		0.05	20	nA
Feedback Capacitance	C_{rss}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		12	25	pF
Input Capacitance	C_{iss}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		25	50	pF
Forward Transconductance	g_{fs}	V_{DG} = 10V, I_D = 2 mA		10		mmhos
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 2 mA		100		μmhos
Noise Voltage	e_n	V_{DG} = 15V, I_D = 2 mA, f = 100 Hz		6.0		nV/√Hz

Examples of process 58 part numbers are as follows. *Denotes preferred parts.

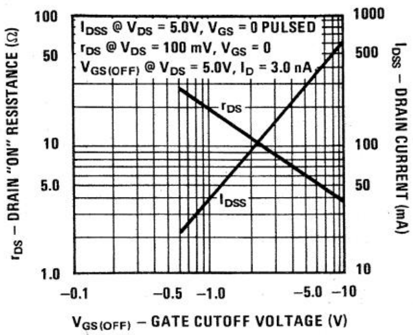
U320	*J108	*2N5432
U321	*J109	*2N5433
U322	*J110	*2N5434

Process 58

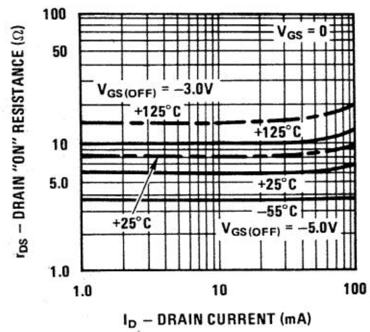
Common Drain-Source Characteristics



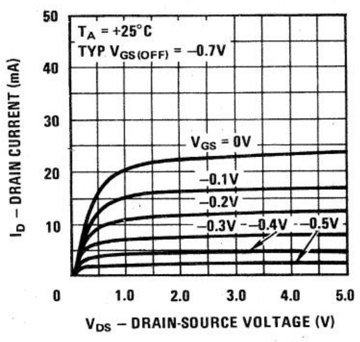
Parameter Interactions



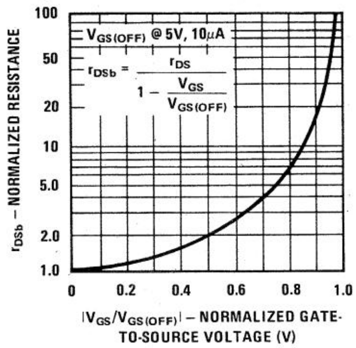
"ON" Resistance vs Drain Current



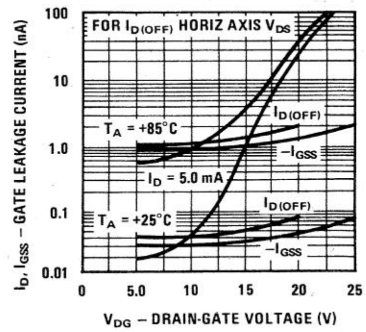
Common Drain-Source Characteristics



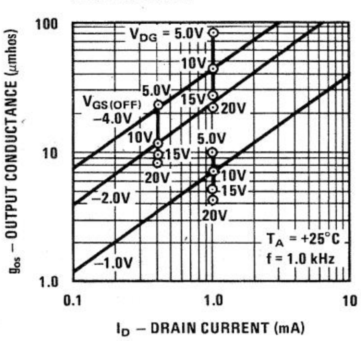
Normalized Drain Resistance vs Bias Voltage



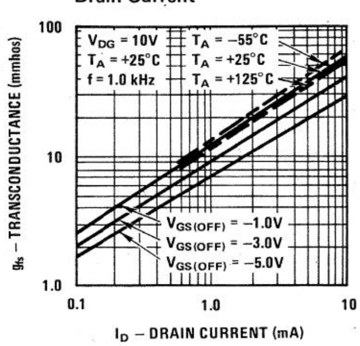
Leakage Current vs Voltage



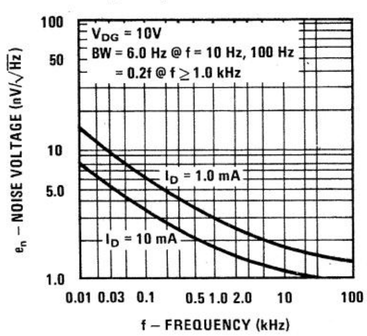
Output Conductance vs Drain Current



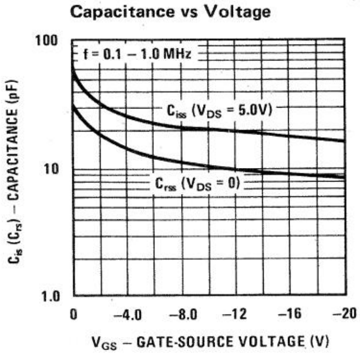
Transconductance vs Drain Current



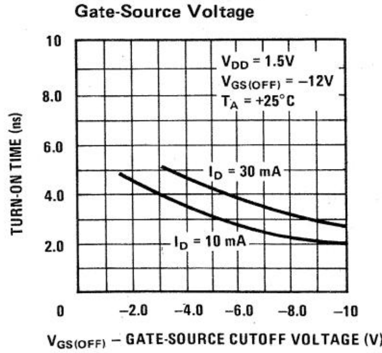
Noise Voltage vs Frequency



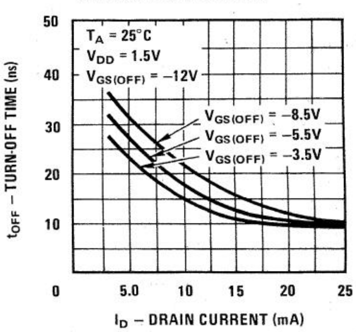
Capacitance vs Voltage



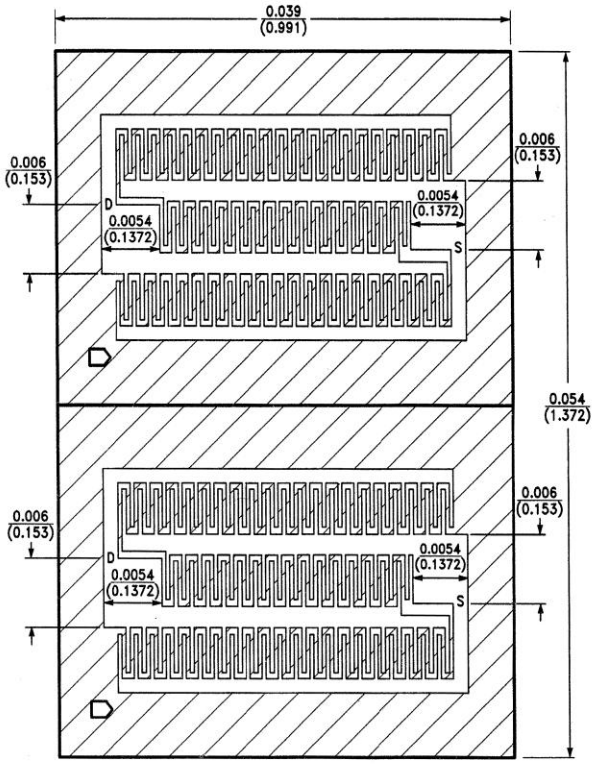
Switching Turn-On vs Gate-Source Voltage



Switching Turn-On Time vs Drain Current



Process 59 N-Channel JFET



Gate is also backside contact

TL/G/10035–60

DESCRIPTION

Process 59 is provided for analog or digital switching applications where very low $R_{DS(ON)}$ is mandatory. The 4Ω typical ON resistance is very useful where switch resistance must be held to an absolute minimum.

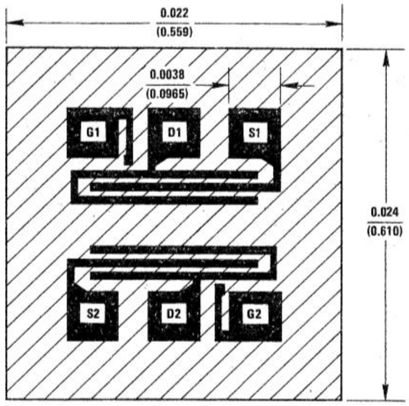
Electrical Characteristics (T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS} = 0V, I_G = −1 μA	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 15V, V_{GS} = 0V Pulse Test	100	600	1500	mA
I_{GSS}	Reverse Gate Leakage	V_{GS} = −15V, V_{DS} = 0V			1.0	nA
$r_{DS(ON)}$	ON Resistance	V_{DS} = 100 mV, V_{GS} = 0V	1.5	4.0	10	Ω
$V_{GS(OFF)}$	Pinch Off Voltage	V_{DS} = 5V, I_D = 100 nA	0.5	5.0	10	V
$I_{D(OFF)}$	Drain OFF Current	V_{DS} = 5V, V_{GS} = −10V		1.0	10	nA
C_{rss}	Feedback Capacitance	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		25	35	pF
C_{iss}	Input Capacitance	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		50	80	pF
g_{fs}	Forward Transconductance	V_{DG} = 10V, I_D = 2 mA		10		mmho
g_{os}	Output Conductance	V_{DG} = 10V, I_D = 2 mA		200		μmho
e_n	Noise Voltage	V_{DG} = 15V, I_D = 2 mA, f = 100 Hz		6.0		$nV/\sqrt{Hz}$

This process is available in the following device types.

J105
J106
J107

Process 83 N-Channel JFET



DESCRIPTION

Process 83 is a monolithic dual JFET with a diode isolated substrate. It is intended for operational amplifier input buffer applications. Processing results in low input bias current and virtually unmeasureable offset current. Likewise matching characteristics are virtually independent of operating current and voltage, providing design flexibility. Most GP 2N types are sorted from this family.

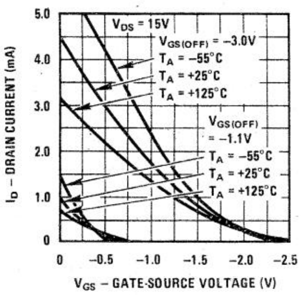
CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	$V_{DS} = 0V$, $I_G = -1\ \mu A$	−50	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 15V$, $V_{GS} = 0$	0.5	2.5	8.0	mA
Forward Trans-conductance	g_{fs}	$V_{DS} = 15V$, $V_{GS} = 0$	1.0	2.5	5.0	mmho
Pinch Off Voltage	$V_{GS(OFF)}$	$V_{DS} = 15V$, $I_D = 1$ nA	−0.5	−2.0	−4.5	V
Gate Current	I_G	$V_{DG} = 20V$, $I_D = 0.2$ mA		3.0	50	pA
Forward Trans-conductance	g_{fs}	$V_{DG} = 15V$, $I_D = 0.2$ mA	600	850		μmhos
Output Conductance	g_{os}	$V_{DG} = 15V$, $I_D = 0.2$ mA		1.0	5.0	μmhos
"ON" Resistance	r_{DS}	$V_{DS} = 100$ mV, $V_{GS} = 0$		450		Ω
Noise Voltage	e_n	$V_{DG} = 15V$, $I_D = 0.2$ mA, f = 100 Hz		10	50	$nV/\sqrt{Hz}$
Differential Match	$\lvert V_{GS1} - V_{GS2} \rvert$	$V_{DG} = 15V$, $I_D = 0.2$ mA		7.0	25	mV
Differential Match	ΔV_{GS1-2}	$V_{DG} = 15V$, $I_D = 0.2$ mA		10	50	$\mu V/^\circ C$
Common Mode Rejection	CMRR	$V_{DG} = 15V$, $I_D = 0.2$ mA	80	95		dB
Feedback Capacitance	C_{rs}	$V_{DG} = 15V$, $I_D = 0.2$ mA, f = 1 MHz		1.0	1.2	pF
Input Capacitance	C_{is}	$V_{DG} = 15V$, $I_D = 0.2$ mA, f = 1 MHz		3.4	4.0	pF

Examples of process 83 part numbers are as follows. *Denotes preferred parts.

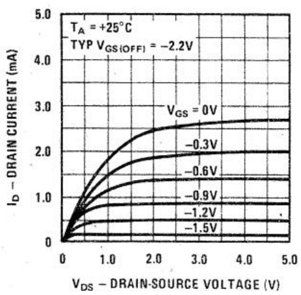
2N3921	2N5047	U233	J410
2N3922	*2N5196	U234	J411
*2N3954	*2N5197	U235	J412
*2N3954A	*2N5198		
*2N3955	*2N5199		*NPD8301
*2N3955A	2N5452		*NPD8302
*2N3956	2N5453		*NPD8303
*2N3957	2N5454		
*2N3958	*2N5545		
2N4084	*2N5546		
2N4085	*2N5547		
2N5045	U231		
2N5046	U232		

Process 83

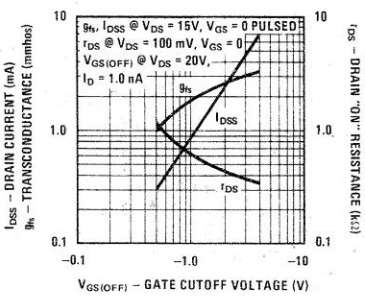
Transfer Characteristics



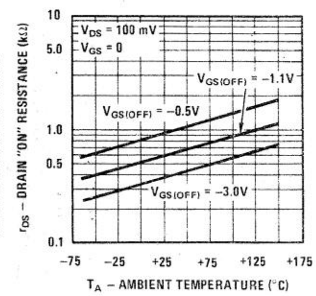
Common Drain-Source Characteristics



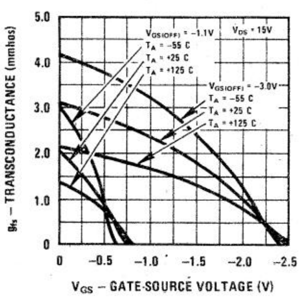
Parameter Interactions



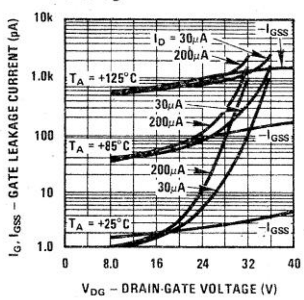
Channel Resistance vs Temperature



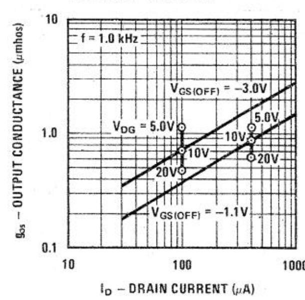
Transfer Characteristics



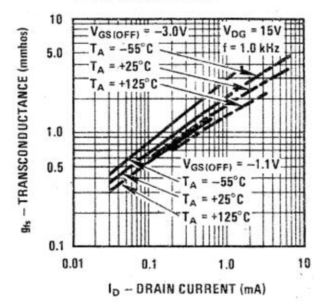
Leakage Current vs Voltage



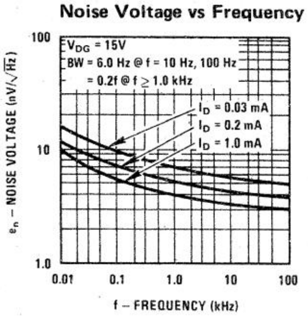
Output Conductance vs Drain Current



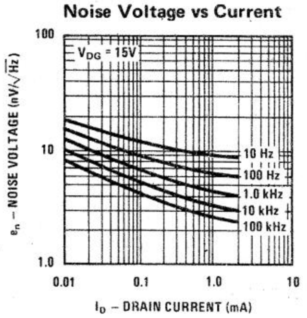
Transconductance vs Drain Current



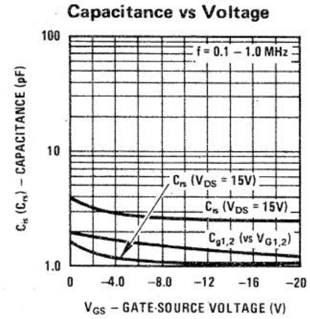
Noise Voltage vs Frequency



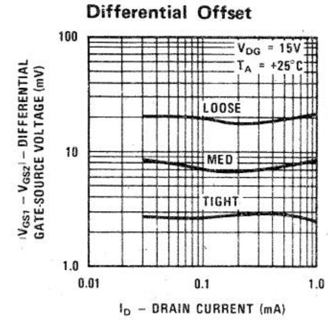
Noise Voltage vs Current



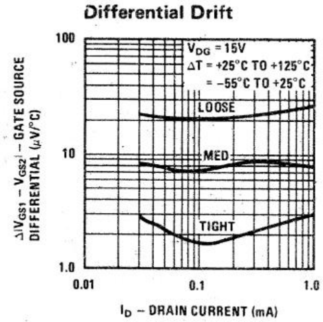
Capacitance vs Voltage



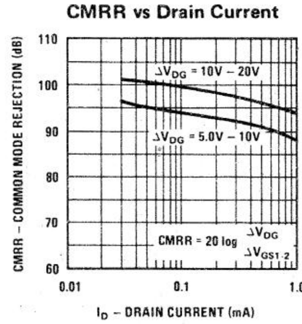
Differential Offset



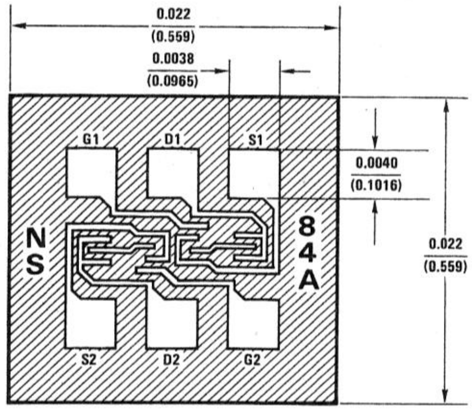
Differential Drift



CMRR vs Drain Current



Process 84 N-Channel JFET



DESCRIPTION

Process 84 is a monolithic dual JFET with a diode isolated substrate. It is designed for the most critical operational amplifier input stages or electrometer single ended preamp. Ideal for medical applications and instrumentation inputs where subpicoamp inputs are important. Device design considered high CMRR, subpicoamp leakage over wide input swings, low capacitance, and tight match over wide current range.

CHARACTERISTIC	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−60		V
Drain Saturation Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0V	20	300	1000	μA
Forward Transconductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0V	90	180	300	μV
Forward Transconductance	g_{fs}	V_{DS} = 15V, I_D = 30 μA	50	120	150	μV
Gate Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	0.5	2	4.5	V
Reverse Gate Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = −20V		1	5	pA
Gate Leakage Current	I_G	V_{DG} = 10V, I_D = 30 μA		0.5	3	pA
Feedback Capacitance	C_{rss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		0.3	0.4	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f =1 MHz		2	3	pF
Noise Voltage	e_n	V_{DS} = 15V, I_D = 30 μA, f = 1 kHz		30	50	$nV/\sqrt{Hz}$
Noise Voltage	e_n	V_{DS} = 15V, I_D = 30 μA, f = 10 Hz		180		$nV/\sqrt{Hz}$
Output Conductance	g_{os}	V_{DS} = 10V, I_D = 30 μA		0.1	0.2	μV
Differential Gate-Source Voltage	$\|V_{GS1}-V_{GS2}\|$	V_{DS} = 10V, I_D = 30 μA		12	25	mV
Differential Gate-Source Voltage Drift	ΔV_{GS1-2}	V_{DS} = 10V, I_D = 30 μA		10	50	μV/°C
Common-Mode Rejection Ratio	CMRR	V_{DS} = 10V, I_D = 30 μA		112		dB

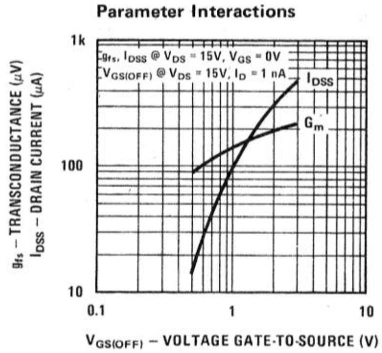
Examples of process 84 part numbers are as follows.

*Denotes preferred parts.

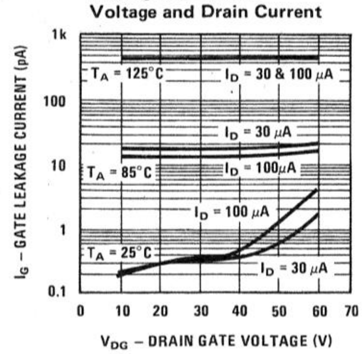
2N5902
2N5903
2N5904
2N5905

*2N5906
*2N5907
*2N5908
*2N5909

Parameter Interactions

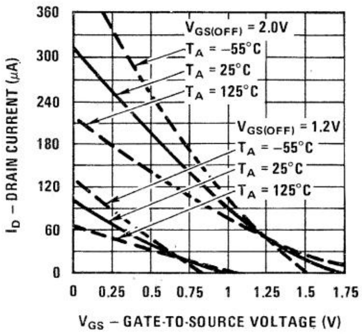


Leakage Current vs Voltage and Drain Current

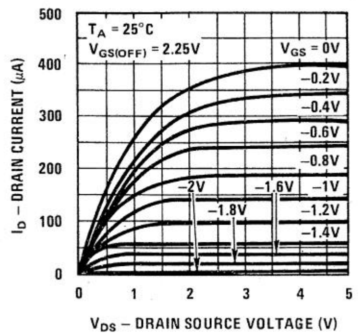


Process 84

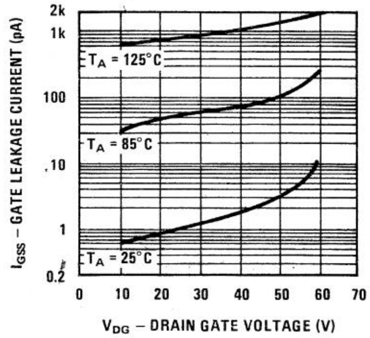
Transfer Characteristics



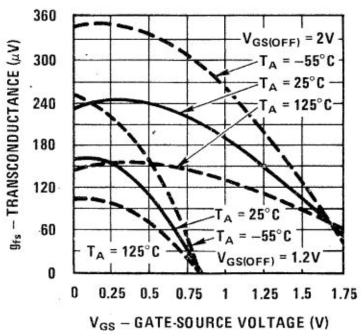
Common Drain-Source Characteristics



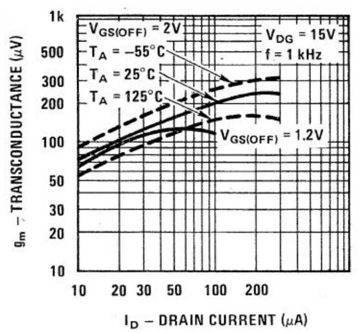
Leakage Current vs Voltage



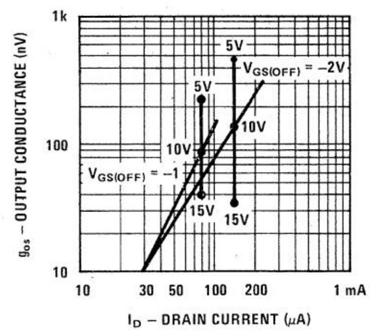
Transfer Characteristics



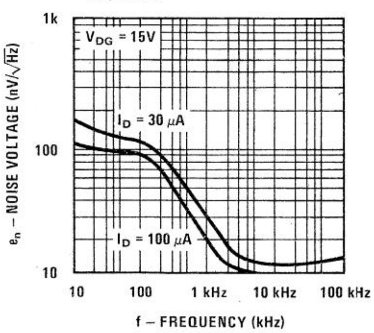
Transconductance vs Drain Current



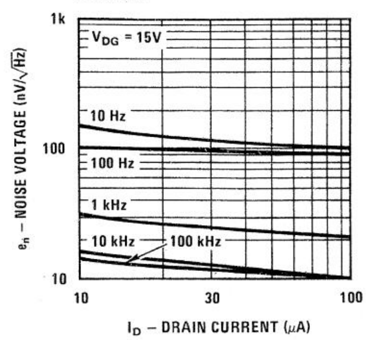
Output Conductance vs Drain Current



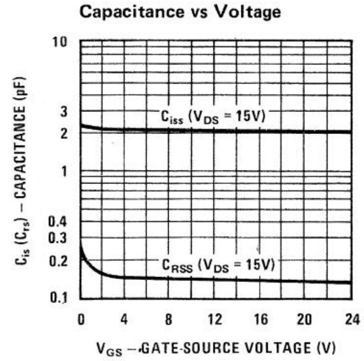
Noise Voltage vs Frequency



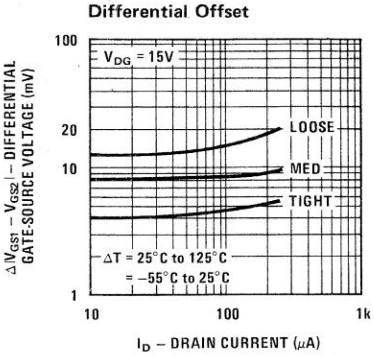
Noise Voltage vs Current



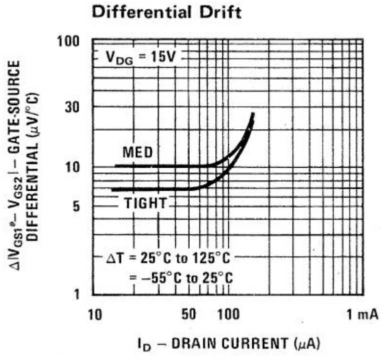
Capacitance vs Voltage



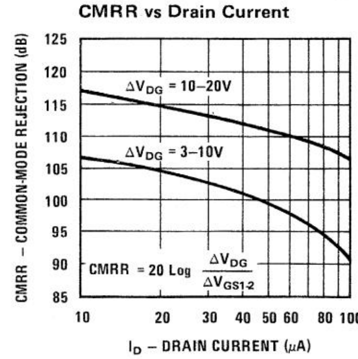
Differential Offset



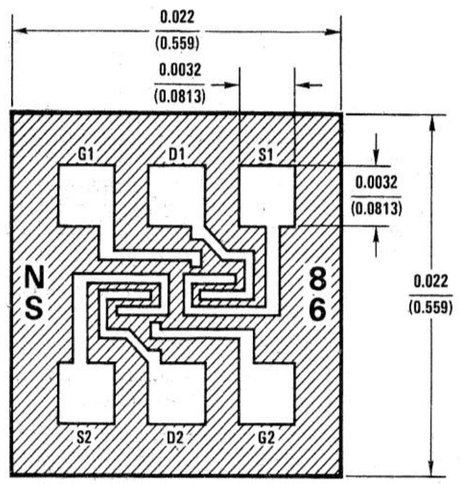
Differential Drift



CMRR vs Drain Current



Process 86 Monolithic Dual JFET



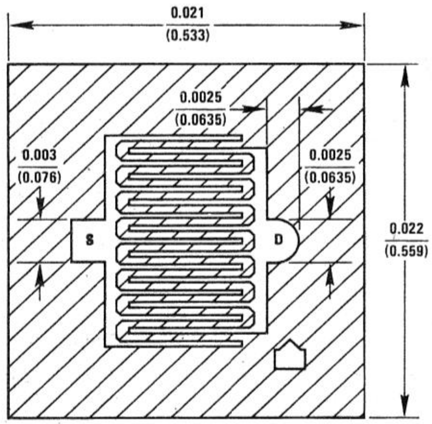
DESCRIPTION

Process 86 is a monolithic dual JFET with a diode isolated substrate. It is intended for critical amplifier input stages requiring low noise, sub picoamp bias currents and high gain. Exacting process control results in consistent parameter distribution with tight match and low drift.

This process is available in the following device types. *Denotes preferred parts.

U421
U422
U423
U424
U425
U426

Process 88 P-Channel JFET



DESCRIPTION

Process 88 is designed primarily for electronic switching applications where a P channel device is desirable. Inherent zero offset voltage, low leakage and low $R_{DS(ON)}$ C_{iss} time constant make this device excellent for low level analog switching, sample and hold circuits and chopper stabilized amplifiers. This device is the complement to Process 51.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = 1 μA	30	40		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −15V, V_{GS} = 0	−5.0	−30	−90	mA
Forward Trans-conductance	g_{fs}	V_{DS} = −15V, V_{GS} = 0	4.0	13	17	mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = −15V, I_D = −2 mA		3.5		mmhos
Gate Leakage	I_{GSS}	V_{GS} = 20V, V_{DS} = 0		0.05	1.0	nA
"ON" Resistance	r_{DS}	V_{DS} = −100 mV, V_{GS} = 0	50	80	200	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = −15V, I_D = −1 nA	0.5	5.0	10	V
Drain "OFF" Current	$I_{D(OFF)}$	V_{DS} = −15V, V_{GS} = 10V		−0.05	−10	nA
Feedback Capacitance	C_{rss}	V_{DG} = −15V, I_D = −2 mA, f = 1 MHz		4.0	5.0	pF
Input Capacitance	C_{iss}	V_{DS} = −15V, I_D = −2 mA, f = 1 MHz		14	15	pF
Output Conductance	g_{os}	V_{DG} = −15V, I_D = −2 mA		100	300	μmhos
Noise Voltage	e_n	V_{DG} = −15V, I_D = −2 mA, f = 100 Hz		20		nV/√Hz

This process is available in the following device types. *Denotes preferred parts.

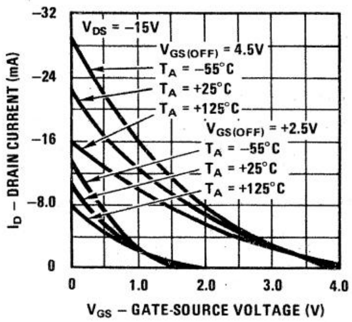
2N2609	2N3382	*J174
2N4382	2N3384	*J175
2N5018	2N3386	*J176
2N5019	2N3993	*J177
*2N5114	2N3993A	*J270
*2N5115	2N3994	*J271
*2N5116	2N3994A	
U300		
U301		
U304	P1086E	
U305	P1087E	
U306	PN4343	

QUALIFIED PER MIL-S-19500

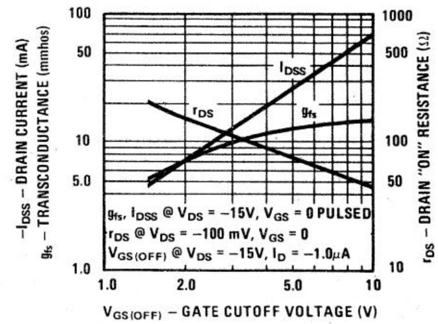
*2N5114JAN, JANTX, JANTXV
*2N5115JAN, JANTX, JANTXV
*2N5116JAN, JANTX, JANTXV

Process 88

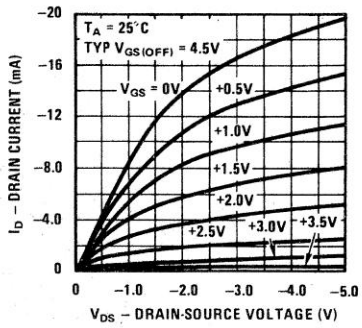
Transfer Characteristics



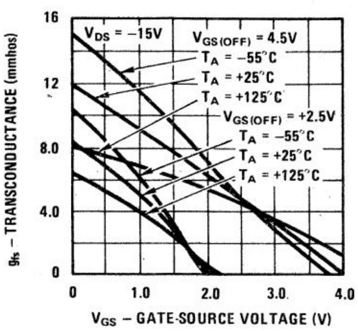
Parameter Interactions



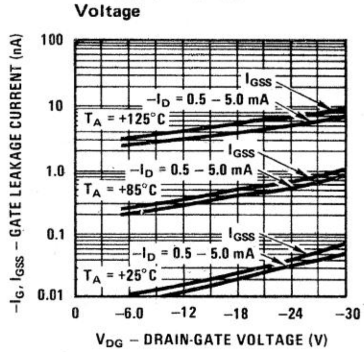
Common Drain-Source Characteristics



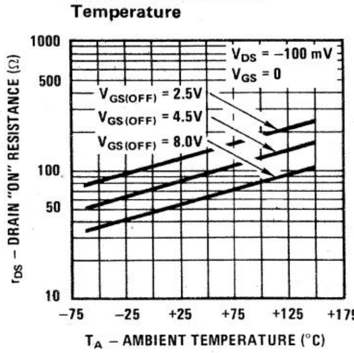
Transfer Characteristics



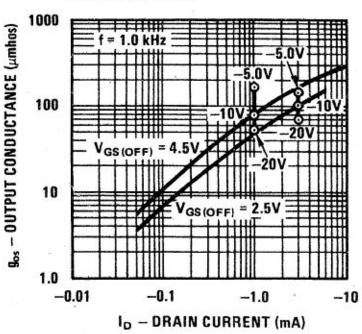
Leakage Current vs Voltage



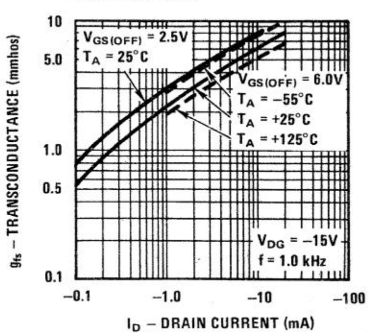
Channel Resistance vs Temperature



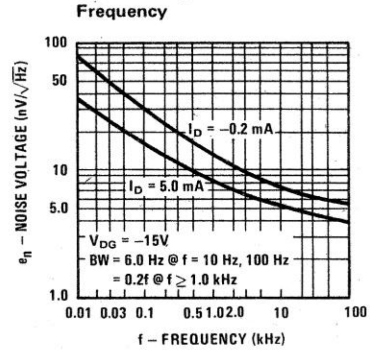
Output Conductance vs Drain Current



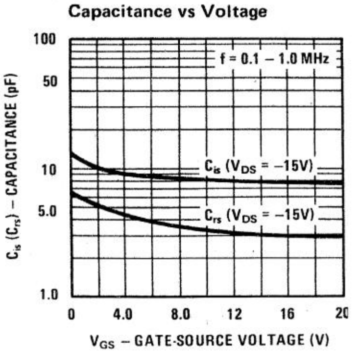
Transconductance vs Drain Current



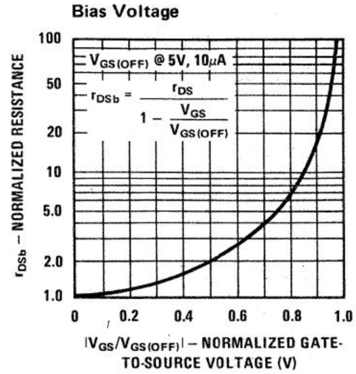
Noise Voltage vs Frequency



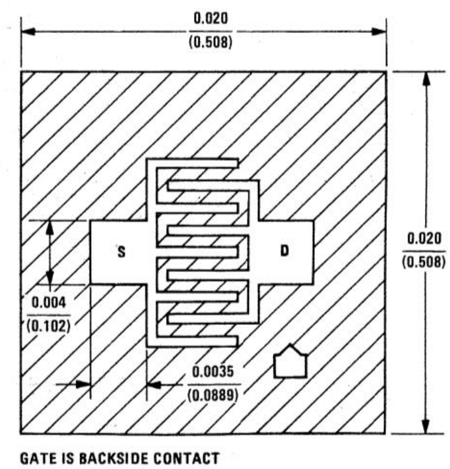
Capacitance vs Voltage



Normalized Drain Resistance vs Bias Voltage



Process 89 P-Channel JFET



DESCRIPTION

Process 89 is designed primarily for low level amplifier applications. This device is the complement to Process 55. Commonly used in voltage variable resistor applications.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = 1 μA	20	40		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −15V, V_{GS} = 0	−0.3	−4.0	−20	mA
Forward Transconductance	g_{fs}	V_{DS} = −15V, V_{GS} = 0	1.0	2.5	4.0	mmhos
Forward Transconductance	g_{fs}	V_{DG} = −15V, I_D = −0.2 mA		700		μmhos
Gate Leakage	I_{GSS}	V_{GS} = 20V, V_{DS} = 0		0.02	1.0	nA
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = −15V, I_D = −1 nA	0.5	3.0	9.0	V
Feedback Capacitance	C_{rss}	V_{DG} = −15V, V_{GS} = 0, f = 1 MHz		2.0	2.5	pF
Input Capacitance	C_{is}	V_{DS} = −15V, I_D = −2 mA, f = 1 MHz		7.0	8.5	pF
"ON" Resistance	r_{DS}	V_{DS} = −100 mV, V_{GS} = 0		450		Ω
Output Conductance	g_{os}	V_{DG} = −15V, I_D = −0.2 mA		5.0	15	μmhos
Noise Voltage	e_n	V_{DG} = −15V, I_D = −0.2 mA, f = 100 Hz		30		$nV/\sqrt{Hz}$

This process is available in the following device types. *Denotes preferred parts.

2N2608
2N4381
2N5020
2N5021

2N3329
2N3330
2N3331
2N3332

*2N5460
*2N5461
*2N5462
PN4342
PN4360
PN5033

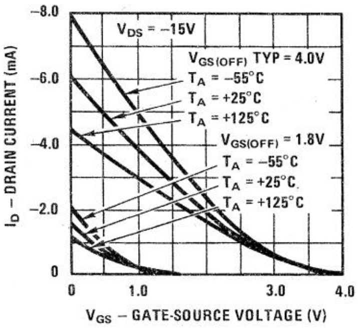
2N3820

QUALIFIED PER MIL-S-19500

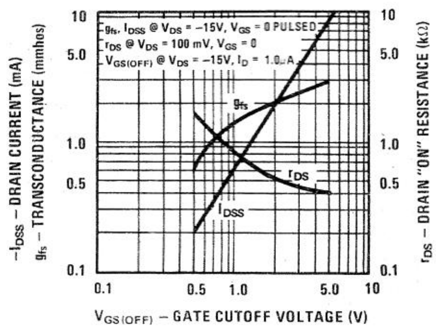
2N2608JAN

Process 89

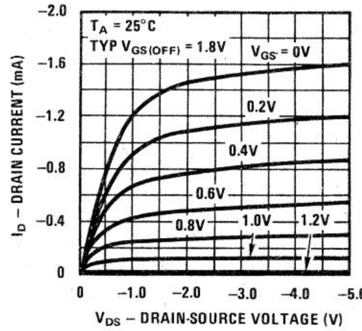
Transfer Characteristics



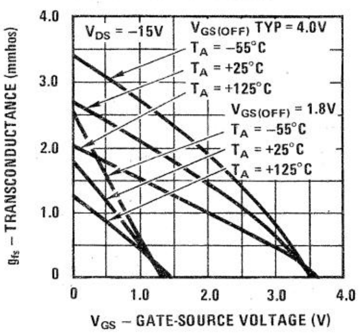
Parameter Interactions



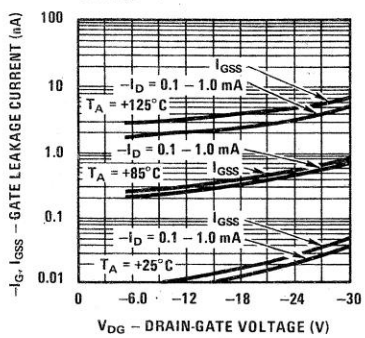
Common Drain-Source Characteristics



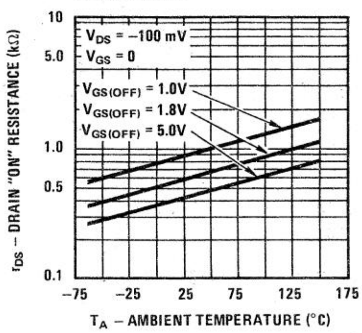
Transfer Characteristics



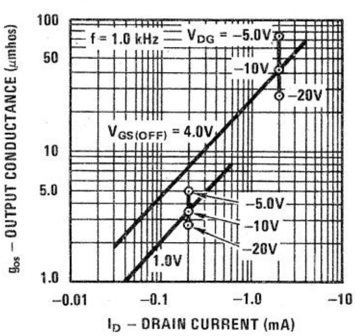
Leakage Current vs Voltage



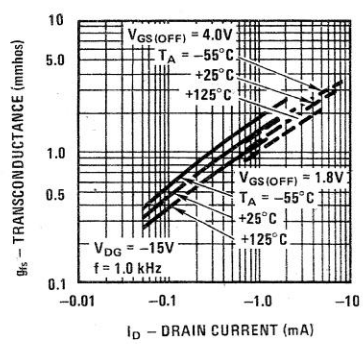
Channel Resistance vs Temperature



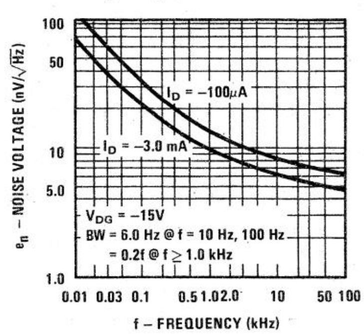
Output Conductance vs Drain Current



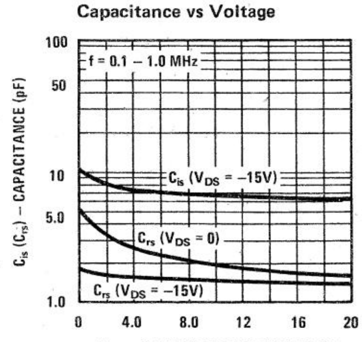
Transconductance vs Drain Current



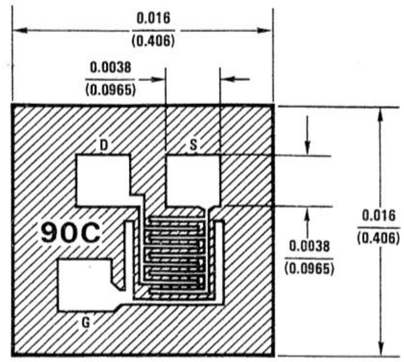
Noise Voltage vs Frequency



Capacitance vs Voltage



Process 90 P-Channel JFET



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

Process 90 is designed for VHF/UHF mixer/amplifier and applications where Process 50 is not adequate. Has sufficient gain and low noise, common gate configuration at 450 MHz, for sensitive receivers. The high transconductance and square law characteristics insures low crossmodulation and intermodulation distortions. Common-gate operation simplifies circuitry. Consider Process 92 for even higher performance.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−20	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0	3	18	40	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0	5.5	8.0	10	mmhos
Forward Trans-conductance	g_{fs}	V_{DS} = 10V, I_D = 5 mA	4.5	5.8		mmhos
Reverse Gate Current	I_{GSS}	V_{GS} = −15V, V_{DS} = 0		−5.0	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0		90		Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−1.5	−3.5	−6.0	V
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 5 mA		45	100	μmhos
Feedback Capacitance	C_{rs}	V_{DG} = 10V, I_D = 5 mA		1.0	1.2	pF
Input Capacitance	C_{is}	V_{DG} = 10V, I_D = 5 mA		4.0	5.0	pF
Noise Voltage	e_n	V_{DG} = 10V, I_D = 5 mA, f = 100 Hz		13		nV/√Hz
Noise Figure	NF	V_{DG} = 10V, I_D = 5 mA, f = 450 MHz		3.0		dB
Power Gain	G_{pg} (CG)	V_{DG} = 10V, I_D = 5 mA, f = 450 MHz		11		dB

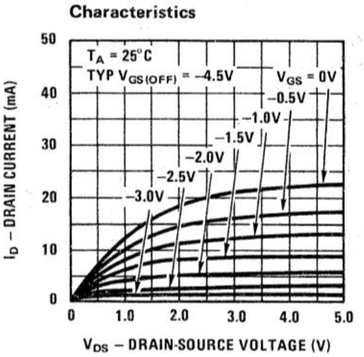
This process is available in the following device types. *Denotes preferred parts.

*2N5397
2N5398
U312

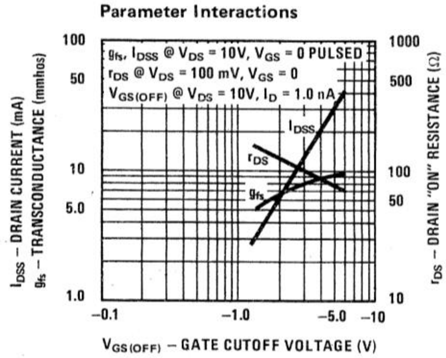
J114
*J210
*J211
*J212
*J300

*2N5245
*2N5246
*2N5247

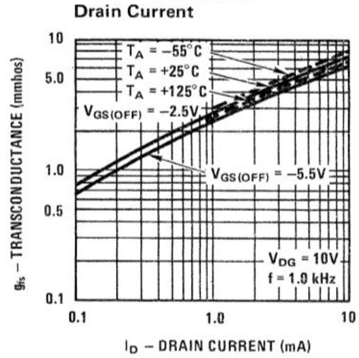
Common Drain-Source Characteristics



Parameter Interactions



Transconductance vs Drain Current

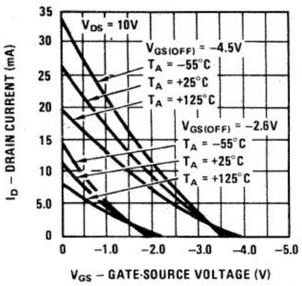


Process 90

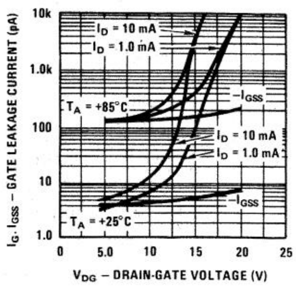
COMMON SOURCE

COMMON GATE

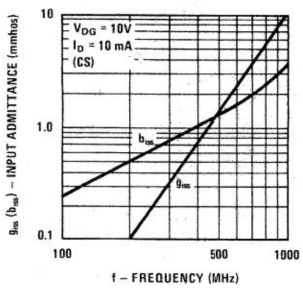
Transfer Characteristics



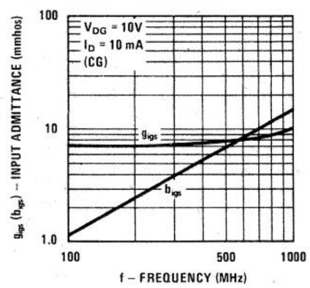
Leakage Current vs Voltage



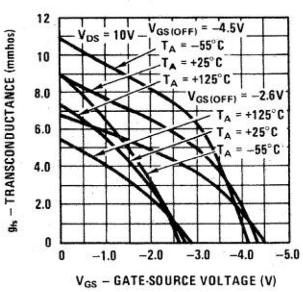
Input Admittance



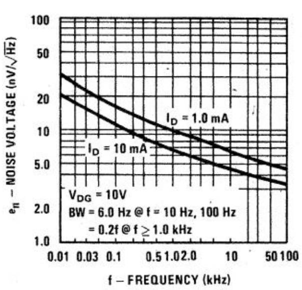
Input Admittance



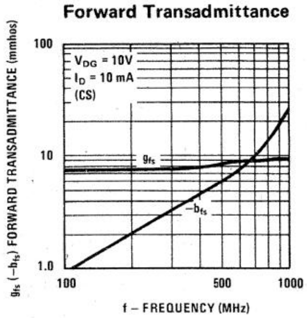
Transfer Characteristics



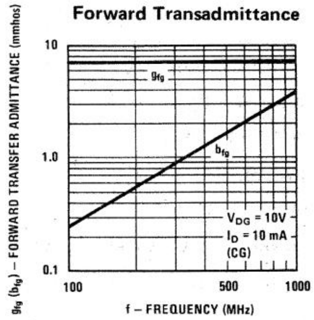
Noise Voltage vs Frequency



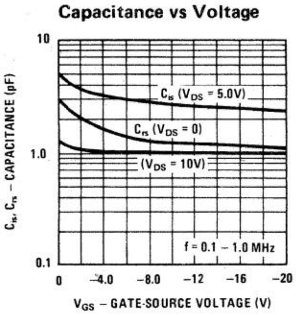
Forward Transadmittance



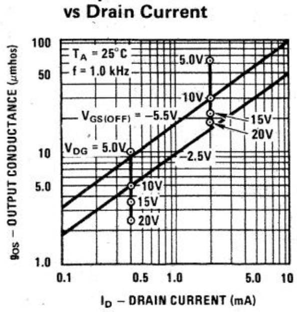
Forward Transadmittance



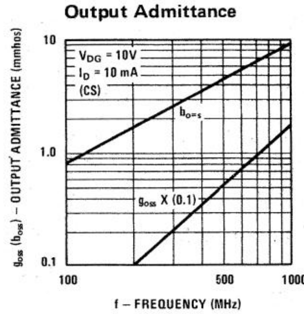
Capacitance vs Voltage



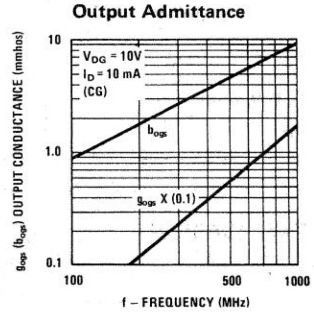
Output Conductance vs Drain Current



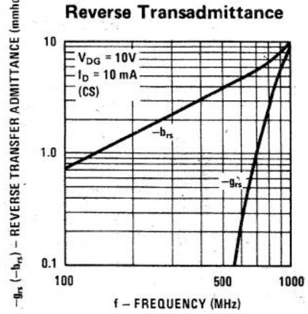
Output Admittance



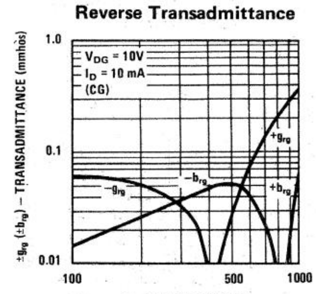
Output Admittance



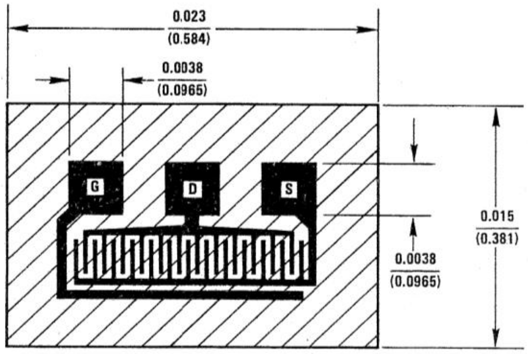
Reverse Transadmittance



Reverse Transadmittance



Process 92 N-Channel Junction Match



GATE IS ALSO BACKSIDE CONTACT

DESCRIPTION

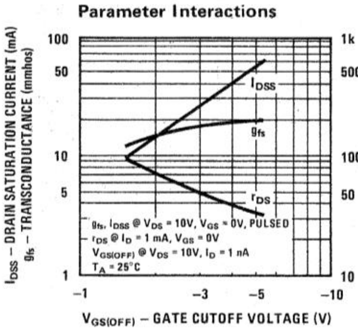
Process 92 is designed for VHF/UHF amplifier, oscillator, and mixer applications. As a common gate amplifier, 16 dB at 100 MHz and 12 dB at 450 MHz can be realized. Worst case 75 ohm input impedance provides ideal input match.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−20	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0, Pulsed	10	38	80	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0, Pulsed		19		mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = 10V, I_D = 10 mA	10	13	18	mmhos
Reverse Gate Current	I_{GSS}	V_{GS} = −15V, V_{DS} = 0		−15	−100	pA
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	35	45	80	Ω
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−1.5	−4.0	−6.5	V
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 10 mA		160	250	μmhos
Feedback Capacitance	C_{gd}	V_{DG} = 10V, I_D = 10 mA, f = 1 MHz		2.0	2.5	pF
Input Capacitance	C_{gs}	V_{DG} = 10V, I_D = 10 mA, f = 1 MHz		4.1	5.0	pF
Noise Voltage	e_n	V_{DG} = 10V, I_D = 10 mA, f = 100 Hz		6.0		nV/√Hz
Noise Figure	NF	V_{DG} = 10V, I_D = 10 mA, f = 450 MHz		3.0		dB
Power Gain	G_{pg}	V_{DG} = 10V, I_D = 10 mA, f = 450 MHz		12		dB

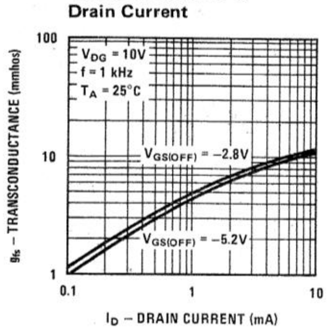
This process is available in the following device types. *Denotes preferred parts.

U308	U430	J308
*U309	U431	*J309
*U310		*J310

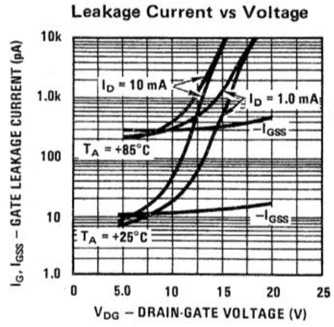
Parameter Interactions



Transconductance vs Drain Current

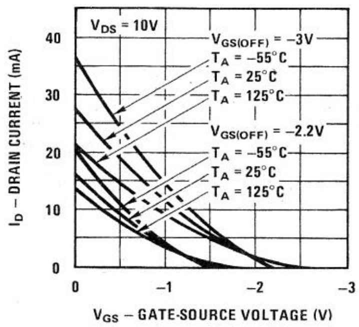


Leakage Current vs Voltage

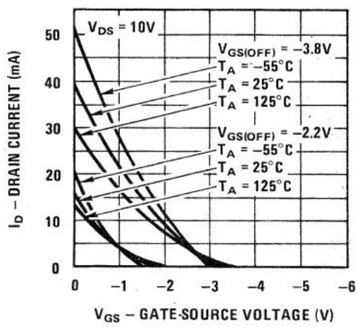


Process 92

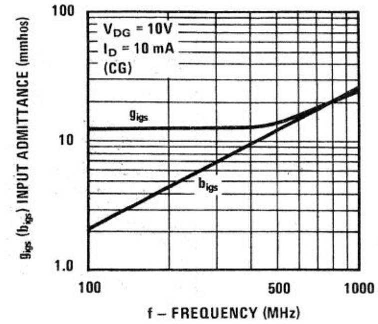
Transfer Characteristics



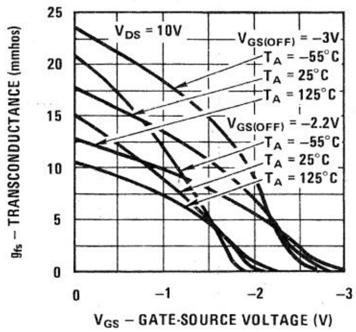
Transfer Characteristics



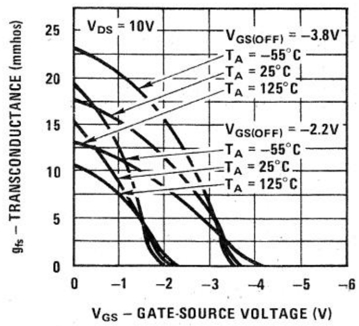
Input Admittance



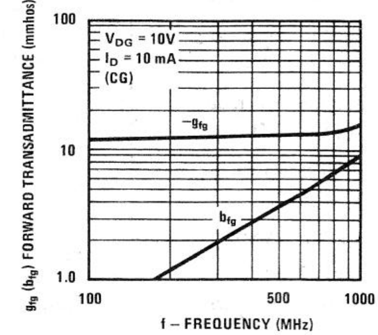
Transfer Characteristics



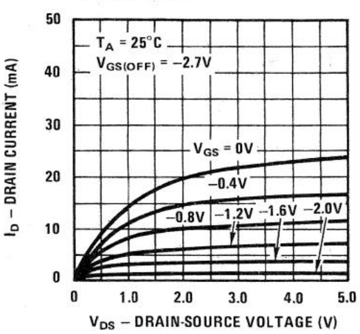
Transfer Characteristics



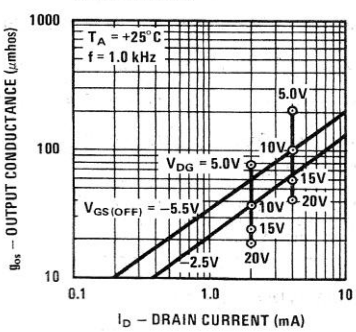
Forward Transadmittance



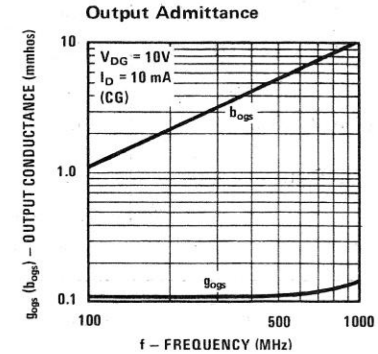
Common Drain-Source Characteristics



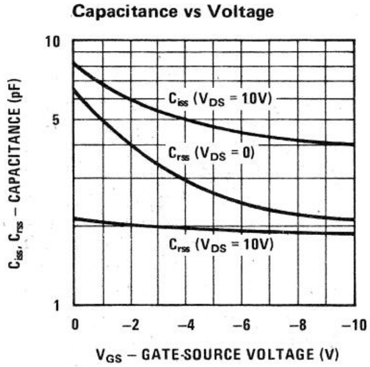
Output Conductance vs Drain Current



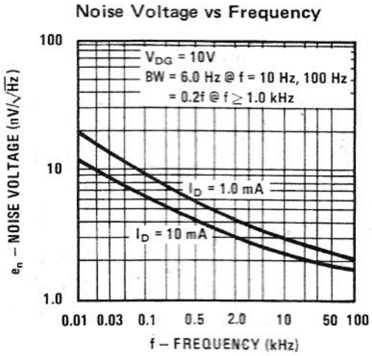
Output Admittance



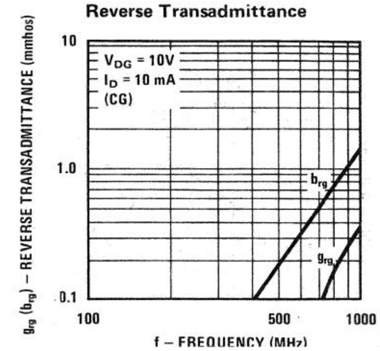
Capacitance vs Voltage



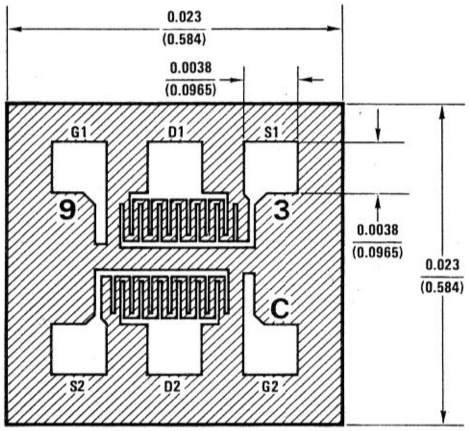
Noise Voltage vs Frequency



Reverse Transadmittance



Process 93 N-Channel JFET



DESCRIPTION

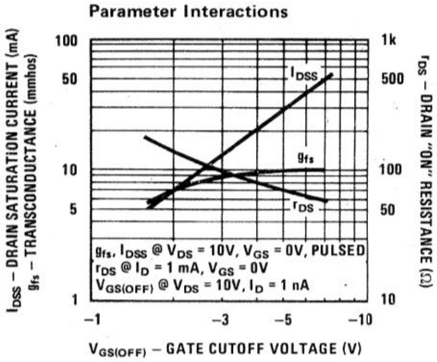
Process 93 is a monolithic dual JFET with a diode isolated substrate. It is intended for wide band, low noise, single ended video amplifier input stages, and high slew rate op amps. Monolithic structure eliminates thermal transient errors, and provides freedom to pick operating current and voltage.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−25	−30		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10V, V_{GS} = 0, Pulsed	3.0	18	40	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 10V, V_{GS} = 0, Pulsed		8.0		mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = 10V, I_D = 5 mA	5.0	6.0	10	mmhos
Output Conductance	g_{os}	V_{DG} = 10V, I_D = 5 mA		50	100	μmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 10V, I_D = 1 nA	−1.5	−3.5	−6.0	V
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0		100		Ω
Gate Current	I_G	V_{DG} = 10V, I_D = 5 mA		10	100	pA
Noise Voltage	e_n	V_{DG} = 10V, I_D = 5 mA, f = 100 Hz		9.0	30	nV/√Hz
Differential Match	$\|V_{GS1}-V_{GS2}\|$	V_{DG} = 10V, I_D = 5 mA		9.0	30	mV
Differential Match	ΔV_{GS1-2}	V_{DG} = 10V, I_D = 5 mA		15	40	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 10V, I_D = 5 mA		90		dB
Feedback Capacitance	C_{rs}	V_{DG} = 10V, I_D = 5 mA, f = 1 MHz		1.0	1.2	pF
Input Capacitance	C_{is}	V_{DG} = 10V, I_D = 5 mA, f = 1 MHz		4.2	5.0	pF

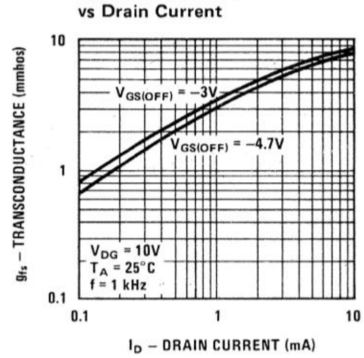
This process is available in the following device types. *Denotes preferred parts.

*2N5911
*2N5912
U257

Parameter Interactions

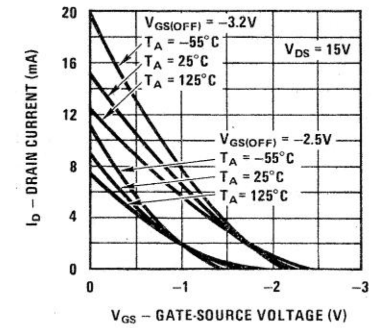


Transconductance vs Drain Current

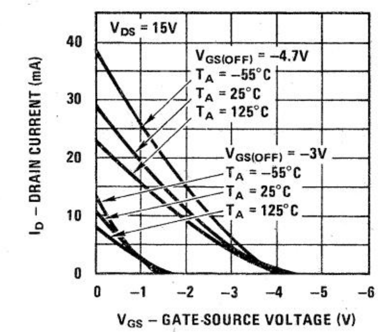


Process 93

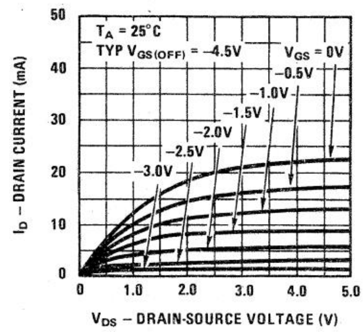
Transfer Characteristics



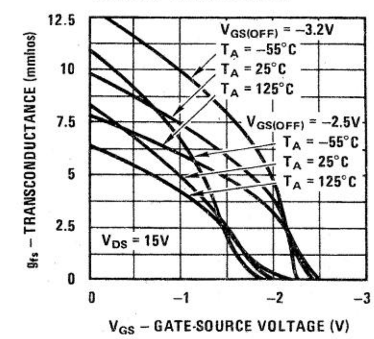
Transfer Characteristics



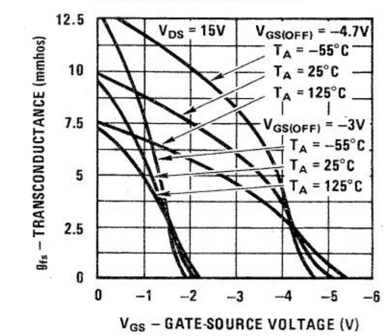
Common Drain-Source Characteristics



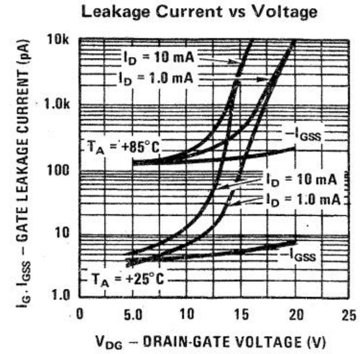
Transfer Characteristics



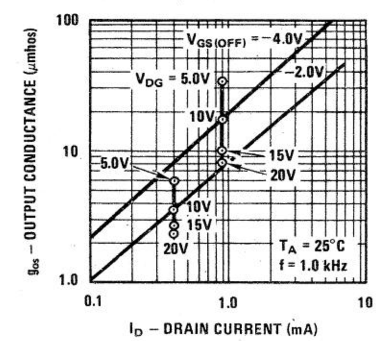
Transfer Characteristics



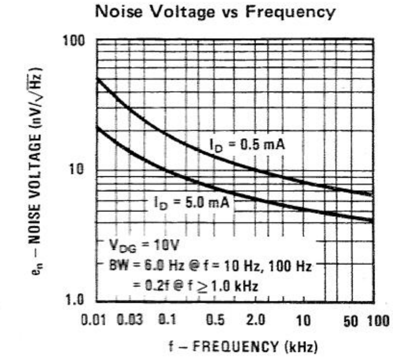
Leakage Current vs Voltage



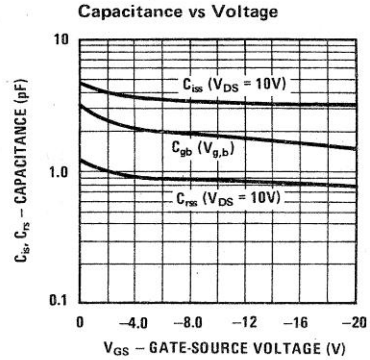
Output Conductance vs Drain Current



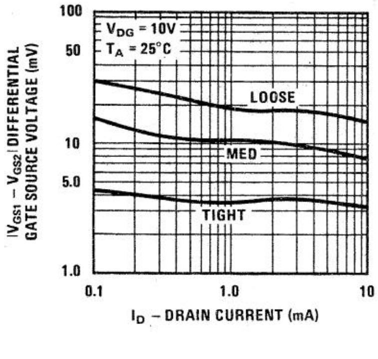
Noise Voltage vs Frequency



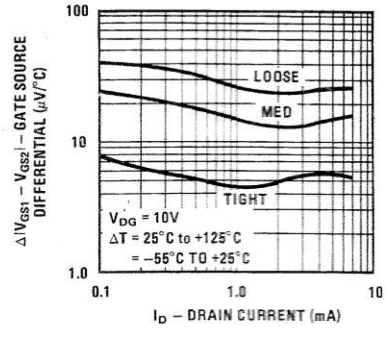
Capacitance vs Voltage



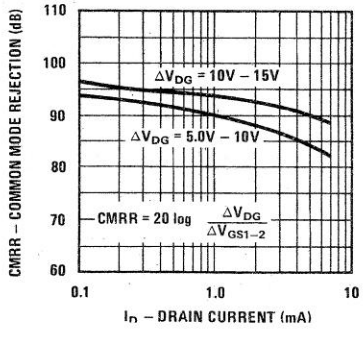
Differential Offset



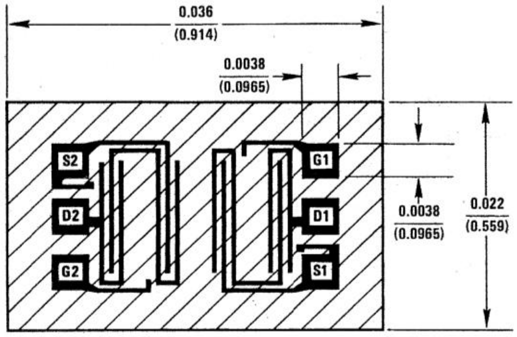
Differential Drift



CMRR vs Drain Current



Process 93 P-Channel JFET



DESCRIPTION

Process 94 is a monolithic dual JFET. It is strictly intended for operational amplifier input buffer applications. Special processing results in extremely low input bias current and virtually unmeasureable offset current. It is important to note that the <5 pico ampere bias current is measured at 35 volts. Typical CMRR is 125 dB. Performance superior to electrometer tubes can be readily achieved with low offset voltage and almost zero long term drift.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0	0.5	3.0	10	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	1.5	3.5	7.0	mmho
Forward Trans-conductance	g_{fs}	V_{DG} = 15V, I_D = 0.2 mA	0.9	1.2	1.8	mmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA	−0.5	−2.0	−6.0	V
Gate Current	I_G	V_{DG} = 35V, I_D = 0.20 mA		1.0	15	pA
Feedback Capacitance	C_{rss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		0.01	0.02	pF
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0, f = 1 MHz		4.0	5.0	pF
Noise Voltage	e_n	V_{DG} = 15V, I_D = 0.2 mA, f = 10 Hz		12	50	$nV/\sqrt{Hz}$
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 0.2 mA		<0.1		μmhos
Differential Match	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 15V, I_D = 0.2 mA		5.0	25	mV
Differential Match	ΔV_{GS1-2}	V_{DG} = 15V, I_D = 0.2 mA		6.0	50	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 15V, I_D = 0.2 mA		125		dB

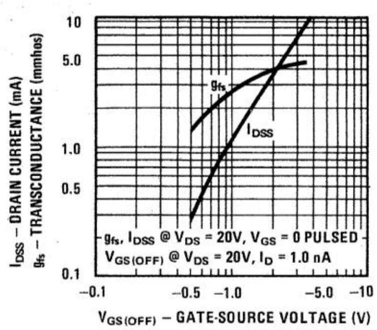
This process is available in the following device types.

*Denotes preferred parts.

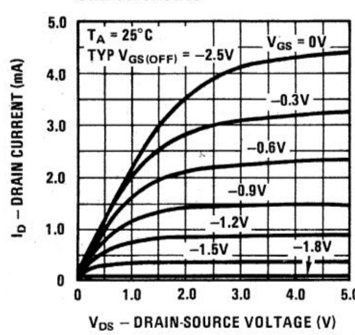
*NDF9406
*NDF9407
*NDF9408
*NDF9409
*NDF9410

NDF9401
NDF9402
NDF9403
NDF9404
NDF9405

Parameter Interactions

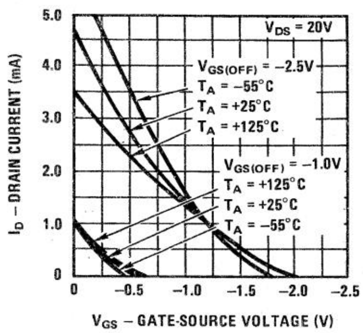


Common Drain-Source Characteristics

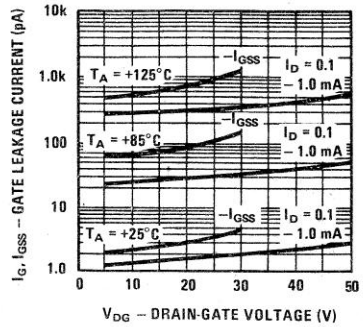


Process 94

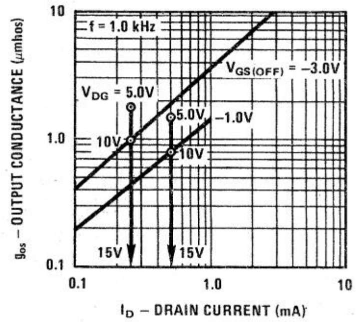
Transfer Characteristics



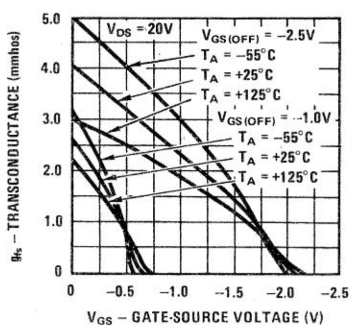
Leakage Current vs Voltage



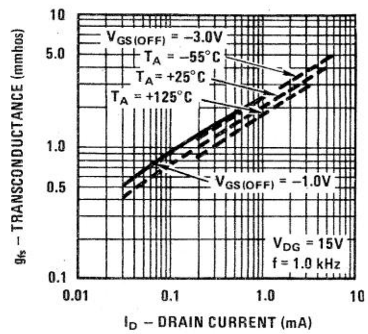
Output Conductance vs Drain Current



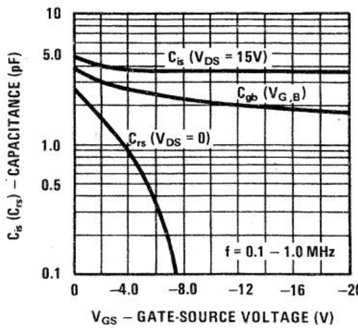
Transfer Characteristics



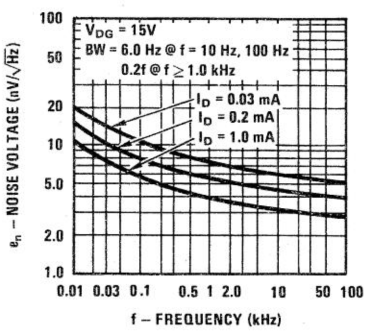
Transconductance vs Drain Current



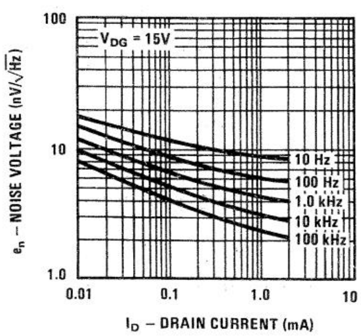
Capacitance vs Voltage



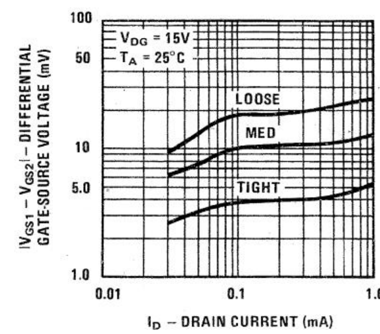
Noise Voltage vs Frequency



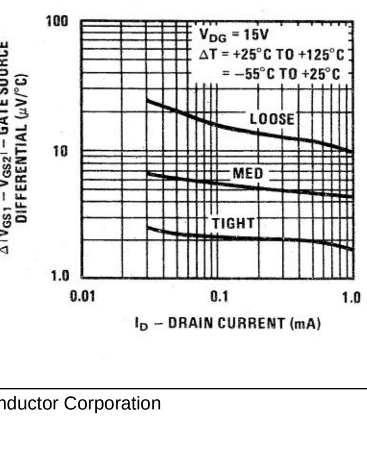
Noise Voltage vs Current



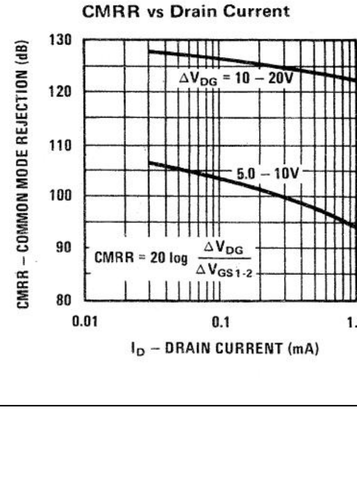
Differential Offset



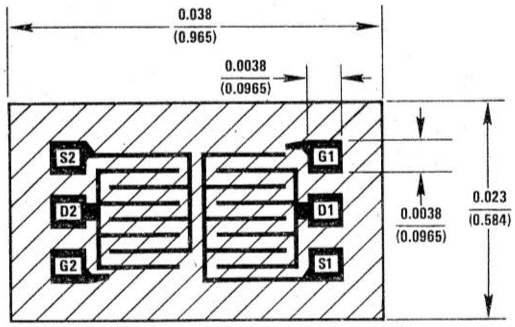
Differential Drift



CMRR vs Drain Current



Process 95 N-Channel JFET



DESCRIPTION

Process 95 is a monolithic dual JFET with a diode isolated substrate. It is intended for operational amplifier input buffer applications. Processing results in low input bias current and virtually unmeasureable offset current. Low noise voltage and high CMRR for critical I/f applications.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	$V_{DS} = 0V$, $I_G = -1\ \mu A$	−40	−70		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 15V$, $V_{GS} = 0$	0.5	3.0	8.0	mA
Forward Trans-conductance	g_{fs}	$V_{DS} = 15V$, $V_{GS} = 0$	1.0	2.5	4.0	mmhos
Forward Trans-conductance	g_{fs}	$V_{DG} = 15V$, $I_D = 0.2$ mA	0.5	0.7		mmhos
Gate Leakage	I_{GSS}	$V_{GS} = -20V$, $V_{DS} = 0$		−5.0	−100	pA
Pinch Off Voltage	$V_{GS(OFF)}$	$V_{DS} = 15V$, $I_D = 1$ nA	−0.5	−2.5	−4.0	V
Input Capacitance	C_{iss}	$V_{DS} = 15V$, $V_{GS} = 0$, f = 1 MHz		10	14	pF
Noise Voltage	e_n	$V_{DS} = 15V$, $I_D = 0.2$ mA, f = 10 Hz		8.0	30	$nV/\sqrt{Hz}$
Noise Voltage	e_n	$V_{DS} = 15V$, $I_D = 0.2$ mA, f = 100 Hz		6.0	10	$nV/\sqrt{Hz}$
Output Conductance	g_{os}	$V_{DG} = 15V$, $I_D = 0.2$ mA		0.3	1.0	µmhos
Feedback Capacitance	C_{rss}	$V_{DS} = 15V$, $V_{GS} = 0$, f = 1 MHz		3.5	5.0	pF
Differential Match	$\lvert V_{GS1}-V_{GS2}\rvert$	$V_{DG} = 20V$, $I_D = 0.2$ mA		6.0	25	mV
Differential Match	ΔV_{GS1-2}	$V_{DG} = 20V$, $I_D = 0.2$ mA		9.0	60	µV/°C
Common Mode Rejection	CMRR	$V_{DG} = 20V$, $I_D = 0.2$ mA	86	115		dB

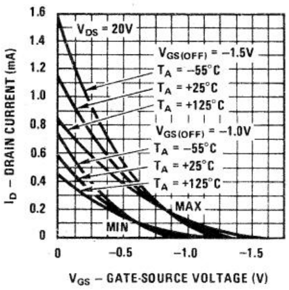
This process is available in the following device types.

2N5515	*2N5522
2N5516	*2N5523
2N5517	*2N5524
2N5518	*2N6483
2N5519	*2N6484
*2N5520	*2N6485
*2N5521	

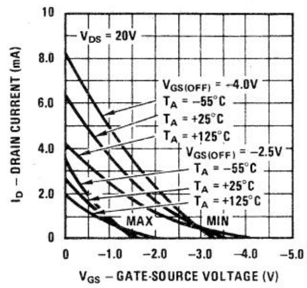
*Denotes preferred parts.

Process 95

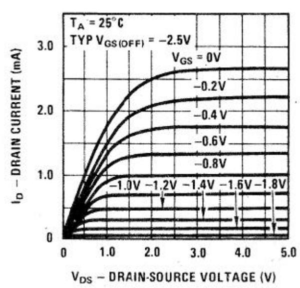
Transfer Characteristics



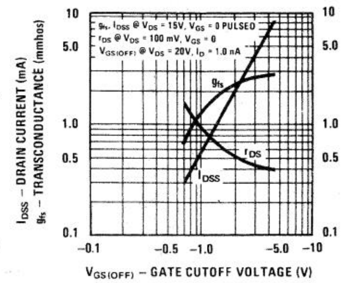
Transfer Characteristics



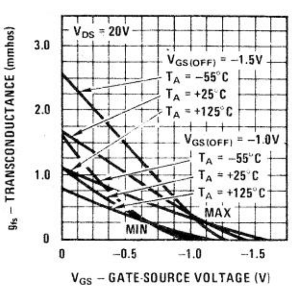
Common Drain-Source Characteristics



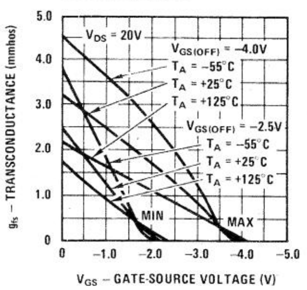
Parameter Interactions



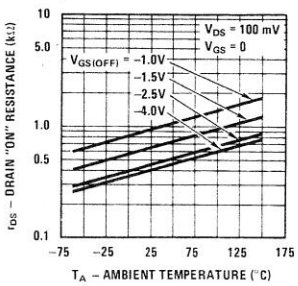
Transconductance Characteristics



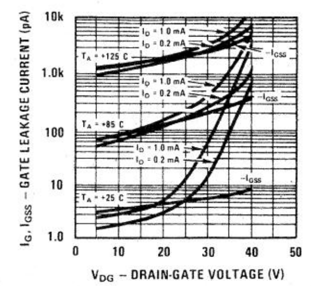
Transconductance Characteristics



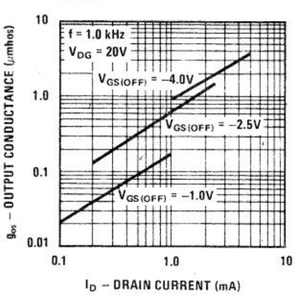
Channel Resistance vs Temperature



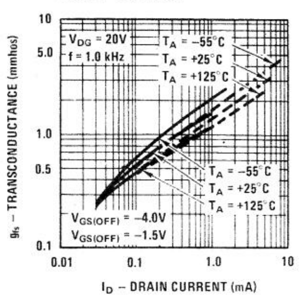
Leakage Current vs Voltage



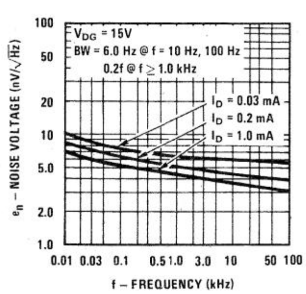
Output Conductance vs Drain Current



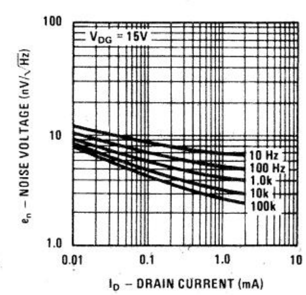
Transconductance vs Drain Current



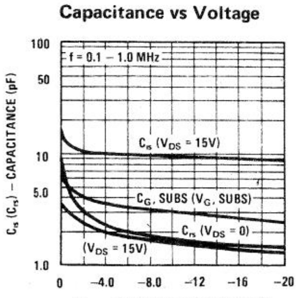
Noise Voltage vs Frequency



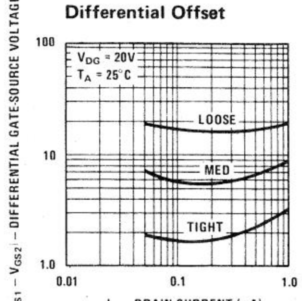
Noise Voltage vs Current



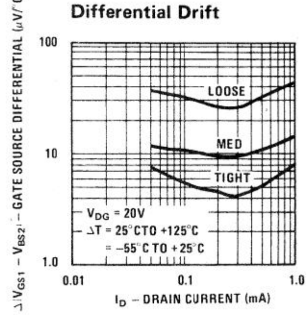
Capacitance vs Voltage



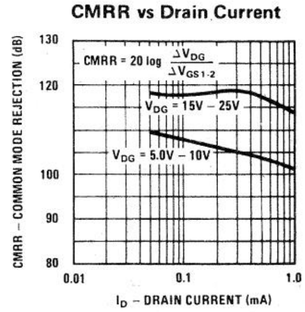
Differential Offset



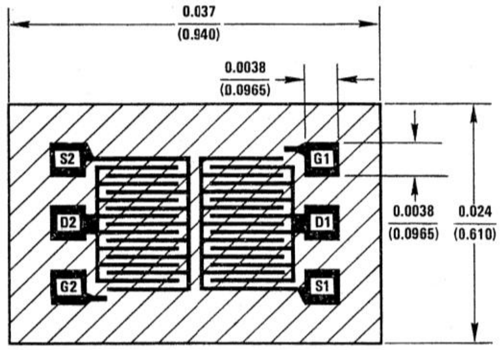
Differential Drift



CMRR vs Drain Current



Process 96 N-Channel JFET



DESCRIPTION

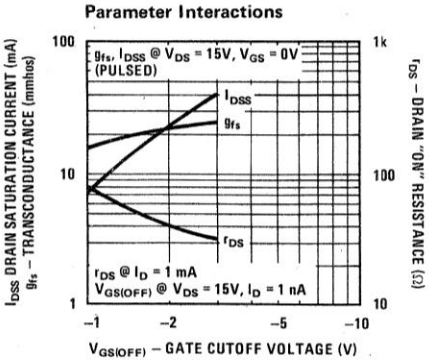
Process 96 is a monolithic dual JFET with a diode isolated substrate. It is intended for wide band, low noise, single ended video amplifier input stages. Also ideal for matched voltage variable resistor applications over 60 dB tracking range.

CHARACTERISTIC	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate-Source Breakdown Voltage	BV_{GSS}	V_{DS} = 0V, I_G = −1 μA	−40	−55		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 15V, V_{GS} = 0	5.0	15	30	mA
Forward Trans-conductance	g_{fs}	V_{DS} = 15V, V_{GS} = 0	9.0	18	30	mmhos
Forward Trans-conductance	g_{fs}	V_{DG} = 15V, I_D = 2 mA	7.5	9.0		mmhos
Output Conductance	g_{os}	V_{DG} = 15V, I_D = 2 mA		15	45	μmhos
Pinch Off Voltage	$V_{GS(OFF)}$	V_{DS} = 15V, I_D = 1 nA		−1.8	−3.0	V
"ON" Resistance	r_{DS}	V_{DS} = 100 mV, V_{GS} = 0	35	70	120	Ω
Gate Current	I_{GSS}	V_{GS} = −20V, V_{DS} = 0		−8.0	−100	pA
Gate Current	I_G	V_{DG} = 15V, I_D = 2 mA		15	200	pA
Noise Voltage	e_n	V_{DG} = 15V, I_D = 2 mA, f = 100 Hz		4.5	10	$nV/\sqrt{Hz}$
Feedback Capacitance	C_{rs}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		2.5	3.0	pF
Input Capacitance	C_{is}	V_{DG} = 15V, I_D = 2 mA, f = 1 MHz		10	12	pF
Differential Voltage	$\|V_{GS1}-V_{GS2}\|$	V_{DG} = 15V, I_D = 2 mA		8.0	25	mV
Differential Voltage	ΔV_{GS}	V_{DG} = 15V, I_D = 2 mA		9.0	50	μV/°C
Common Mode Rejection	CMRR	V_{DG} = 15V, I_D = 2 mA	76	95		dB

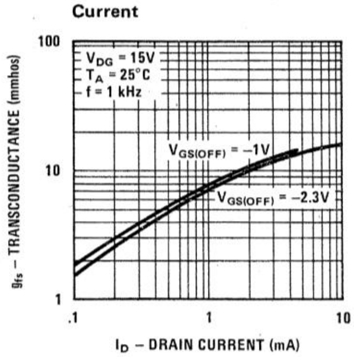
This process is available in the following device types. *Denotes preferred parts.

*2N5564 *NPD5564
*2N5565 *NPD5565
*2N5566 *NPD5566

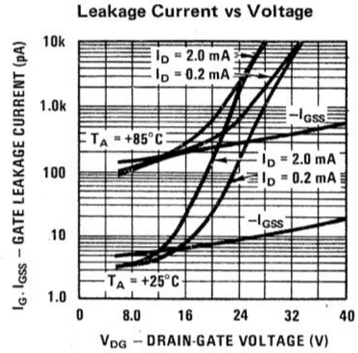
Parameter Interactions



Transconductance vs Drain Current

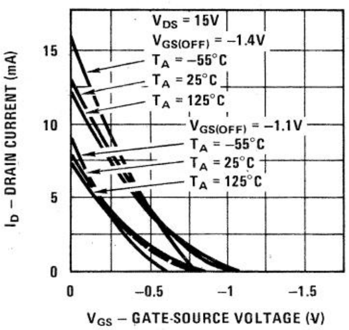


Leakage Current vs Voltage

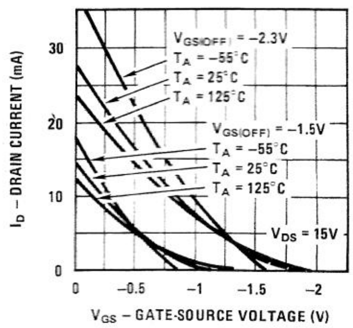


Process 96

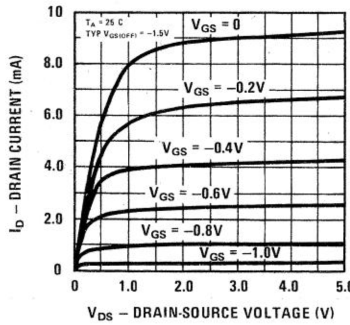
Transfer Characteristics



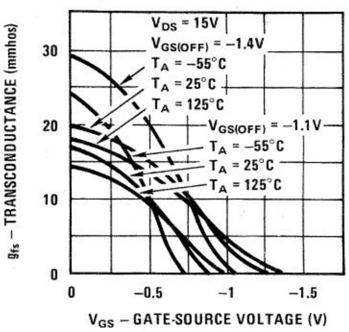
Transfer Characteristics



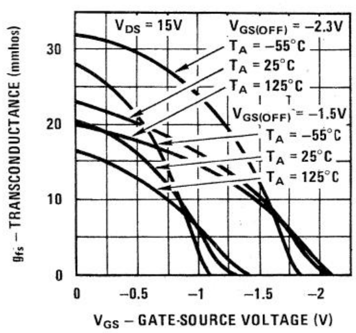
Common Drain-Source Characteristics



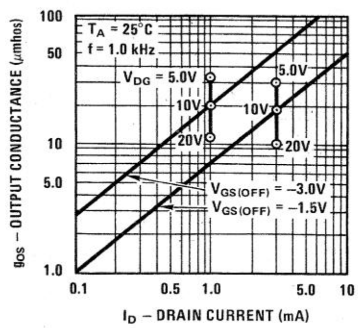
Transfer Characteristics



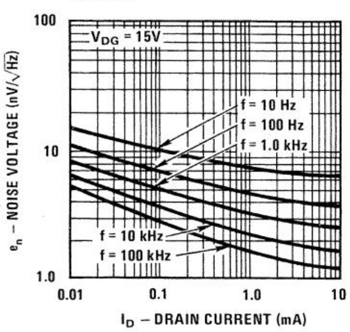
Transfer Characteristics



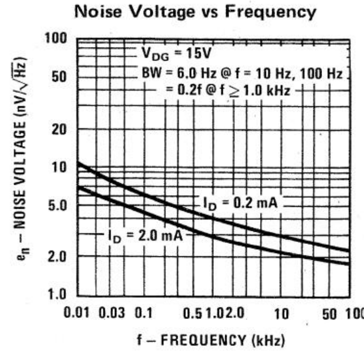
Output Conductance vs Drain Current



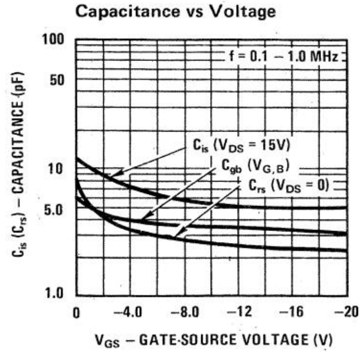
Noise Voltage vs Current



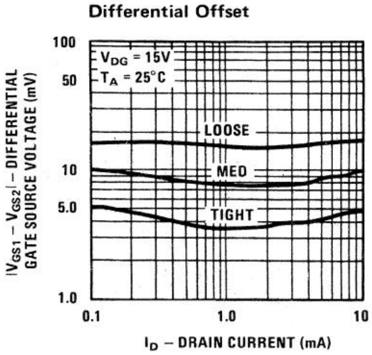
Noise Voltage vs Frequency



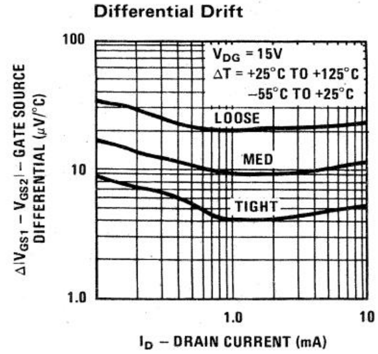
Capacitance vs Voltage



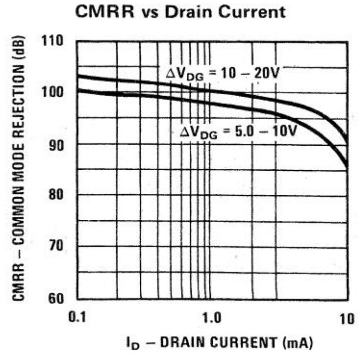
Differential Offset



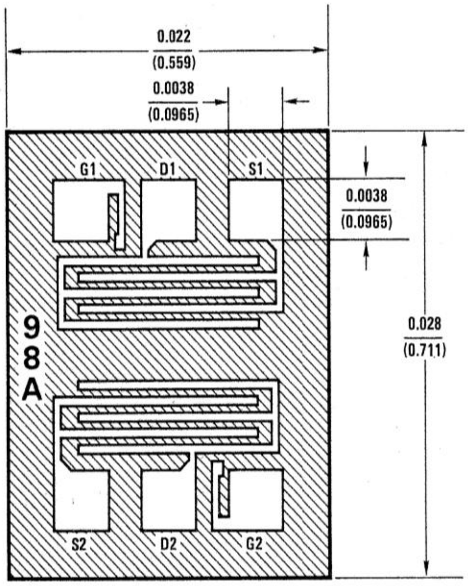
Differential Drift



CMRR vs Drain Current



Process 98 N-Channel JFET



DESCRIPTION

Process 98 is a high gain, general purpose, monolithic dual JFET with a diode isolated substrate. It is intended for amplifier input stages requiring high gain, low noise and low offset drift over temperature. Strict processing controls result in low input bias currents and virtually immeasurable offset currents. Matching characteristics are essentially independent of operating current and voltage.

This process is available in the following device types.

*Denotes preferred parts.

2N5561	J401
2N5562	J402
2N5563	J403
U401	J404
U402	J405
U403	J406
U404	
U405	
U406	

References

[1] 1977 JFET DATABOOK, National Semiconductor

Editor: *Richard Dunipace, June 2015.*

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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