ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

AN-6603

A Linear Gain Controlled Amplifier

Introduction

A linear control function over three decades of gain can be achieved with a JFET in the feedback path of a non inverting amplifier. Besides the ultimate simplicity of the circuit, multiple tracking gain control circuits can be constructed with dual op amps and monolithic dual JFET's or quad op amps and monolithic quad JFET's. Such circuits could even be integrated with ion-implanted JFET's on single or multiple monolithic op amp chips. The gain control range may be designed for less than 2 to 1 or higher than 1000:1, but input voltage levels are limited by acceptable levels of distortion. Bandwidth is dependent on maximum gain and unity gain bandwidth of the op amp used. The gain control circuit is especially suitable for volume expansion applications.

Gain Control with JFETS

The JFET has long been used as a Voltage Controlled Resistor (VCR), often as the shunt arm in the series-shunt attenuator of Figure 1. Advantages of the JFET as a VCR are that:

1. The control signal is almost perfectly isolated from the controlled signal path, and

2. The resistance can be made to vary over an almost infinite max./min. ratio.

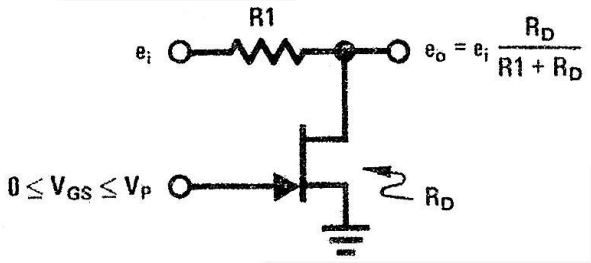


Figure 1. Voltage Controlled JFET Attenuator

Disadvantages are that:

1. The JFET behaves as a linear resistance only for small values of source-drain voltage V_{DS}.

2. Non-linearity (of resistance) increases as the control voltage V_{GS} approaches cut-off voltage V_P when the resistance is maximum.

3. The relationship of resistance r_d to V_{GS} is reciprocal rather than direct linear,

4. VCR multiples with matched resistance characteristics over their full control range have been extremely difficult to obtain at any kind of reasonable price, and

5. Production spread in V_P requires separate bias set and gain set on each circuit.

Examination of the JFET drain characteristics in Figure 2 through Figure 5 reveal the essential non-linearity of r_d at high signal levels, especially as V_{GS} approaches V_P. This non-linear region must be avoided in order to achieve tolerable distortion levels. One obvious way is to limit V_{DS} to small values when r_d is high as suggested by Figure 4 and Figure 5 another is to utilize JFET's with high V_P as suggested by reference to Figure 3 and Figure 5 .

The reciprocal relationship of r_d and V_{GS} is an advantage, as it is precisely that which allows the linear control of gain in the circuit to be described. The availability of matched monolithic dual JFET's such as the 2N3958 (watch out for the matched pairs as their resistance match close to V_P may not be as good as that of the monolithic versions) make available low cost duals with very closely matched resistance characteristics over the full control range. There are even some monolithic quads available. The final problem of the production range of V_P can be much improved with ion-implant diffusion techniques whereby lot variation in V_P may be held to within a few tenths of one volt.

The gain control circuit is that of an ordinary non-inverting op amp with feedback. The usual circuit is modified in Figure 6 to include a JFET as a controlled resistor. The gain function is normal except that r_d replaces R2 in the usual form.

$$A_V = 1 + \frac{R1}{r_d} \quad (1)$$

Now r_d can be equated to a control voltage V_C as follows:

$$r_d = r_o \frac{V_P}{V_P - V_{GS}} \quad (2)$$

where:

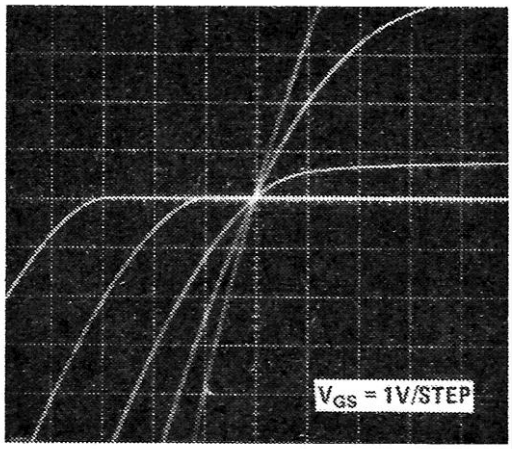
$$r_O = r_d \mid V_{GS} = 0 \quad (3)$$

where

$$V_C = V_P - V_{GS} \quad (4)$$

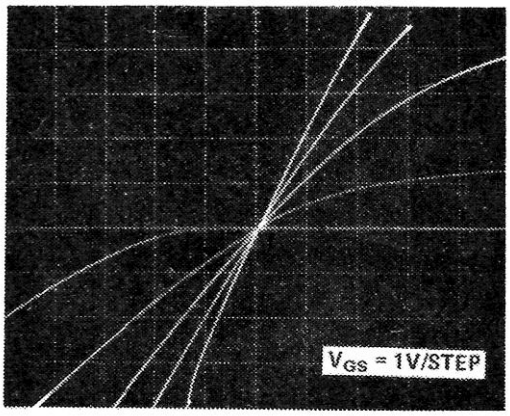
The gain function is thus seen to be linear with V_C.

$$A_V = 1 + \frac{R1}{r_O}\frac{V_C}{V_P} \quad (5)$$



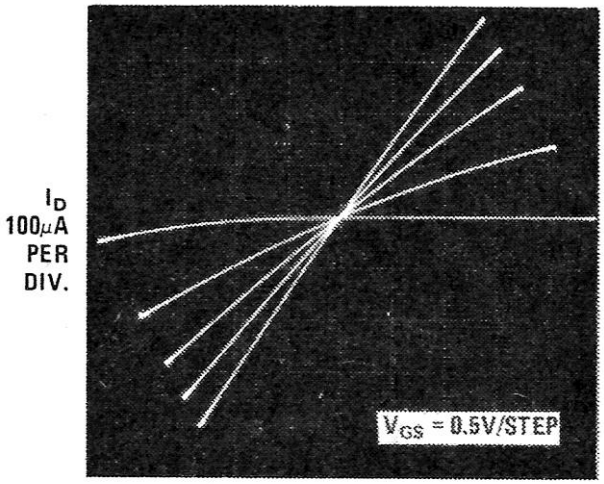
V_{DS} = 0.5V/DIV.

Figure 2. V_P=2.8 V



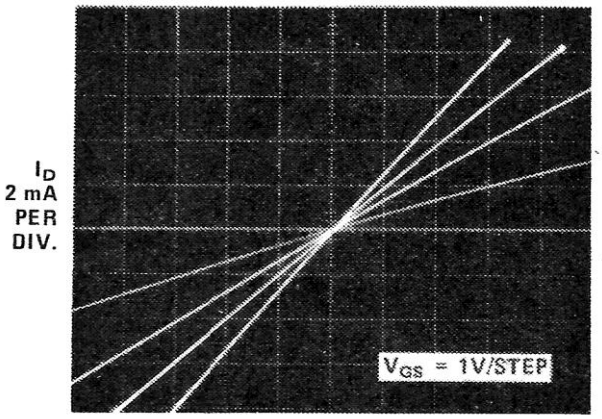
V_{DS} = 0.5V/DIV.

Figure 3. V_P=9 V



V_{DS} = 50 mV/DIV.

Figure 4. V_P=2.8 V



V_{DS} = 50 mV/DIV.

Figure 5. V_P=9 V

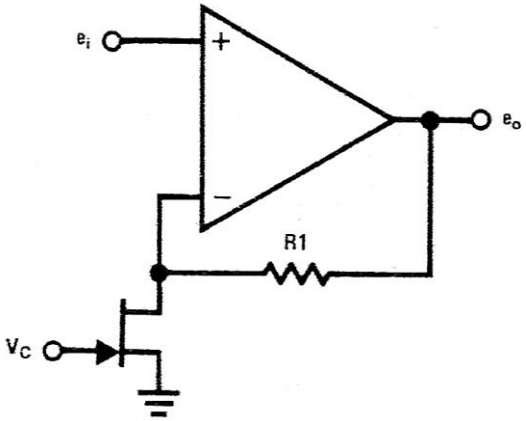


Figure 6. A_{VMIN}=1

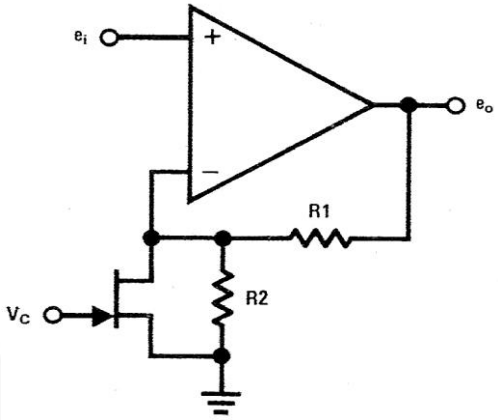


Figure 7. A_{VMIN} >1

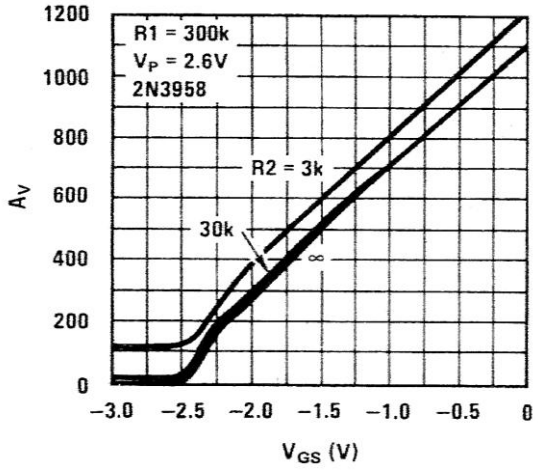


Figure 8. Gain vs. Control Voltage for Short Channel JFET

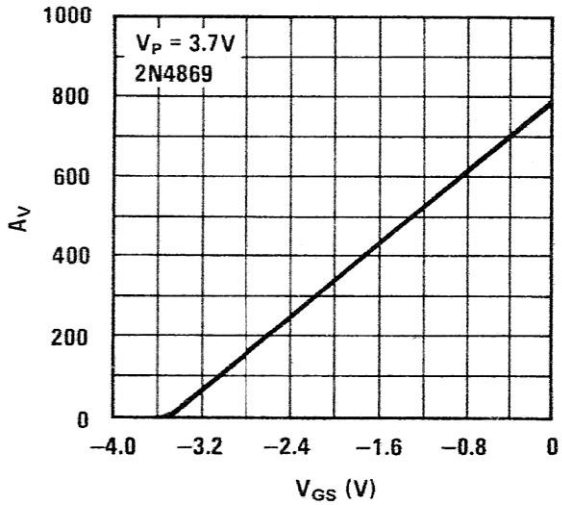


Figure 9. Gain vs. Control Voltage for Long-Channel JFET

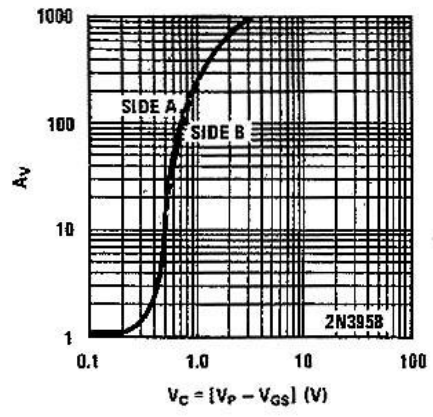


Figure 10. Control-Gain Match for Dual JFET

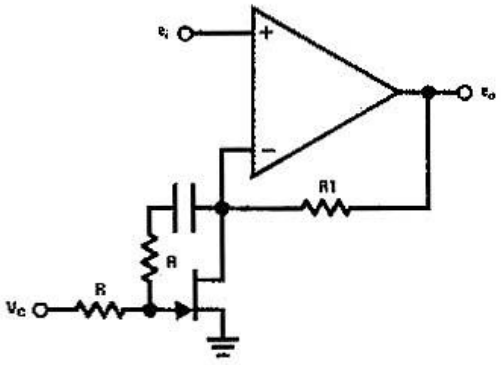


Figure 11. $\frac{V_{DS}}{2}$ Feedback to Gate

At $V_C = 0$, the gain reduces to unity; and at $V_C = V_P$, the gain increases to $1 + R1/r_o$ which may be as high as 1000 or so. If it is desired to limit the minimum gain to some value greater than unity, another resistor R2 may be added as in Figure 7. Then the gain equation becomes:

$$A_V = 1 + \frac{\frac{R1}{R2\ r_O\ (V_P/V_C)}}{R2 + r_o(V_P/V_C)} = \frac{1 + [R2 + r_o\ (V_P\ /\ V_C)]}{R2\ r_o(V_P/V_C)} \qquad (6)$$

$$A_V = 1 + \frac{R1}{R2} + \frac{R1\ V_C}{r_o V_P}$$

In either case, the gain function is linear with V_C.

The circuits of Figure 6 and Figure 7 do indeed show a linear gain versus control voltage as plotted in Figure 8 for several values of minimum gain. There is some non-linearity near minimum gain which appears in all curves. This is certainly due to a non-ideal characteristic of the JFET caused by finite contact and bulk resistance at source and drain. Figure 9 shows a similar control curve for a JFET with longer channel in which the controlled channel resistance is a greater part of the total resistance than that of the short channel device of Figure 8. For those applications requiring a more precisely linear control of gain, the long channel devices are preferred.

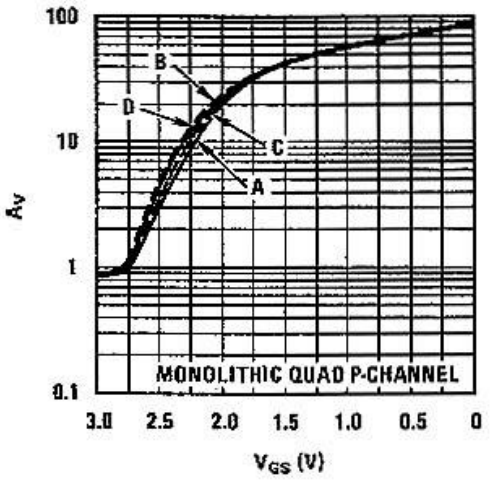


Figure 12. Monolithic Quad Gain Control Tracking

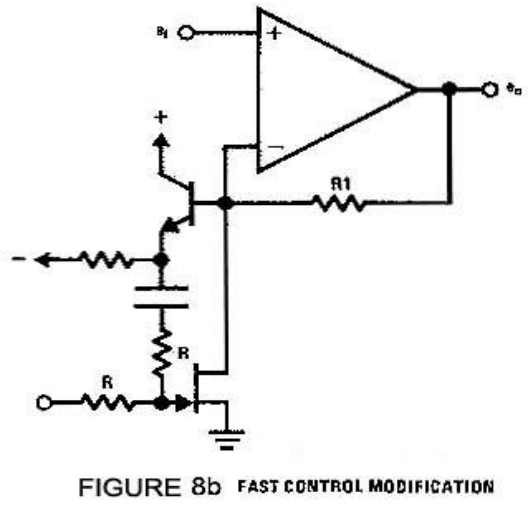


Figure 13. Fast Control Modification

Several variable-gain circuits can be made to track when monolithic multiple JFET's are used as the control elements with matched feedback resistors. A monolithic JFET dual (NSC 2N3958) used in two identical control circuits shows remarkable tracking over the entire control range, even when V_{gs} is near V_p where variations would be expected to be most apparent. The plots appear in Figure 10. Similar performance for a quad gain control using a monolithic P-channel quad JFET (AM97C09 or AM9709) is shown in Figure 12.

Distortion

Figure 2 through Figure 5 show that the JFET acts as a linear resistance only for a relatively small value of drain-source voltage, in either polarity. This is particularly apparent for positive V_{DS} (for N-channel JFET) and V_{GS} approaching V_P. The difference between Figure 4 and Figure 5 indicates that the maximum allowed applied signal is greater for high V_P as compared with low V_P.

It is possible to improve the linearity characteristics somewhat by applying a part of the V_{DS} in series with the control voltage applied as V_{GS}. The circuits to accomplish this are shown in Figure 11 and Figure 13. It happens that about half of V_{DS} applied to the gate provides the greatest improvement for small signals. The addition of two resistors and one capacitor as in Figure 11 is all that is required. The capacitor simply blocks the control voltage from the JFET drain and the op amp input. Figure 13 shows the addition of an emitter follower to prevent abrupt changes in V_c from coupling to the op amp. Figure 14 and Figure 15 show the improved linearity of the drain characteristics as compared to Figure 2 through Figure 5. The improvement is also seen in the distortion versus input signal plots of Figure 16,Figure 17,Figure 20,Figure 21. Note that the distortion at any value of V_c is primarily a function of input signal (which equals the feedback signal applied to the JFET drain at the inverting input). Some modification is made to this direct relationship if an R2 is shunted across the JFET as in Figure 7, Measured distortion at low signal level is the result of noise rather than of signal distortion. Maximum gain is limited to about 100 in these plots so as to avoid the region of lower S/N. The noise is that of the op amp input stage and the signal source resistance plus the contribution of the JFET which is essentially the thermal noise of r_d.

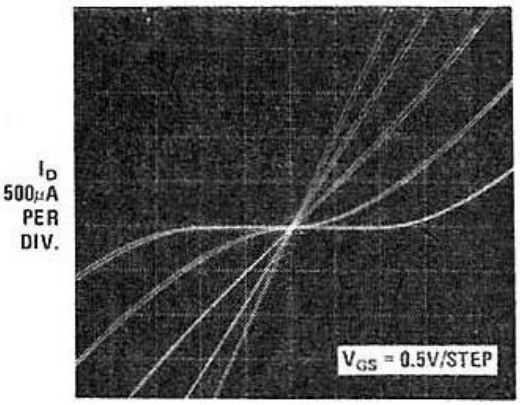


Figure 14. V_P=2.8 V

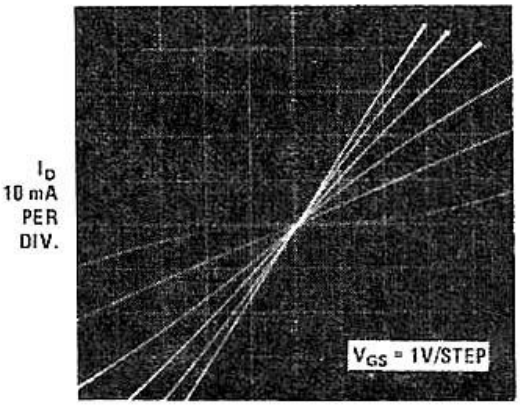


Figure 15. V_P=9 V

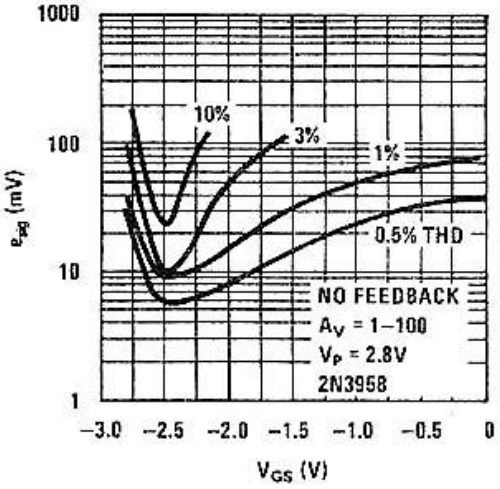


Figure 16. Distortion with V_p= 2.8 V

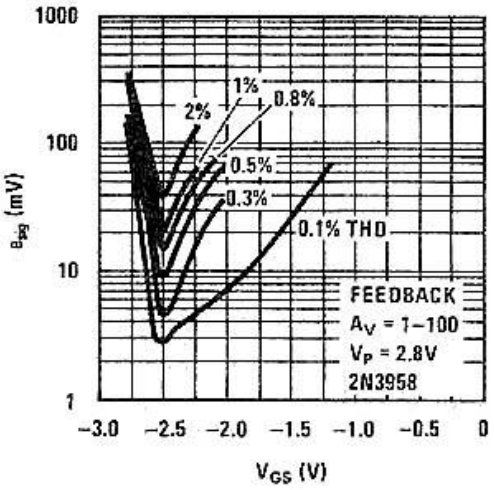


Figure 17. Distortion with V_p= 2.8 V with Linearization

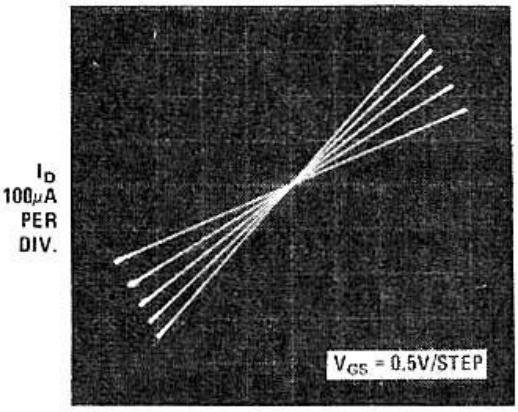


Figure 18. V_P=2.8 V

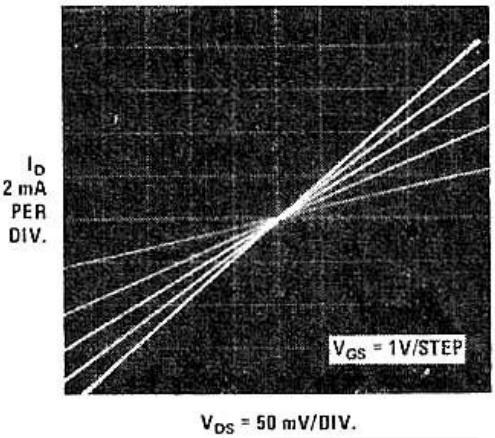


Figure 19. V_P=9 V

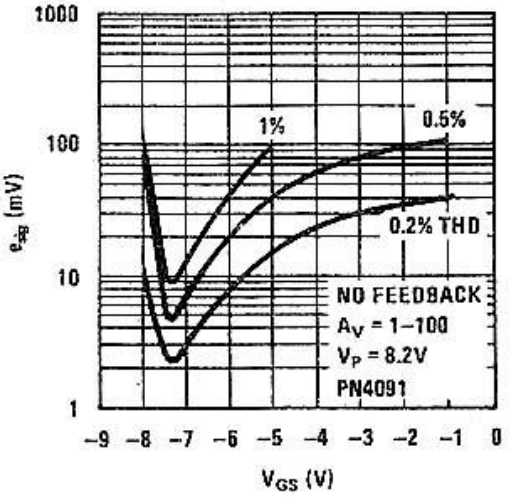


Figure 20. Distortion with V_p=8.2 V

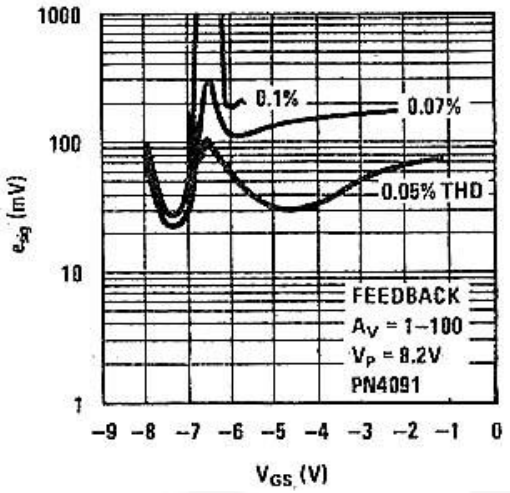


Figure 21. Distortion with V_p=8.2 V, Linearized

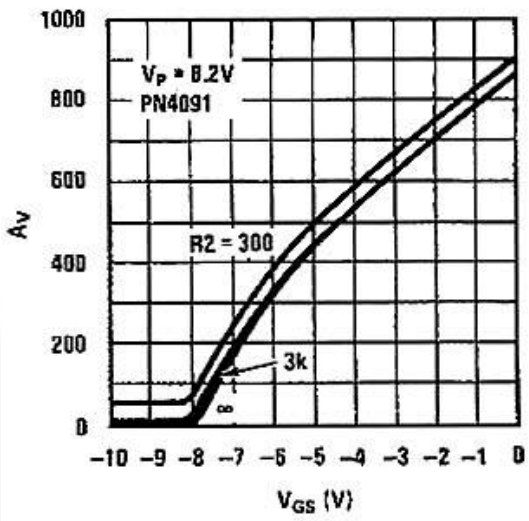


Figure 22. Gain for Circuit Figure 23

Bandwidth and Control Time Constant

The circuit bandwidth is the closed loop bandwidth of the op amp used at the (instantaneous) set gain. The gain control time constant is that of the input circuit to the JFET (dependent on the value of R in Figure 13) limited by the slew rate of the op amp. The JFET itself reacts practically instantly, producing a step change in feedback ratio. Control time constant is thus a few microseconds at most.

Applications

Three obvious applications present themselves; they are:

1. Remote or multichannel gain control

2. Volume expansion

3. Volume compression/limiting

To this short list might be added a number of others, including applications in noise reduction and quad sound techniques.

The gain-controlled amplifier of Figure 23 has a gain range of 1-1000, a maximum output level of 8.5 Vrms, and a bandwidth of better than 20 kHz at maximum gain. The JFET used has high V_p for maximum freedom from distortion. Figure 22 and Figure 24 show the gain function and constant distortion contour lines. Note that the gain control curve is non-linear near unity gain because the PN4091 is a short channel JFET.

Distortion is quite low except as limited by maximum output voltage. Note that the maximum e_{in} is restricted by output saturation. The LM318 is used in the example only to achieve wideband response at maximum gain. The amplifier input voltage must be restricted to about 8 mVrms at maximum gain when the S/N is about 60 dB over a 10 kHz bandwidth.

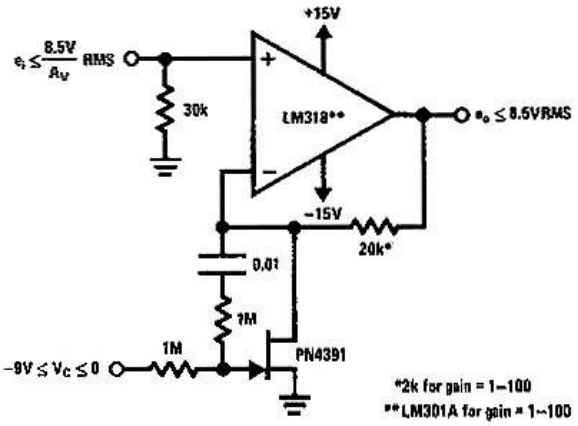


Figure 23. Amplifier with Gain Range= 1--1000

A more practical circuit might employ a gain range of 1--100. Then the amplifier could be a LM301A and still achieve a 10 kHz bandpass at maximum gain. The input signal could, accordingly, be increased to 80 mVrms for a S/N of 80 dB. This performance can he extended to dual and quad control circuits with tracking gain functions, but watches the bandwidth as required at maximum gain. Any of the several dual op amps could be used with the 2N3958 (monolithic dual), or the LM324 quad op amp can be used in limited gain times bandwidth applications with a quad monolithic JFET. Figure 26 shows all details of an ac coupled tracking quad gain control with 40 dB range. Gain varies over 1--100 range, bandwidth is 10 kHz minimum, S/N is better than 70 dB with 4.3 Vrms maximum output. Figure 12 shows the gain curve and matching characteristics.

Noise considerations could be important in this method of gain control, as the signal is amplified rather than attenuated. To realize the function of a 40 dB variable attenuator, it is necessary to install a fixed attenuator at the amplifier input and perhaps also at the output. This will reduce the minimum signal level to milli-volts, thus a low noise amplifier is desirable. The LM381 dual low-noise ac coupled amplifier could be used in a 40 dB audio attenuator to realize S/N about 100 dB or in a 60 dB attenuator to realize 80 dB S/N. Improvements in S/N can be made by reducing system bandwidth in fixed or low frequency operation. Minimum noise is also achieved by using the minimum practical amplifier source resistance. Values as low as 1 kΩ are advantageous.

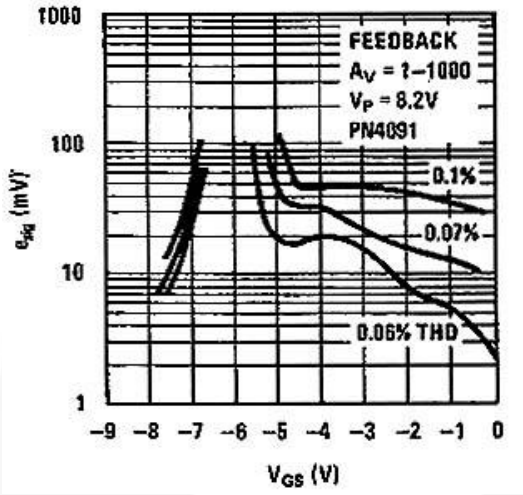


Figure 24. Distortion for Circuit of Figure 23

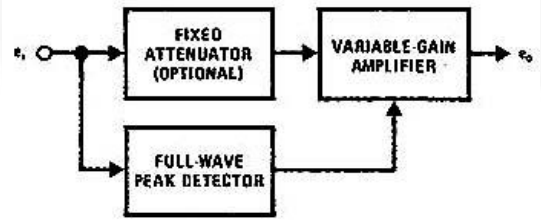


Figure 25. Volume Expander/Compressor Block Diagram

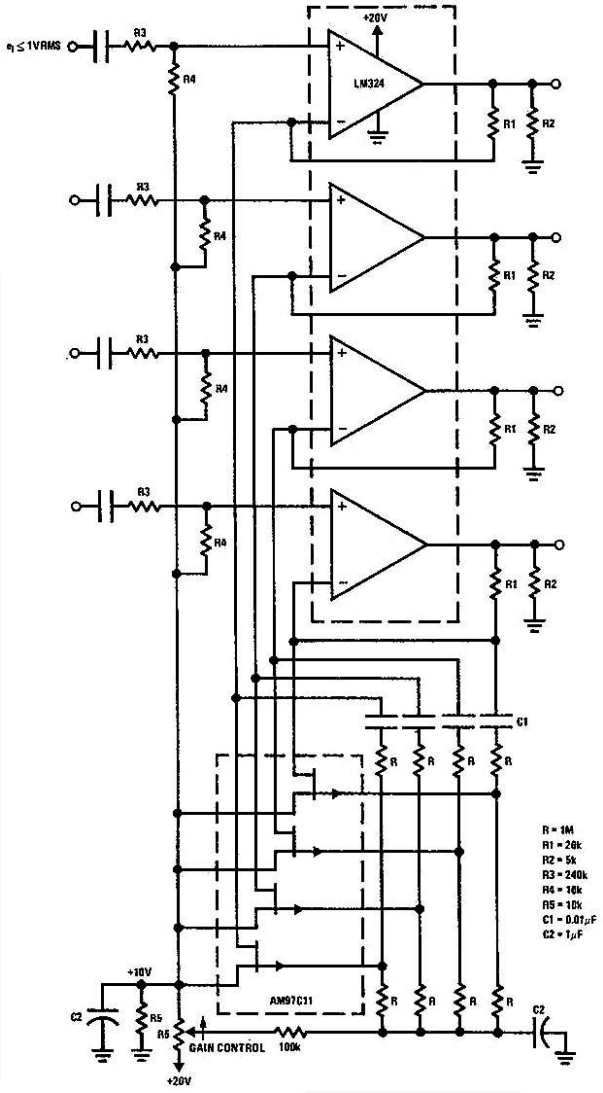


Figure 26. Quad Gain Control

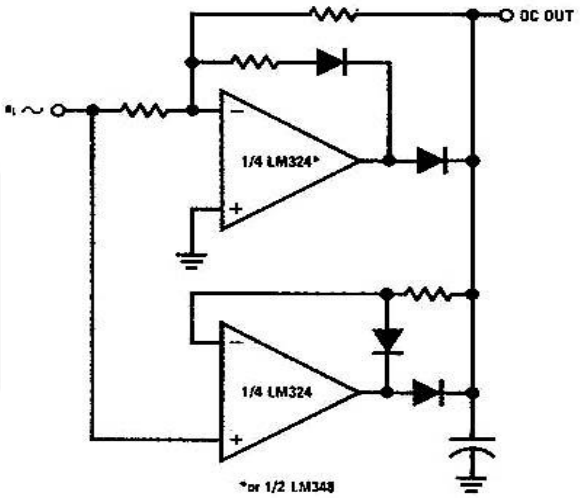


Figure 27. Full-Wave Linear Precision Peak Detector

The effect of temperature will be to change the gain according to the temperature sensitivity of the JFET. This effect can be reduced by using a silicon resistor for the feedback resistor, R1. If the JFET were to be integrated onto the op amp chip, an attempt should be made to include R1 on the chip as well.

The application to a volume expander circuit is of interest as the control is linear, the required control range is only about 1:4, and the input signal is small for the low gain condition when distortion would other-wise be most apparent. The elements of a volume expander are indicated in Figure 25. The gain controlled amplifier need only exhibit a 12 dB variation in gain, being lowest for small signals. The slope of gain versus control should be linear, more specifically the slope of (log) gain in dB versus (log) signal in dB should be linear. A practical range is 12 dB gain change over a 30 dB input signal range. The peak detector should be linear down to very small signals, exhibit a fast attack or charge time of a millisecond or less, a discharge time constant of about 2 seconds, and operate on the first half cycle (full-wave detector). The detector should, therefore, be a full-wave precision linear peak detector with low internal impedance; the requirements can be met with the circuit of Figure 26.

The expander circuit shown in Figure 28 will perform as desired. The gain control function is plotted in Figure 29; distortion is below 0.1% at all levels. Resistors R3 and R4 are added in order to modify the linear control curve to the desired log curve. Note that the input signal is attenuated prior to amplification in order to reduce distortion and maintain an overall gain of approximately 0 dB at midrange of expansion. The noise with the LM124 over a 20 kHz bandwidth is, of course, a function of signal; but the maximum signal to noise ratio is 80 dB. The circuit could be adapted to stereo or quad sound as in Figure 30-Figure 32. Questions for individual design concern the method of control. Whether to expand all channels together, and whether to derive the control signals individually from each channel, a summation from 2 to 4 channels, or from a single channel (assuming that high level from any channel indicates high levels from all channels). Note that the JFET is biased OFF (minimum gain) for low signals, and increasing signals progressively bias the JFET ON (maximum gain).

The volume compression circuit is a logical mate to the expander. The only difference would be that the JFET is initially biased ON (maximum gain) for low signals, and increasing signals progressively bias the JFET OFF (minimum gain). A disadvantage is that the circuit produces greatest distortion in the low gain condition when signals are highest. Maximum S/N is degraded by 24 dB over that of the expander, minimum S/N is the same.

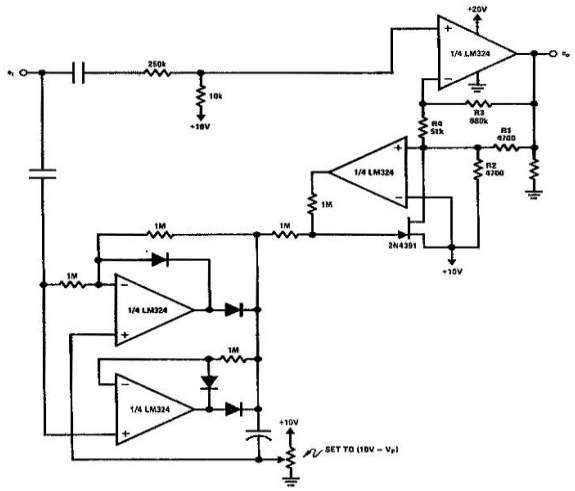


Figure 28. Volume Expander Circuit

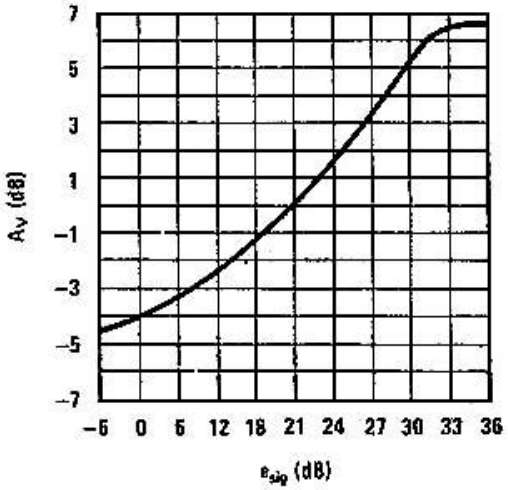


Figure 29. Expander Gain Characteristics

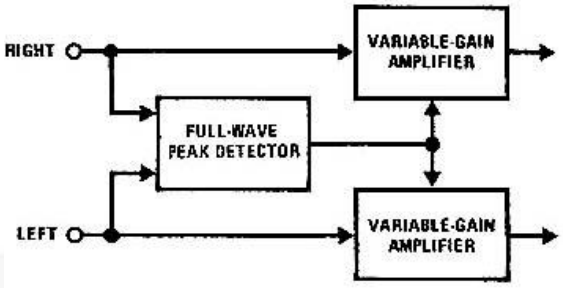


Figure 30. Stereo Expander Block

Conclusion

The combination of JFET and op amp provides a linear dc (voltage) control of gain over a range to 60 dB. As the circuit realizes positive gain, rather than being a controlled attenuator, the input signal is limited. Input signal is further limited to several hundred milli-volts by the non-linearity of the JFET (which sees the full input signal). Because input signals are generally in the 10-300 mV range, noise performance of the selected op amp is important. Even so, S/N of 60-100 dB is obtainable with standard amplifiers. Tracking pair or quad gain-control amplifiers are realizable with existing monolithic dual or quad JFET's, and the combination of JFET and op amp lends itself to simple integration. The circuit is well-suited to remote and multiple linear gain control and to volume expander/compressors. The volume expander is especially interesting as the signal level and gain conditions result in extremely low distortion and more than adequate signal-to-noise ratio.

Author: Jim Sherwin, August 1975, Note 129

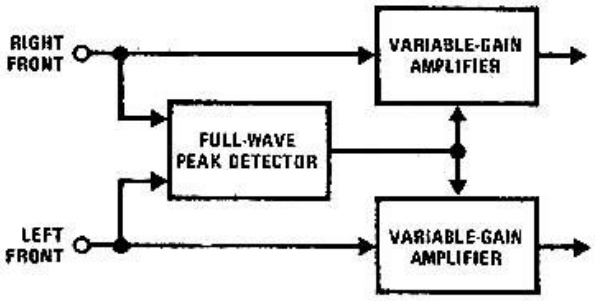


Figure 31. Four-Channel Expander Block

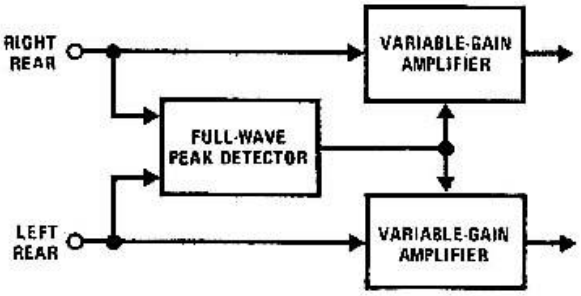


Figure 32. Four-Channel Expander Block

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative