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AN-6224

Applying FAN6224 for Flyback and Forward Freewheeling Rectification

Introduction

FAN6224 is a secondary-side Synchronous Rectification (SR) controller to drive MOSFETs for improved efficiency. It is suitable for Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Quasi-Resonant (QR) flyback converters. It can be applied on both low-side and high-side rectification, as shown in Figure 1 and Figure 2. It can also be applied on forward or dual-forward free-wheeling rectification, as shown in Figure 3.

The SR MOSFET turn-off timing is determined by linear-predict timing control and the operating principle is based on voltage-second balance theorem. This control algorithm is implemented by detection of secondary-side winding voltage and output voltage, as shown in Figure 1. The method avoids sense-resistor usage, which improves the efficiency. In addition, it is independent from the turn-on resistance of the MOSFET and, therefore, increases the flexibility of MOSFET selection.

To drive the SR MOSFET, the reference ground of the SR controller must be connected to the source terminal of MOSFET. For low-side application, the reference ground is the same as output ground. For high-side application, the reference ground is floating. Since the output ground doesn’t contain switching devices for high-side application, the EMI performance is better than in low-side application.

FAN6224 can operate in both fixed-frequency and variable-frequency systems; the maximum operating frequency is up to 140 kHz.

To improve no-load and light-load efficiency, a Green Mode is utilized. In Green Mode, the FAN6224 stops switching to reduce the operating current and save switching losses. To increase design flexibility, the loading level to trigger Green Mode is adjustable by the external resistor of the RP pin.

This application note describes the design procedure for using FAN6224 for flyback and forward free-wheeling rectification; provides a design example of flyback high-side rectification is shown; explains troubleshooting; and supplies printed circuit board layout guidelines.

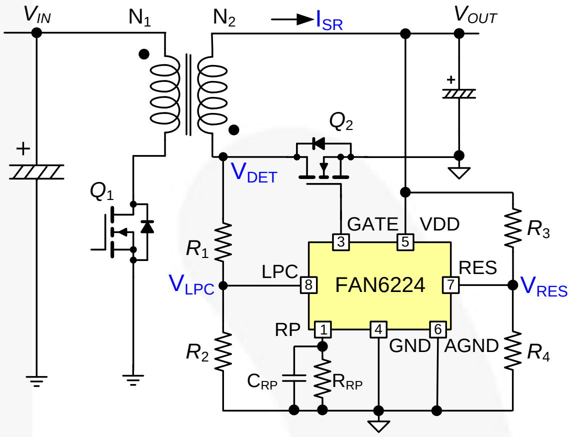

Figure 1. Typical Application Circuit for Low-Side Flyback Converter

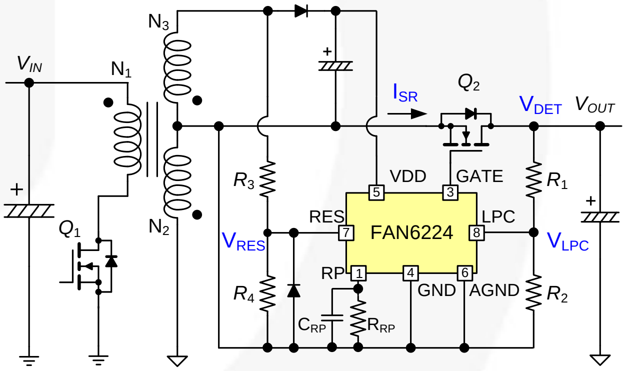

Figure 2. Typical Application Circuit for High-Side Flyback Converter

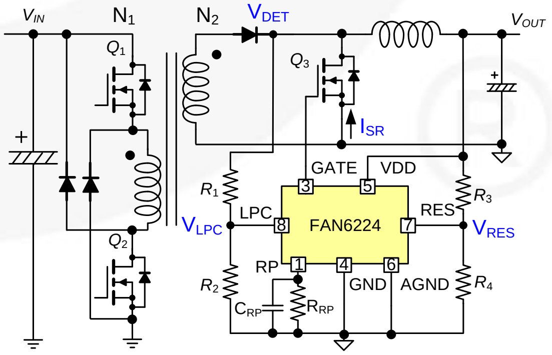

Figure 3. Typical Application Circuit for Dual-Switch Forward Free-Wheeling Rectification

External Components Design

IC Power Supply

For low-side applications, the output (V_{OUT}) can supply power for the FAN6224. As shown in Figure 1, the V_{DD} pin is connected to V_{OUT} directly. The V_{DD} operating range is between 11.5 V and 26 V. If the rated output voltage is out of this range or the FAN6224 is used for high-side application, an auxiliary winding (N_3) is required to supply power for the FAN6224. The auxiliary winding reflects V_{OUT}, so V_{DD} is derived as:

$$V_{DD} = \frac{N_3}{N_2} \cdot V_{OUT} \tag{1}$$

Therefore, N_3 and N_2 must be well-designed to satisfy the operating range of V_{DD}.

Selection of Operating Frequency

The FAN6224 can be applied in different operating frequency ranges. The capacitor of the RP pin (C_{RP}) fits the controller into the proper range of operating frequency. For low-frequency systems (under 100 kHz), C_{RP} is recommended as 10 nF. For high-frequency systems (100 kHz to 140 kHz), C_{RP} is recommended as 1 nF.

Flyback Low-Side Rectification

As Figure 1 shows, the resistors of the LPC and RES pins need to be designed appropriately for linear-predict timing control. When designing the four resistors, begin with the LPC part. First, determine the proper LPC operating range by selecting the ratio of LPC resistors ($Ratio_{LPC}$). Then choose the proper resistance of R_1 and R_2 according to $Ratio_{LPC}$. Next, select the voltage scaled-down ratio (K). Then the ratio of the RES resistors ($Ratio_{RES}$) can be obtained. Finally, R_3 and R_4 are determined based on $Ratio_{RES}$ and the design is complete.

The timing diagram for low-side application is shown in Figure 4. When LPC voltage (V_{LPC}) is higher than $V_{LPC\text{-}EN}$ (87.5% of $V_{LPC\text{-}HIGH}$) over a blanking time ($t_{LPC\text{-}EN}$); the SR gate is ready to output. After the LPC voltage drops below $V_{LPC\text{-}TH\text{-}HIGH}$ (1.22 V), the SR controller sends out gate signals. Based on the control algorithm, $V_{LPC\text{-}EN}$ must be higher than $V_{LPC\text{-}TH\text{-}HIGH}$ or the SR MOSFET cannot be turned on; therefore:

$$0.875 \cdot V_{LPC-HIGH} > 1.22 \tag{2}$$

Considering the tolerance,

$$V_{LPC-HIGH} > 1.54 \tag{3}$$

Define the turn-ratio between N_1 and N_2 as;

$$n_1 = \frac{N_1}{N_2} \tag{4}$$

Define the ratio of LPC resistors as:

$$Ratio_{LPC} = \frac{R_1 + R_2}{R_2} \tag{5}$$

Considering the minimum input voltage ($V_{IN.MIN}$) and the turn-ratio, (3) can be rewritten as:

$$\frac{1}{Ratio_{LPC}} \cdot \left(\frac{V_{IN.MIN}}{n_1} + V_{OUT} \right) > 1.54 \tag{6}$$

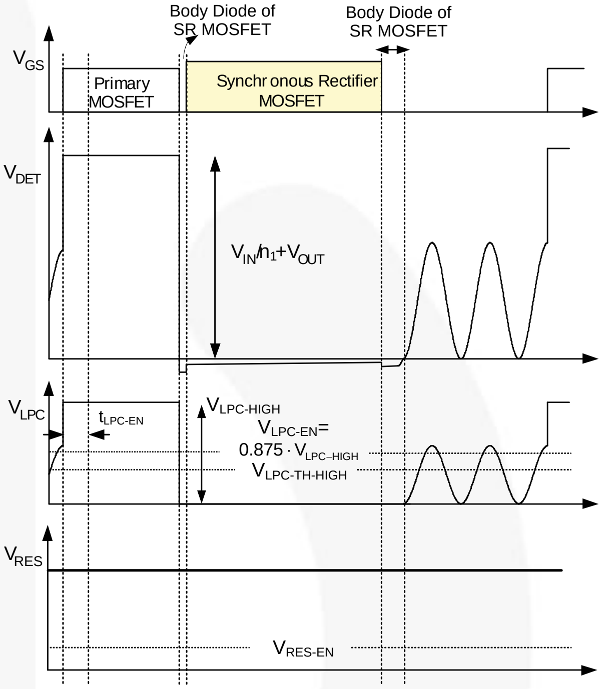

Figure 4. Typical Waveforms of QR Low-Side Flyback Converter with FAN6224

On the other hand, the maximum linear operating range of the LPC pin is under 4.8 V, so:

$$\frac{1}{Ratio_{LPC}} \cdot \left(\frac{V_{IN.MAX}}{n_1} + V_{OUT} \right) < 4.8 \tag{7}$$

where $V_{IN.MAX}$ is the maximum input voltage.

Therefore, when selecting proper $Ratio_{LPC}$, Equations(6) and (7) must be satisfied.

Combine (6) and (7), FAN6224 is applicable only if the system parameters, n_1, $V_{IN.MAX}$, $V_{IN.MIN}$, and V_{OUT} satisfy:

$$\frac{\left(\frac{V_{IN.MIN}}{n_1} + V_{OUT} \right)}{1.54} > \frac{\left(\frac{V_{IN.MAX}}{n_1} + V_{OUT} \right)}{4.8} \tag{8}$$

Therefore, verify the system parameters satisfy Equation (8) in the initial stage of design. If (8) is not satisfied, some parameters may need to be redesigned.

For low-side application, R_2 is suggested to be equal or larger than 12 kΩ. As shown in Figure 4, when the secondary side starts to conduct current, the MOSFET drain-to-source voltage (V_{DS}) is negative. To avoid the LPC pin from being damaged by the negative voltage, the LPC pin internally sources current when V_{LPC} is less than $V_{LPC\text{-}SOURCE}$ (0.1 V). Therefore, R_2 cannot be too small to clamp negative voltage on the LPC pin. After the resistance of R_2 is determined, R_1 can be calculated by Equation (5) with proper $Ratio_{LPC}$ selection. In practice, choose the maximum of $Ratio_{LPC}$ as an initial.

If the noise interference is severe on the LPC pin due to poor PCB layout, a small ceramic capacitor (around 10 pF to 22 pF) can be mounted parallel to the LPC pin.

When determining R_3 and R_4, the voltage scale-down ratio (K) between the RES and LPC pins must be taken into consideration first. Define K by:

$$K = \frac{Ratio_{LPC}}{Ratio_{RES}} \tag{9}$$

where:

$$Ratio_{RES} = \frac{R_3 + R_4}{R_4} \tag{10}$$

The SR MOSFET turns off when the internal timing capacitor, C_T, is fully discharged. If K is equal to 3.9, the discharge time of the C_T capacitor, $t_{CT.DIS}$, is the same as the inductor current discharge time, $t_{L.DIS}$. Therefore, the SR MOSFET turns off exactly when the inductor current reaches its initial value. However, considering the tolerance of voltage divider resistors and internal circuit, the scale-down ratio (K) should be larger than 3.9 to guarantee that $t_{CT,DIS}$ is shorter than $t_{L,DIS}$ and to avoid overlapping. It is typical to set K to be 4.2 to 4.7.

After the scale-down ratio is selected, $Ratio_{RES}$ can be calculated by Equation (8) since $Ratio_{LPC}$ is already obtained. Note that $Ratio_{RES}$ is also required to satisfy the linear operating range of RES pin (2~4.8 V). In other words, the equation below must be satisfied:

$$2 < \frac{V_{OUT}}{Ratio_{RES}} < 4.8 \tag{11}$$

If Equations (6), (7), and (11) show contradiction, some of the parameters (n_1, $V_{IN.MAX}$, $V_{IN.MIN}$, and V_{OUT}) may need to be fine-tuned. When determining the resistance of R_3 and R_4, since there is no concern of negative voltage of RES pin for low-side application, R_4 is suggested to be several-tens of kilo-ohms; R_3 can be calculated by Equation (10).

Flyback High-Side Rectification

The design considerations of the voltage divider of the LPC pin (R_1 and R_2) for high-side applications are the same as those for low-side because the drain-to-source voltage detected by R_1 and R_2 is equal for both applications. Therefore, (6) and (7) must be satisfied when applying FAN6224 to drive high-side MOSFET.

However, when determining the voltage divider of the RES pin (R_3 and R_4), the turn-ratio of secondary winding (N_2) and auxiliary winding (N_3) must be taken into consideration. The turn-ratio is defined as:

$$n_2 = \frac{N_2}{N_3} \tag{12}$$

Equation (9) is then rewritten as:

$$K = \frac{Ratio_{LPC}}{n_2 \cdot Ratio_{RES}} \tag{13}$$

R_3 and R_4 detect the reflected output voltage of the auxiliary winding rather than directly detecting the output voltage, so Equation (11) is modified as:

$$2 < \frac{V_{OUT}}{n_2 \cdot Ratio_{RES}} < 4.8 \tag{14}$$

For high-side application, R_4 is recommended to be equal or larger than 27 kΩ for clamping negative voltage of the RES pin. As Figure 5 shows, when primary-side MOSFET (Q_1) turns on, the voltage across N_3 (V_{N3}) is negative. Through the voltage divider of the RES pin, the RES pin voltage (V_{RES}) is also negative. To avoid the controller being damaged by negative voltage, the RES pin internally sources current when V_{RES} is less than $V_{RES\text{-}SOURCE}$ (0.2 V). Therefore, R_4 cannot be too small to clamp the negative voltage on the RES pin. After the resistance of R_4 is determined, R_3 can be calculated by (10).

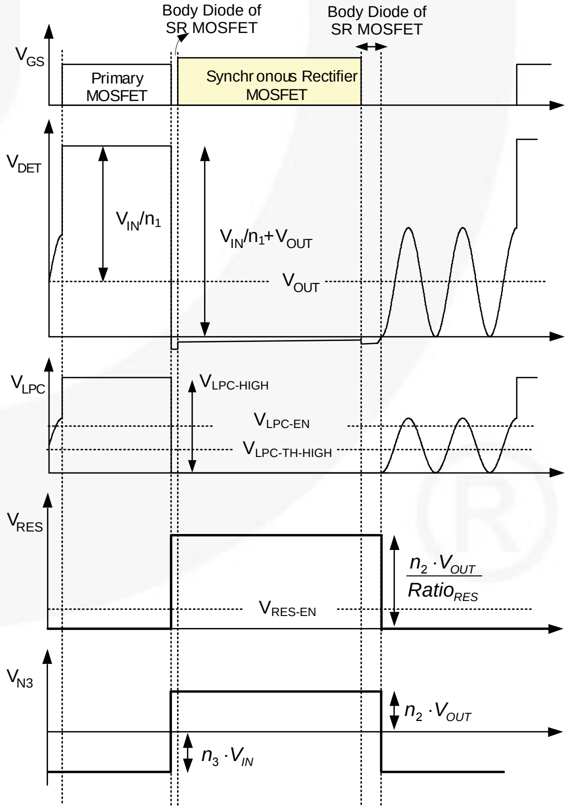

Figure 5. Typical Waveforms of QR High-Side Flyback Converter with FAN6224

Forward / Dual-Switch Forward Free-Wheeling Rectification

Figure 3 shows the typical application circuit of applying FAN6224 on dual-switch forward free-wheeling rectification. The related key waveform is shown in Figure 6. When the primary MOSFETs turn on, the reflected voltage across the SR MOSFET, V_{DET}, is obtained as:

$$V_{DET} = \frac{V_{IN}}{n_1} \tag{15}$$

where n_1 is defined as the turn-ratio between N_1 and N_2, which is the same as (4). Since V_{DET} is different from that of flyback application, (6) and (7) are rewritten as:

$$\frac{V_{IN.MIN}}{Ratio_{LPC} \cdot n_1} > 1.54 \tag{16}$$

$$\frac{V_{IN.MAX}}{Ratio_{LPC} \cdot n_1} < 4.8 \tag{17}$$

The resistance of R_2 is also suggested to be equal to or larger than 12 kΩ and the following design procedure is much the same as flyback applications. Start with selecting the maximum of $Ratio_{LPC}$, then calculate R_1 by (5). Next, consider the dead-time and select a proper scale-down ratio (K) between 4.2 and 4.7. Then $Ratio_{RES}$ is calculated by (8) and the result must satisfy (10). Finally, select the resistance of R_4, which is around several-tens of kilo-ohms, then R_3 can be calculated by (9).

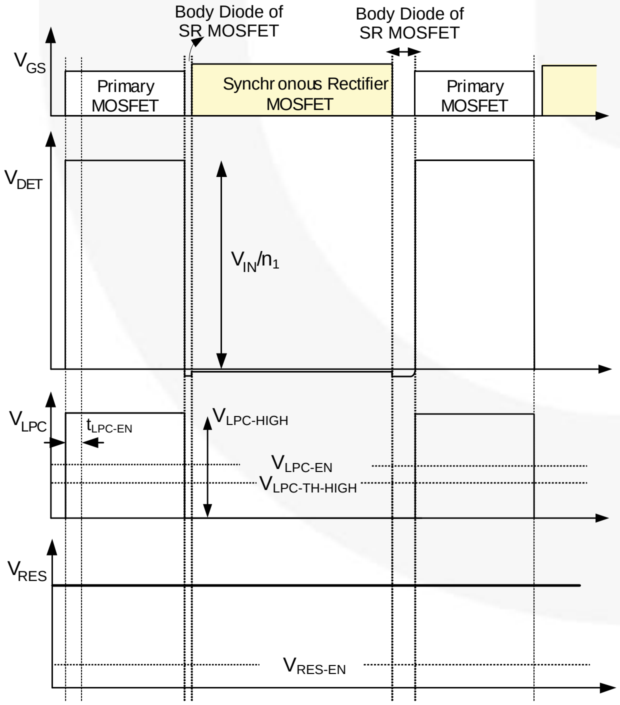

Figure 6. Typical Waveforms of Forward Free-Wheeling Rectification with FAN6224

Green Mode Modulation

To minimize the power consumption at light-load and no-load condition, the FAN6224 enters Green Mode and the SR MOSFET switching is disabled. As shown in Figure 7, the discharge time of the inductor and internal capacitor (C_T) decrease as load decreases. If the discharge time of the C_T capacitor ($t_{CT,DIS}$) is shorter than $t_{GREEN-ON}$ for more than three cycles, the SR controller enters Green Mode and the operating current is reduced to 300 µA.

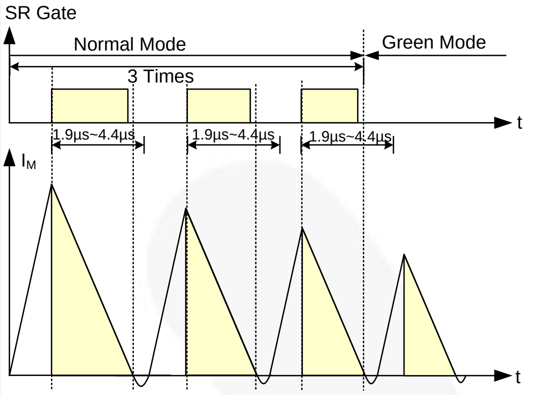

Figure 7. Timing of Entering Green Mode

In contrast, when the discharge time of the C_T capacitor is longer than $t_{GREEN-OFF}$ for more than fifteen cycles, the SR controller leaves Green Mode and resumes normal operation, as shown in Figure 8.

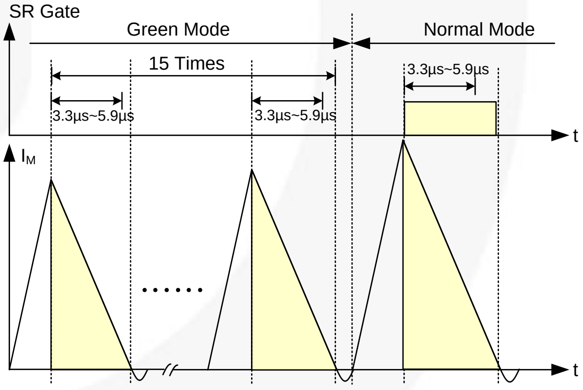

Figure 8. Timing of Resuming Normal Operation

To enhance the flexibility of design, $t_{GREEN-ON}$ and $t_{GREEN-OFF}$ are adjustable by the external resistor, R_{RP}. The R_{RP} resistance corresponds to $t_{GREEN-ON}$ and $t_{GREEN-OFF}$ and the equations are defined as:

$$t_{GREEN-ON} = 0.02 \cdot R_{RP} + 0.4 \tag{18}$$

$$t_{GREEN-OFF} = t_{GREEN-ON} + 1.34 \tag{19}$$

As the characteristic curve shows in Figure 9, the minimum and maximum values of R_{RP} resistance are 75 kΩ and 200 kΩ, respectively. Each R_{RP} resistance corresponds to a set of $t_{GREEN.ON}$ and $t_{GREEN.OFF}$.

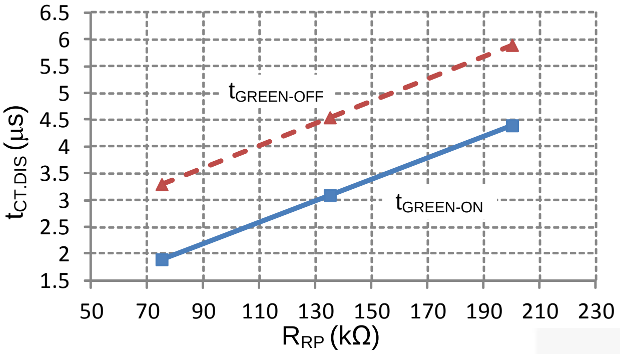

Figure 9. Adjustable $t_{GREEN\text{-}ON}$ and $t_{GREEN\text{-}OFF}$

When selecting the resistance of R_{RP}, the loading of entering Green Mode is first determined, then $t_{GREEN\text{-}ON}$ is measured and R_{RP} can be calculated by Equation (17). In practice, at least two efficiency curves need to be measured and compared to optimize the design. One uses the minimum value of R_{RP} (75 kΩ), while the other uses the maximum value (200 kΩ). The loading of the crossover of the two curves is the optimized loading to enter Green Mode. If there is no crossover, then either 75 kΩ or 200 kΩ is the best choice.

Design Example for Flyback High-Side Rectification

Step 1. Define System Parameters

- The maximum input voltage, $V_{IN.MAX}$: 373 V
- The minimum input voltage, $V_{IN.MIN}$: 86 V
- Output voltage, V_{OUT}: 19 V
- Turns of the primary-side winding, N_1: 38 turns
- Turns of the secondary-side winding, N_2: 8 turns
- Turn-ratio n_1: 4.75
- Take $V_{IN.MAX}$, $V_{IN.MIN}$, n_1, and V_{OUT} into (8):

$$\frac{\left(\frac{86}{4.75}+19\right)}{1.54} > \frac{\left(\frac{373}{4.75}+19\right)}{4.8}$$

FAN6224 is applicable for this system.

Step 2. Calculate the Auxiliary Winding, N_3:

V_{DD} is set between 11.5 V and 26 V. Select 15 V and N_3 can be obtained from (1),

$$N_3 = \frac{V_{DD} \cdot N_2}{V_{OUT}} = 6.3$$

N_3 is then selected as 6 turns.

Step 3. Calculate the Operating Range of $Ratio_{LPC}$:

The maximum of $Ratio_{LPC}$ is obtained from (6):

$$Ratio_{LPC} < \frac{\frac{V_{IN.MIN}}{n_1} + V_{OUT}}{1.54} = 24.1$$

The minimum of $Ratio_{LPC}$ is obtained from (7):

$$Ratio_{LPC} > \frac{\frac{V_{IN.MAX}}{n_1} + V_{OUT}}{4.8} = 16.9$$

$Ratio_{LPC}$ is selected as 23.5. In practice, choose $Ratio_{LPC}$ close to its maximum value is a good start. In the following steps, if the calculated $Ratio_{RES}$ is over its operating range, return to this step and reconsider the selection of $Ratio_{LPC}$.

Step 4. Calculate the Resistance of R_1:

The resistance of R_2 is first selected as 12 kΩ, as long as it is large enough to clamp negative voltage of the LPC pin. R_1 is then obtained from Equation (5) as:

$$R_1 = R_2 \cdot (Ratio_{LPC} - 1) = 270\ \text{k}\Omega$$

Step 5. Calculate $Ratio_{RES}$:

First, select a proper scale-down ratio (K) between 4.2 and 4.7. The selection is based on the adjustment of dead-time and can be fine-tuned later. In this case, 4.11 is selected and $Ratio_{RES}$ is calculated by Equation (12) as:

$$Ratio_{RES} = \frac{Ratio_{LPC}}{n_2 \cdot K} = \frac{23.5}{1.33 \cdot 4.11} = 4.3$$

Second, check whether $Ratio_{RES}$ satisfies Equation (14). If it does not fit into the operating range, go back to Step 3 and reconsider the selection of $Ratio_{LPC}$. In this case,

$$2 < \frac{V_{OUT}}{Ratio_{RES} \cdot n_2} = \frac{19}{4.3 \cdot 1.33} = 3.32 < 4.8$$

The result is acceptable.

Step 6. Calculate the Resistance of R_3

The resistance of R_4 is first selected as 27 kΩ, as long as it is large enough to clamp negative voltage of the RES pin. R_3 is then obtained from Equation (10) as:

$$R_3 = R_4 \cdot (Ratio_{RES} - 1) = 89.1\ \text{k}\Omega$$

As a result, the resistance of R_1, R_2, R_3, and R_4 are calculated. If the dead-time is checked, then the four resistors are determined. The process of fine-tune the dead-time is explained in the following section.

Troubleshooting

Fine-Tune the Dead-Time

If SR dead-time is too large, decrease R_1 or increase R_2. Either way, V_{LPC} is increased and the discharge time of C_T capacitor ($t_{CT.DIS}$) is prolonged to decrease the dead-time, as shown in Figure 10. However, note that Equation (7) must be satisfied when increasing V_{LPC}.

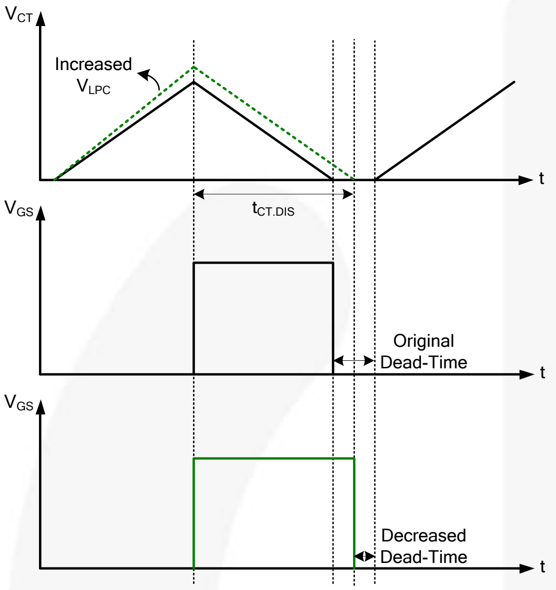

Figure 10. Decrease SR Dead-Time

In contrast, if SR dead-time is too small, decrease R_3 or increase R_4. Either way, V_{RES} is increased and the discharge time of C_T capacitor ($t_{CT.DIS}$) is reduced to increase the dead-time, as shown in Figure 11. However, note that (14) must be satisfied when increase V_{RES}.

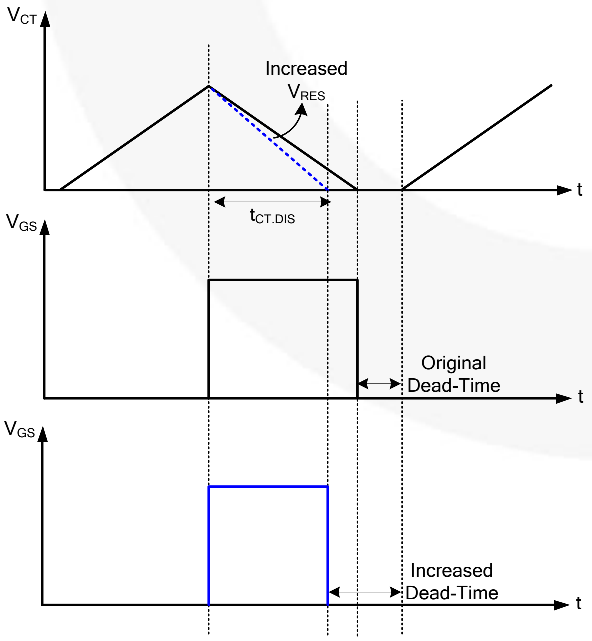

Figure 11. Increase SR Dead-Time

FAN6224 is Unable to Enter Green Mode

The loading to enter Green Mode is determined by the on-time of SR and is adjustable by R_{RP}. If FAN6224 can't enter Green Mode, select larger R_{RP} resistance. As the SR on-time is shorter than the set $t_{GREEN\text{-}ON}$ as load decreases, the controller enters Green Mode.

The SR Does Not Switch

First, verify the V_{DD} operating voltage is between 11.5 V and 26 V. Second, verify the $V_{LPC\text{-}HIGH}$ is larger than 1.54 V, as defined in Equation (3). Third, when the SR MOSFET or its body diode conducts; verify that V_{RES} is larger than 2 V. Finally, verify FAN6224 is not in Green Mode.

The SR Switches for a While and Shuts Down Repetitively

In static-load operation, the SR switches on and off regularly according to linear-predict timing control. However, during a load transient, the charge and discharge of inductor current is not always balanced. Therefore, FAN6224 includes several functions; such as LPC-width expansion and shrink protection, gate-expansion-limit protection, fault-timing protection, RES-voltage-drop protection, and LPC and RES pin open/short protection that prevents overlapping due to voltage-second imbalance. Once those protections are triggered, FAN6224 shuts down SR switching immediately and returns to normal operation after the abnormal conditions are cleared. Refer to the datasheet for the detailed descriptions and check if any of those protections are triggered in static-load operation.

Printed Circuit Board Layout

Figure 12 and Figure 13 show the layout for FAN6224 in low-side and high-side systems, respectively. Good PCB layout improves efficiency, minimizes excessive EMI, and prevents the power supply from being disrupted during surge/ESD tests.

IC Side:

- The reference ground of the LPC and RES pins is connected to the IC GND directly (trace 1).
- The GND and AGND pins should be connected together with a short wide trace or a wide area (trace 2).
- The reference ground of C_{VDD} should directly connect to the GND and AGND pins (trace 3), then connect to the output ground (trace 4).
- The trace line of LPC and RES should be away from magnetic components.

System Side:

- Since trace 5 is the power loop on the secondary side, it must be as short and wide as possible.
- The Y-CAP should be connected to the output ground directly (trace 6).

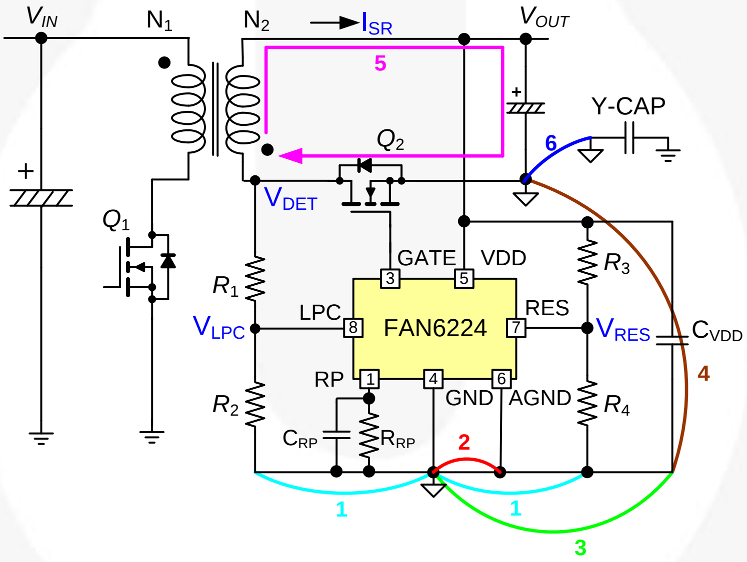

Figure 12. Layout Considerations of Low-Side System

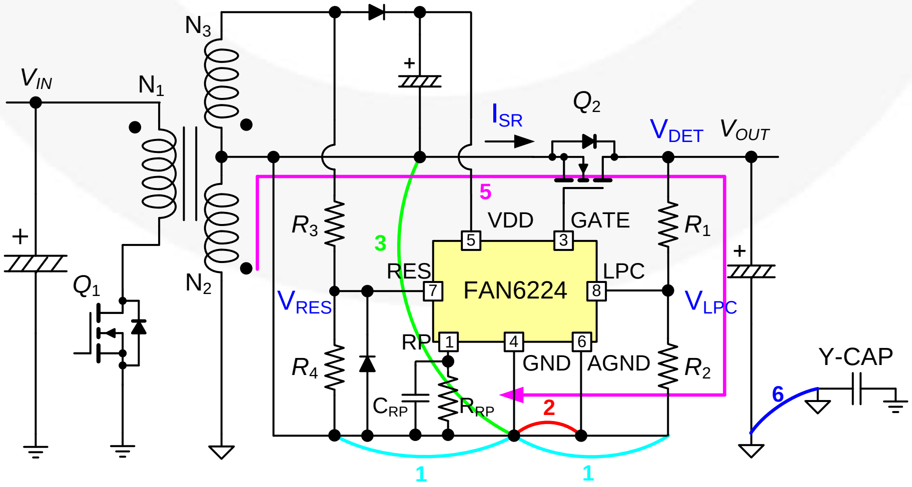

Figure 13. Layout Considerations of High-Side System

Design Example

This section shows a design example of a 65 W (19 V / 3.42 A) adaptor using FAN6756. The schematic is shown in Figure 14. From the specification, all critical components are covered and the final measurement results are given.

Table 1. System Specification

Input	
Input Voltage Range	90~264 V_{AC}
Line Frequency Range	47~63 Hz
Output	
Output Voltage (V_o)	19 V
Output Power (P_o)	65 W

Based on the design guideline, the critical parameters are calculated and summarized as shown in Table 2.

Table 2. Critical System Parameters

PWM Stage	
Turns of Primary Inductor of PWM Transformer (N_P)	38 Turns
Turns of Secondary Inductor of PWM Transformer (N_S)	8 Turns
Turns of Auxiliary Winding of PWM Transformer (N_{AUX1})	7 Turns
Turns of Auxiliary Winding of PWM Transformer (N_{AUX2})	6 Turns
Turns Ratio of PWM Transformer (n)	4.75
Primary Inductor (L_P)	510 µH
Switching Frequency (f_S)	65 kHz

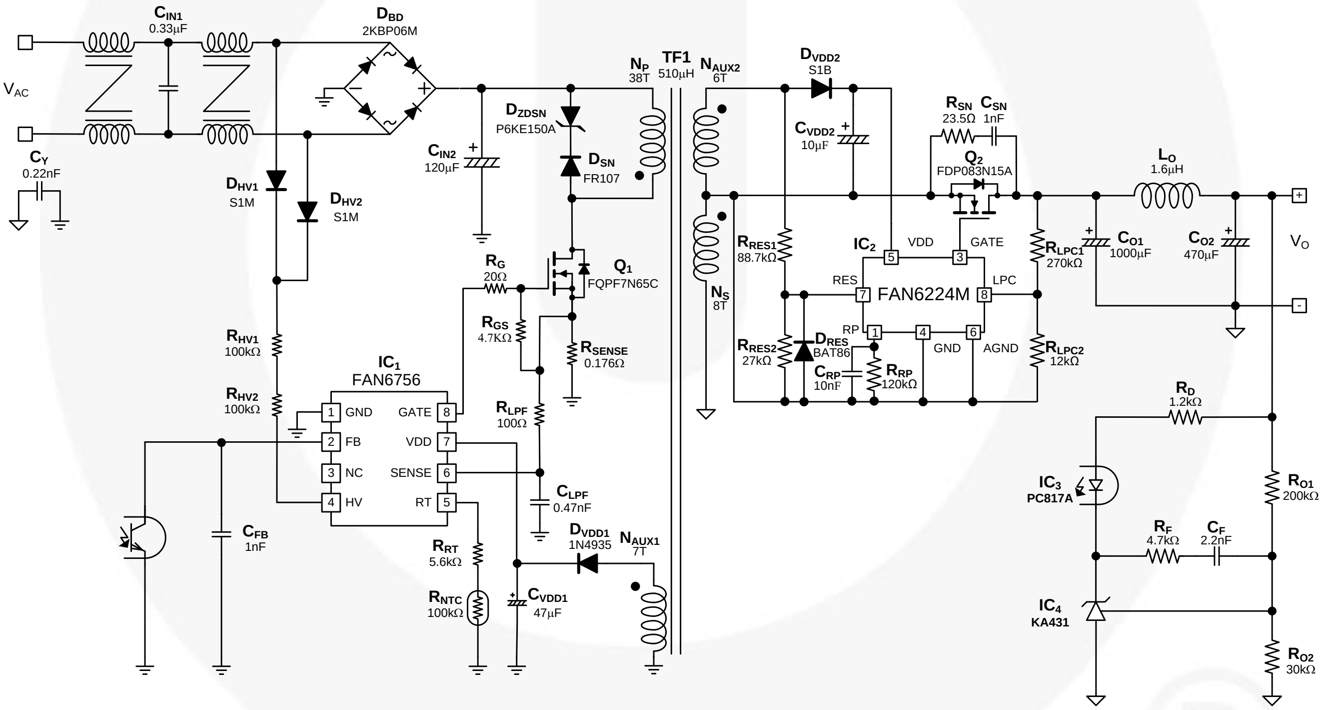

Figure 14. Complete Circuit Diagram

Table 3. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			C_{VDD1}	47 µF	50 V
R_D	1.2 kΩ	1/4 W	C_{VDD2}	10 µF	50 V
R_F	4.7 kΩ	1/8 W	C_Y	0.22 nF	Y-CAP
R_G	20 Ω	1/4 W	**Diode**		
R_{GS}	4.7 kΩ	1/4 W	D_{BD}	2KBP06M	
R_{HV1}	100 kΩ	1/4 W	D_{HV1}	S1M	
R_{HV2}	100 kΩ	1/4 W	D_{HV2}	S1M	
R_{LPC1}	270 kΩ	1/8 W	D_{RES}	BAT86	
R_{LPC2}	12 kΩ	1/8 W	**MOSFET**		
R_{LPF}	100 Ω	1/8 W	D_{SN}	FR107	
R_{NTC}	100 kΩ		D_{VDD1}	1N4935	
R_{O1}	200 kΩ	1/8 W	D_{VDD2}	S1B	
R_{O2}	30 kΩ	1/8 W	D_{ZDSN}	P6KE150A	
R_{RES1}	88.7 kΩ	1/8 W	Q_1	FQPF7N65C	
R_{RES2}	27 kΩ	1/8 W	Q_2	FDP083N15A	
R_{RP}	120 kΩ	1/8 W	**Inductor**		
R_{RT}	5.6 kΩ	1/4 W	L_O	1.6 µH	
R_{SENSE}	0.176 Ω	1 W	**IC**		
R_{SN}	23.5 Ω	1/2 W	IC_1	FAN6756A	
Capacitor			IC_2	FAN6224M	
C_F	2.2 nF		IC_3	FOD817A	
C_{FB}	1 nF		IC_4	KA431AZTA	
C_{IN1}	0.33 µF	X-CAP			
C_{IN2}	120 µF	400 V			
C_{LPF}	0.47 nF				
C_{O1}	1000 µF	25 V			
C_{O2}	470 µF	25 V			
C_{RP}	10 nF				
C_{SN}	1 nF				

Figure 15 shows the test waveforms of 100% loading (3.42 A) on 19 V / 65 W evaluation board. The SR gate can be turned off by the linear-predict timing control and can keep a dead time between the primary-side and secondary-side MOSFET.

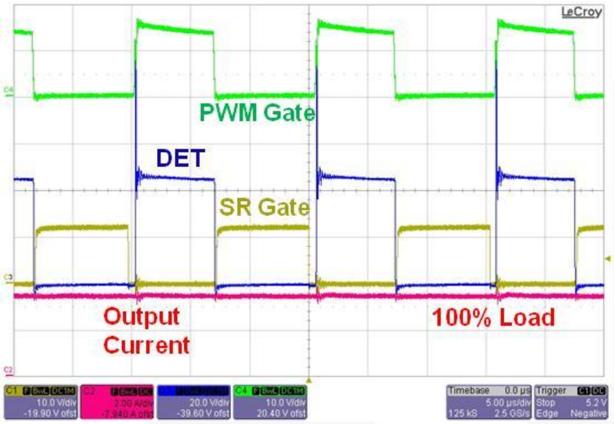

Figure 15. Test Waveforms of 100% Loading

Figure 16 shows the test waveforms of 25% loading on a 19 V / 65 W evaluation board. Linear-predict timing control can also be activated to turn off the SR MOSFET to prevent overlapping with the primary-side MOSFET.

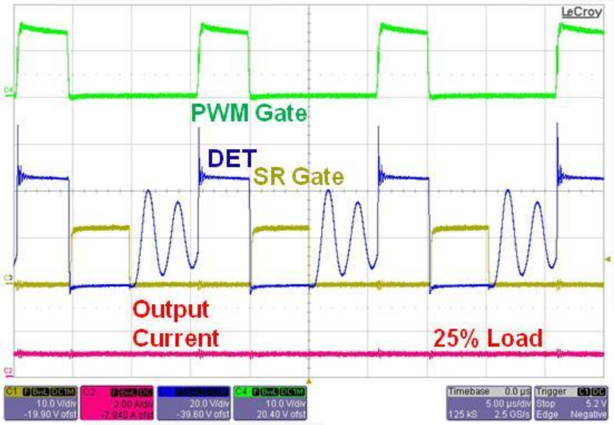

Figure 16. Test Waveforms of 25% Loading

Figure 17 and Figure 18 show the test waveforms for load changing from light load to heavy load and from heavy load to light load. There is no overlapping between the primary-side and secondary-side MOSFET.

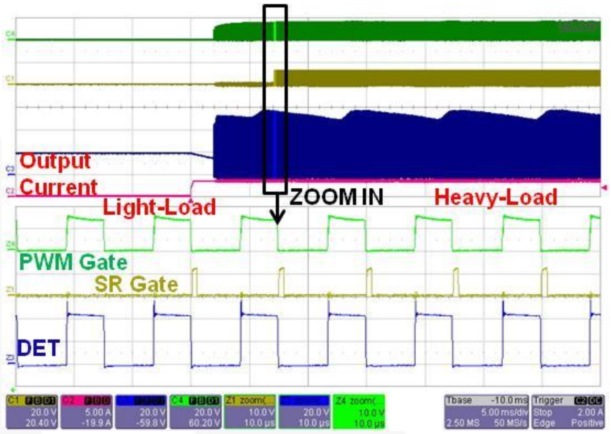

Figure 17. Test Waveforms for Load Change (from Light-Load to Heavy-Load)

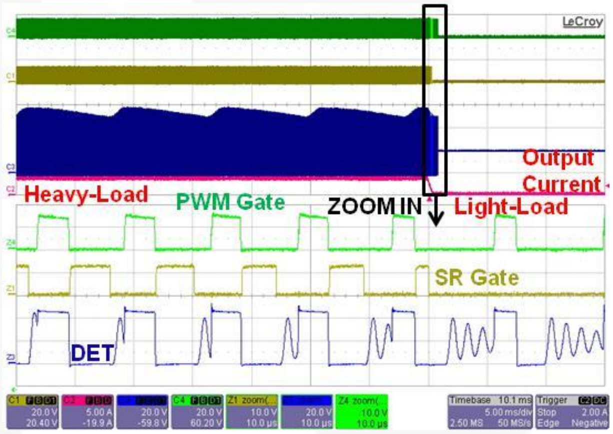

Figure 18. Test Waveforms for Load Change (from Heavy-Load to Light-Load)

Related Resources

FAN6224 — Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

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