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AN-6206

Primary-Side Synchronous Rectifier (SR) Trigger Solution for Dual-Forward Converter

Introduction

In any switching converter, rectifier diodes are used to obtain DC output voltage. The conduction loss of diode rectifier contributes significantly to the overall power losses in a power supply; especially in low output voltage applications, such as personal computer (PC) power supplies. The conduction loss of a rectifier is proportional to the product of its forward-voltage drop and the forward conduction current. Using synchronous rectification (SR) where the rectifier diode is replaced by MOSFET with proper on resistance (Rds_{ON}), the forward-voltage drop of a synchronous rectifier can be lower than that of a diode rectifier and, consequently, the rectifier conduction loss can be reduced.

The highly integrated FAN6210 is a primary-side SR controller for dual-forward converter that provides control signals for the secondary-side SR driver FAN6206. FAN6210 also provides drive signal for the primary-side power switches by using an output signal from the PWM controller. FAN6210 can be combined with any PWM controller that can drive a dual-forward converter. To obtain optimal timing for the SR drive signals, transformer winding voltage is also monitored. To improve light-load efficiency, green-mode operation is employed, which disables the SR turn-on trigger signal, minimizing gate drive power consumption at light-load condition.

This application note describes the design procedure of SR circuit using FAN6210 and FAN6206. The guidelines for printed circuit board (PCB) layout and a design example with experiment results are also presented.

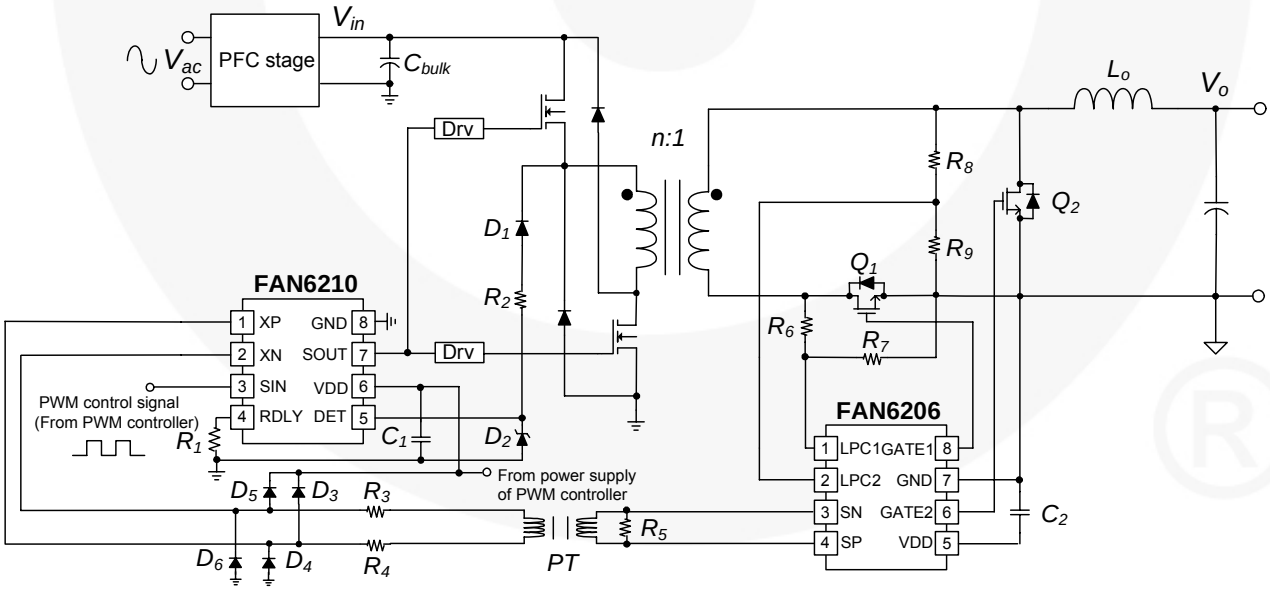

Figure 1. Typical Application

1. FAN6210 External Component Setting

Figure 2 and Figure 3 show the simplified schematic of two switch forward converters and their waveforms. The rectifying SR (SR1) should be turned on right after the primary-side MOSFETs are turned on. Then, SR1 should be turned off right before the primary-side MOSFETs are turned off. The freewheeling SR (SR2) should be turned on right after the primary-side MOSFETs are turned off. Then, SR2 should be turned off right before the primary-side MOSFETs are turned on. The primary-side SR trigger controller FAN6210 generates XN and XP signals, where XN rising edge triggers the turn-off of SR and XP rising edge triggers the turn-on of SR. FAN6210 generates XP and XN signals two times for each in one switching cycle and FAN6206 in the secondary side determines which SR MOSFET should be controlled for each XP and XN signals within one switching cycle.

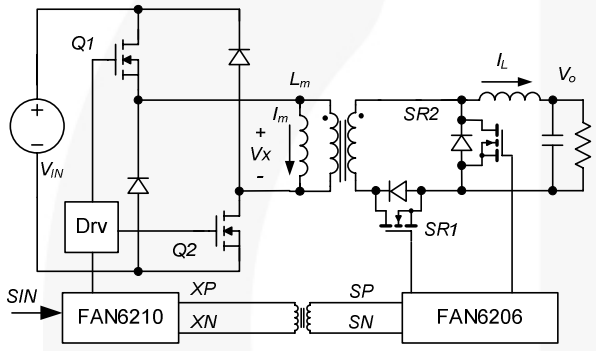

Figure 2. Simplified Circuit Diagram of Dual-Forward Converter

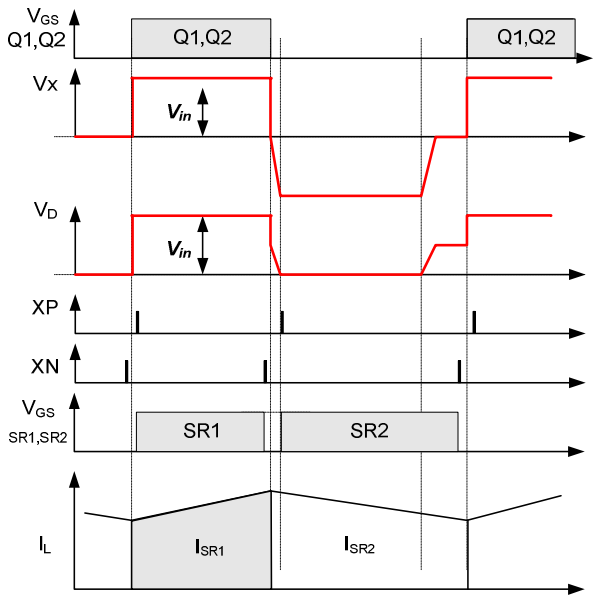

Figure 3. Key Waveforms of Dual-Forward Converter

Figure 4 and Figure 5 show the detailed timing diagrams of XP and XN for the rising edge and falling edge of the SIN signal. The delay from the rising edge of SOUT to XP signal rising edge (t_{DLY_XP}) is programmable using R_1, as shown in Figure 1. The linear relationship between R_1 and t_{DLY_XP} is shown in Figure 6.

The transformer winding voltage is much higher than the voltage rating of FAN6210 during PWM turn-on time. Therefore, R_2 and D_1 are used to block the high voltage, as shown in Figure 1. Since there is a 400ns DET falling-edge detection window after SOUT falls to prevent mis-triggering of XP in DCM operation, too large value of R_2 does not trigger XP properly due to too large RC time delay. It is typical to use 10kΩ~33kΩ for R_2.

The other requirement for triggering XP signal is that the HIGH level of the DET signal must be higher than 3V. To shorten the falling time from HIGH level to LOW level, the breakdown voltage of Zener diode D_2 is recommended as 5~6V.

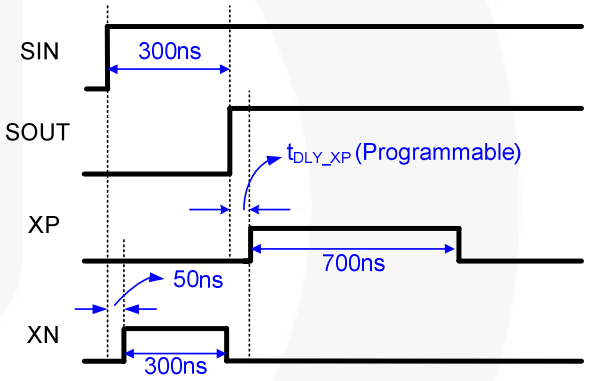

Figure 4. Timing Diagram During PWM Rising Edge

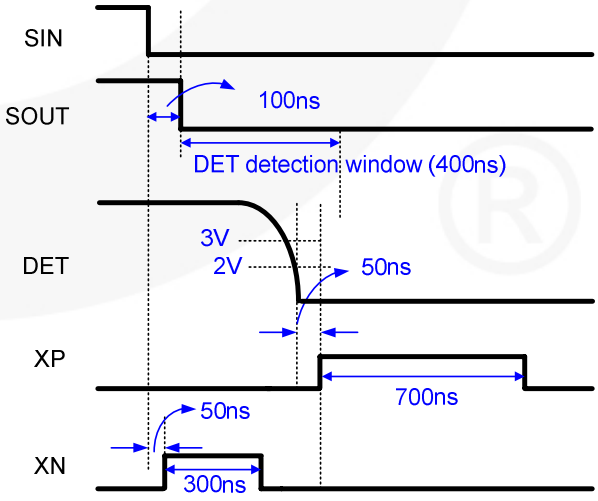

Figure 5. Timing Diagram During PWM Falling Edge

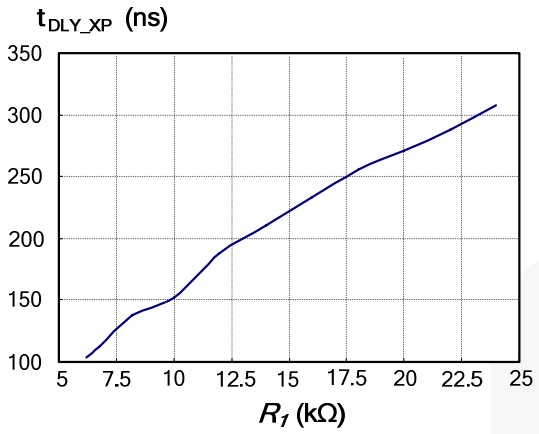

Figure 6. Programmable Delay with Resistor R_1

2. Pulse Transformer (PT)

The differential SR control XP-XN is delivered from FAN6210 to FAN6206 through a pulse transformer (*PT*), as shown in Figure 7. For the proper signal transfer, the core should have high initial permeability (μ_i). To separate primary-side and secondary-side windings, isolation is also necessary. It is typical to have the same number of turns for the primary and secondary to maximize the coupling. As the inductance of the winding decreases, the magnetizing increases, causing the voltage drop in the primary winding, as shown in Figure 8. The HIGH level of XP or XN signal should be higher than 4V to ensure proper SR gate driving. Meanwhile, too many turns may increase the inter-winding capacitance and, therefore, the inductance value should be determined properly. Typically, the inductance value is recommended as 100μH~300μH.

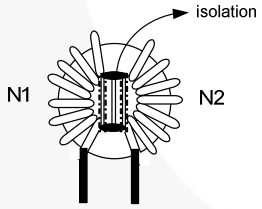

Figure 7. Pulse Transformer Structure

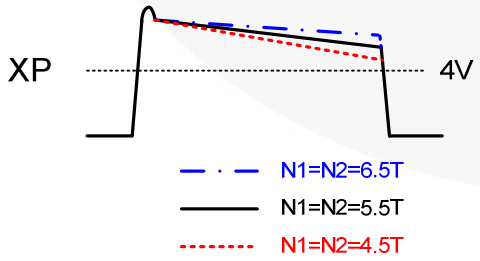

Figure 8. Slope Difference Between Different Turn Number On XP Signal

To protect the XP and XN pins from transient voltage spikes; components R_3, R_4, D_3, D_4, D_5, and D_6 are necessary (shown in Figure 1). R_3 and R_4 are recommended as 10Ω. D_3~D_6 are chosen as Fairchild diode 1N4148.

At the secondary side, R_5 is connected between the SP and SN pins for reducing the overshoot caused by *PT*. The proper value of R_5 is 1kΩ~10kΩ for most of applications.

FAN6206 External Components Setting

FAN6206 needs only four resistors to achieve winding detection and linear-predict control (LPC). Voltage divider with R_6 and R_7 detects the voltage across the drain-to-source terminal of Q_1, while the other divider with R_8 and R_9 detects the voltage across the drain-to-source terminal of Q_2. Figure 9 shows the typical waveform under CCM operation, which includes rectifying SR MOSFET drain voltage ($V_{ds\text{-}R}$), freewheeling SR MOSFET drain voltage ($V_{ds\text{-}F}$), inductor current (I_{Lo}), SR control signals (SP & SN), and SR gate signals. The detected signal on LPC1 and LPC2 pin determines the operation of synchronous rectification.

The voltage divider scale-down factors are defined as:

$$Ratio_{LPC1} = \frac{R_7}{R_6 + R_7} \quad (1)$$

$$Ratio_{LPC2} = \frac{R_9}{R_8 + R_9} \quad (2)$$

2.1 Rectifying SR Gate Drive

Linear-predict control (LPC) is not essential for rectifying SR because rectifying SR is always turned off by the SN signal. Voltage divider with R_6 and R_7 is used to detect the HIGH/LOW status of $V_{ds\text{-}R}$, as shown in Figure 9. The HIGH level threshold voltage for LPC1 is 2V, so the plateau voltage of LPC1 should be higher than 2V. To guarantee stable operation, the minimum plateau voltage of LPC1 is suggested to be 3V. However, LPC pin is a low-voltage pin, so the proper operation range is from 3V to 5V. Therefore:

$$3 < Ratio_{LPC1} \cdot \frac{V_{in}}{n} < 5 \quad (3)$$

where $Ratio_{LPC1}$ is specified in Equation 1, V_{in} is the input voltage for PWM stage, and n is the turn ratio between primary and secondary winding.

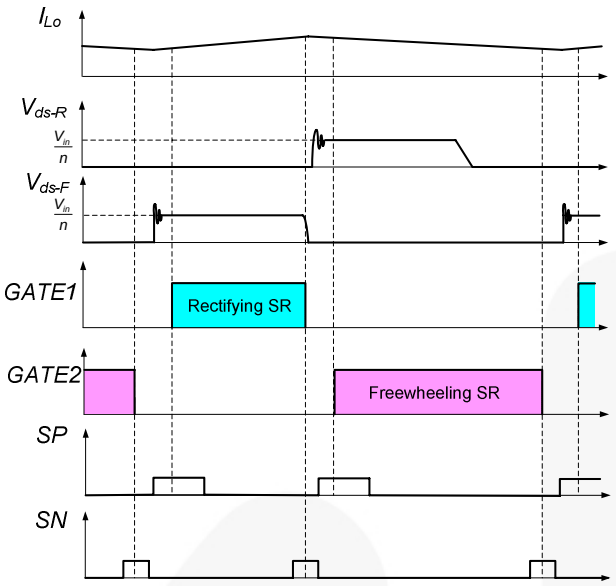

Figure 9. Typical Waveform in CCM Operation

2.2 Freewheeling SR Gate Drive

Once the forward converter enters discontinuous conduction mode (DCM) at light-load condition, the current through the freewheeling SR decreases to zero before the turn-off command by XN signal is given. Thus, the current can flow in the reverse direction if the freewheeling SR is not turned off before the current changes direction. LPC function is necessary to turn off the free-wheeling SR before the output inductor current reaches zero in DCM operation.

Voltage divider with R_8 and R_9 determines the turn-off timing of freewheeling SR. For proper LPC operation, the LPC pin voltage should be normalized to the nominal output voltage. The scale-down factor of the voltage divider should be $1/V_O$.

For 12V output application, the proper value of $Ratio_{LPC2}$ is:

$$\frac{1}{11.5} < Ratio_{LPC2} < \frac{1}{12} \quad (4)$$

Figure 10 shows the typical waveform in DCM operation. In proper designs, freewheeling SR is turned off before I_{Lo} decreases to zero. $Ratio_{LPC2}$ determines the internal charge current of LPC function. Figure 11 shows the relationship between $Ratio_{LPC2}$ and freewheeling SR gate drive signal. The voltage level detected by the LPC2 pin (V_o/n) determines the internal charge current I_{CHG}. If $Ratio_{LPC2}$ becomes smaller, I_{CHG} decreases. The voltage level of the VDD pin determines the internal discharge current I_{DISCHG}. However, I_{DISCHG} does not vary with $Ratio_{LPC2}$. Therefore, the discharging period is shortened. The turn-off instant of freewheeling SR gets earlier when $Ratio_{LPC2}$ gets lower. If $Ratio_{LPC2}$ gets too much higher, freewheeling SR is still turned on after I_{Lo} decreases to zero. Therefore, negative I_{Lo} is generated. Abnormal voltage on V_{dsR} is derived from negative I_{Lo} and exceeds the V_{ds} rating of MOSFET in DCM operation. It's important to determine $Ratio_{LPC2}$ properly. For normal LPC operation, the value of R_7 and R_9 are recommended as 4.7kΩ~15kΩ. R_6 and R_8 can be calculated according to proper $Ratio_{LPC1}$ and $Ratio_{LPC2}$.

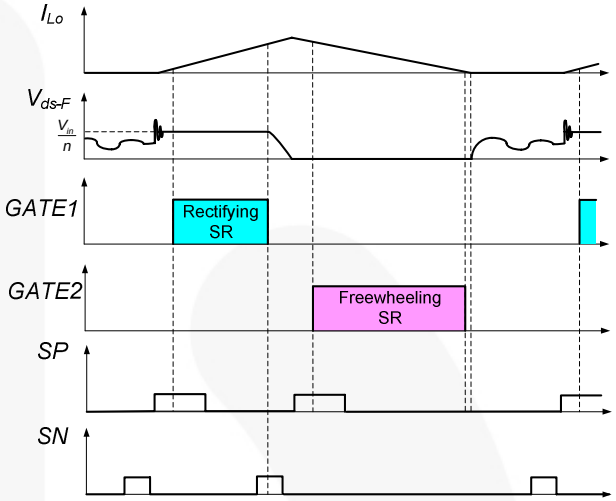

Figure 10. Typical Waveform in DCM Operation

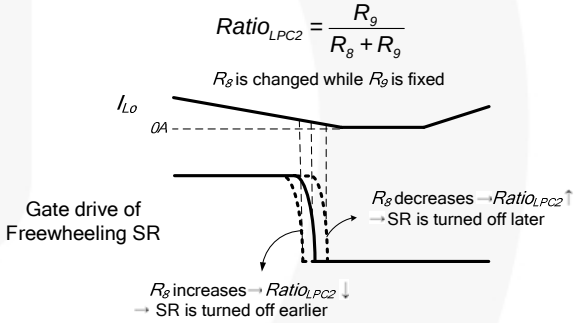

Figure 11. Typical Waveform of QR Operation

2.3 VDD Section

The power supply source of FAN6206 is provided from output voltage terminal (V_o). To keep FAN6206 away from output current interference, the VDD pin is suggested not to be connected to V_o directly. In PC power applications, the supervisor IC is applied to manage the protection of secondary side. Output terminal V_o is connected to the supervisor to achieve protection under abnormal conditions. Therefore, V_o detecting terminal of the supervisor IC can be used as the power source of the VDD pin. Adding a capacitor C_2 between the VDD pin and the GND pin can keep the VDD pin away from noise. Adding a capacitor C_1 is also recommended for the VDD pin of FAN6210. The recommended value for C_1 and C_2 is 100nF~1μF.

Printed Circuit Board Layout

In Figure 12, the power traces are marked as bold lines. Good PCB layout improves power system efficiency, minimizes excessive EMI, and prevents the power supply from being disrupted during surge/ESD tests.

Guidelines

- For PC power applications, the PFC/PWM combination controller is usually separated from main board and is applied at a daughter board. FAN6210 is also recommended to be placed on the same daughter board. As indicated by **1** and **2**, FAN6210 control circuits' ground should be connected together and to the GND pin of FAN6210 first, then the GND pin to ground of PFC/PWM combination controller.
- As indicated by **3** and **4**, PFC/PWM combination controller's ground and PWM MOSFETs' ground are connected to the negative terminal of C_{bulk}. Keep trace **4** short, direct, and wide.
- A Y-cap between the primary and secondary is necessary for PC power applications. As indicated by **5** and **6**, the Y-cap is suggested on the low-side, where it is between the negative terminal of C_{bulk} and case. Connecting trace **6** directly to case is helpful to surge immunity. According to the safety requirements, the creepage between the two pointed ends should be at least 5mm. The Y-cap should be far away from *PT*.
- As indicated by **8**, FAN6206 control circuits' ground should be connected together, then to the GND pin of FAN6206.
- As indicated by **9**, the GND pin of FAN6206 should be connected to the source of Q_1 and Q_2 separately. Keeping trace **9** short and direct can maintain the ground level between MOSFET and GND pin closed. Thus, the SR control signal can be kept away from error triggering.
- As indicated by **10**, the source terminals of Q_1 and Q_2 are connected to the negative terminal of C_o. Keep trace 10 short, direct, and wide.
- As indicated by **11**, V_o is connected to the supervisor IC. As indicated by **12**, the power supply source of FAN6206's VDD pin is connected to the detection terminal of supervisor IC. Trace **11** should be long and far away from V_o terminal. It's helpful to prevent LPC mechanism from output current interference.
- As indicated by **7**, the negative terminal of C_o is connected to case directly.

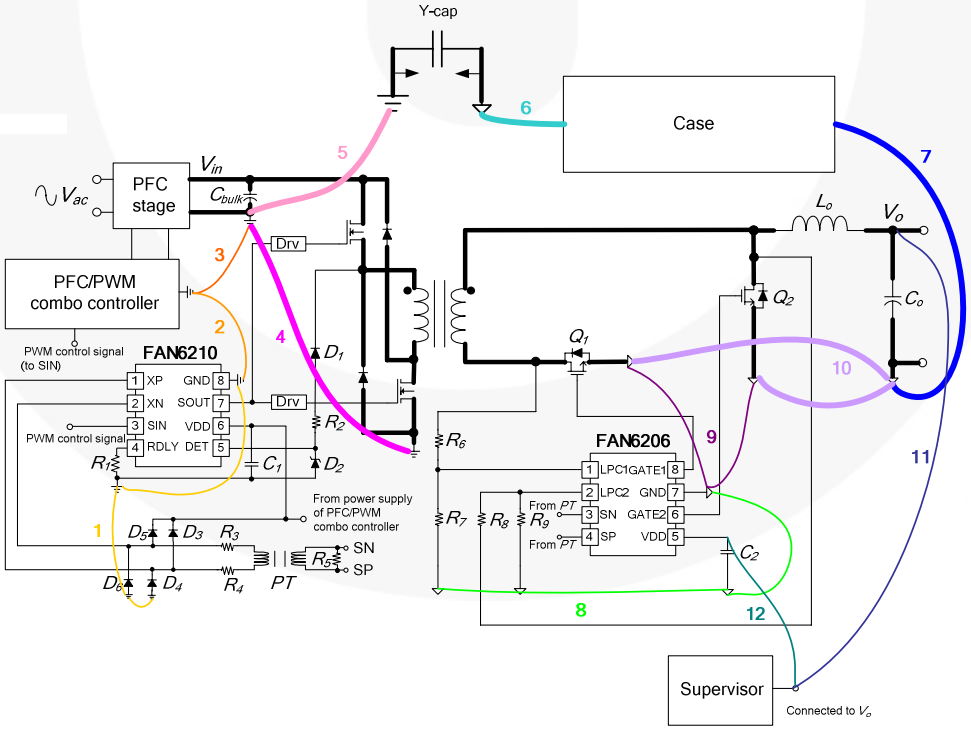

Figure 12. Layout Considerations

Design Example

The following example is a 12V/300W PC power supply, in which the dual-forward topology is used. As Figure 13 shows, the FAN4801 integrated CCM PFC/PWM combination controller is used as the controller for both PFC stage and PWM stage.

The basic system parameters are listed in Table 1.The two-level V_{bulk} is derived from FAN4801. The typical voltage level for V_{bulk} is 380V; but under low-line and light-load condition, V_{bulk} is 310V for decreasing power loss at the PFC stage. The typical switching frequency (f_s) is 65kHz for both PFC and PWM stage.

In a typical PC power application, multi-output is necessary. If the 12V output terminal is used to generate other output terminals, SG6520 can be the proper supervisor IC. The power supply of the supervisor is from 5V standby output terminal. Flyback topology is the general structure for standby power. The following measurements include standby loading. FAN6751 is chosen to be the PWM controller of standby stage.

From the specification, all critical components are treated and final measurement results are given. Base on the design guideline, the critical parameters are calculated and summarized in Table 2.

Table 1. System Specification

Input	
Input Voltage Range	90~264V_{AC}
Line Frequency Range	47~63Hz
Output Voltage of PFC Stage (V_{bulk})	310V / 380V
Output	
Output Voltage (V_o)	12V
Output Power (P_o)	300W
Typical Switching Frequency (f_s)	65kHz

In addition to low-line and light-load condition, V_{bulk} is boosted to 380V. The turn ratio n for of TX_1 is 11, hence the V_{ds} voltage during PWM turn-on period is 380/11=34.55V. According to Equation 4, $Ratio_{LPC2}$ = 1/11.5. The divided voltage on LPC2 is 3.00V. According to Equation 3, the plateau divided voltage on LPC1 during PWM turn-off period should be between 3V~5V. Select $Ratio_{LPC2}$ = 1/7.8, then the divided voltage is 4.43V. Select R_9 = 10kΩ and R_8 = 105kΩ, then R_7 = 10kΩ and R_6 = 68kΩ. Under low-line and light-load condition, V_{bulk} is decreased to 310V. The divided voltage on LPC2 is 2.45V, while the divided voltage on LPC1 is 3.61V.

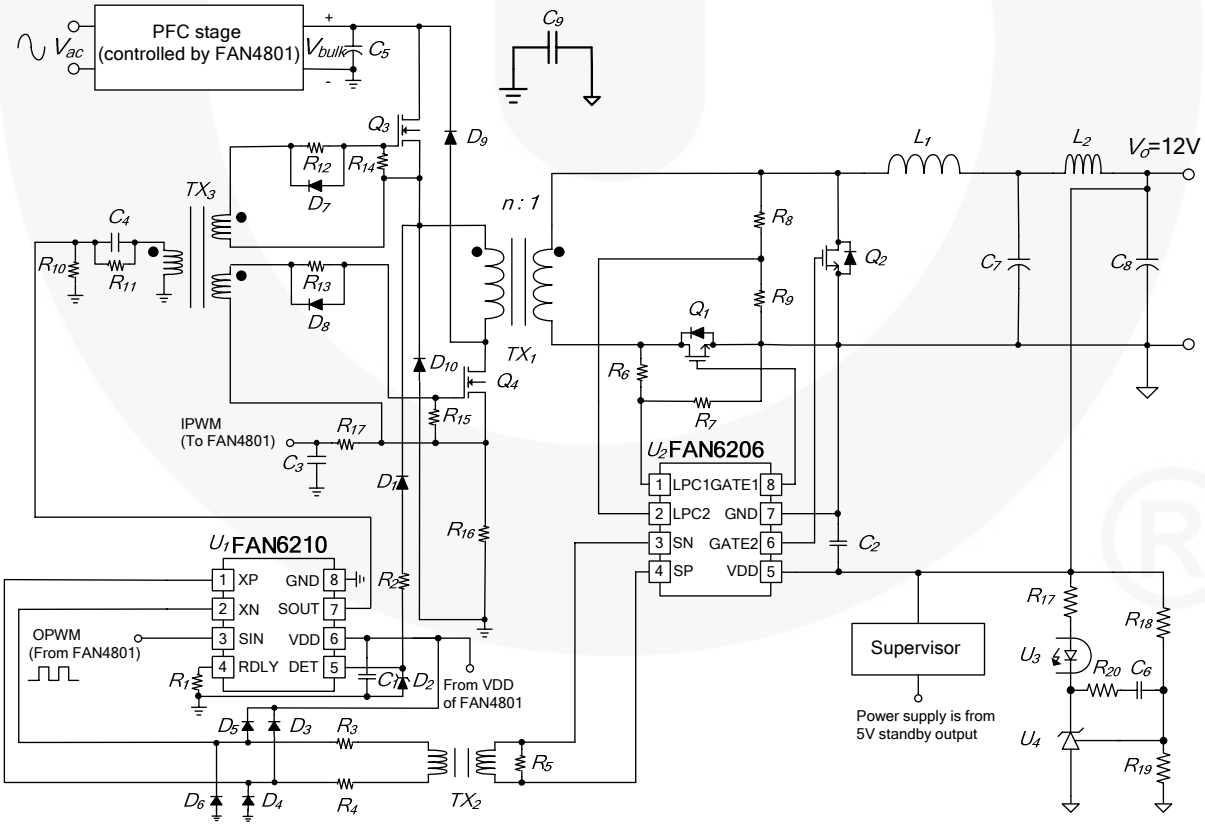

Figure 13.Complete Circuit Diagram

Table 2. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R_1	8.2kΩ	1/8W	L_1	73μH	
R_2	10kΩ	1/4W	L_2	1.8μH	
R_3	10Ω	1/8W	**Diode**		
R_4	10Ω	1/8W	D_1	FR107	
R_5	2kΩ	1/8W	D_2	Zenor Diode/5.6V	
R_6	68kΩ	1/8W	D_3	1N4148	
R_7	10kΩ	1/8W	D_4	1N4148	
R_8	105kΩ	1/8W	D_5	1N4148	
R_9	10kΩ	1/8W	D_6	1N4148	
R_{10}	10kΩ	1/8W	D_7	1N4148	
R_{11}	10kΩ	1/8W	D_8	1N4148	
R_{12}	4.7Ω	1/8W	D_9	UF1007	
R_{13}	4.7Ω	1/8W	D_{10}	UF1007	
R_{14}	10kΩ	1/8W	**MOSFET**		
R_{15}	10kΩ	1/8W	Q_1	FDP5800	
R_{16}	0.15Ω	2W	Q_2	FDP5800	
R_{17}	3kΩ	1/8W	Q_3	FCP20N60	
R_{18}	38.3kΩ	1/8W	Q_4	FCP20N60	
R_{19}	10kΩ	1/8W	**Transformer**		
R_{20}	1kΩ	1/8W	TX_1	66:6	Primary 20mH
Capacitor			TX_2	1:1	Primary 160μH
C_1	100nF	50V	TX_3	1:1.2	Primary 300μH
C_2	100nF	50V	**IC**		
C_3	470pF	25V	U_1	FAN6210	
C_4	100nF	50V	U_2	FAN6206	
C_5	270μF	450V	U_3	PC817	
C_6	1μF	50V	U_4	TL431	
C_7	3300μF	16V			
C_8	3300μF	16V			
C_9	4.7nF/250V	Y-Capacitor			

Figure 14 and Figure 16 show the example design waveform. Figure 14 shows the typical SR driving signals and SR control signal SP-SN under CCM operation. Figure 16 shows that the freewheeling SR is turned off by the LPC mechanism under DCM operation.

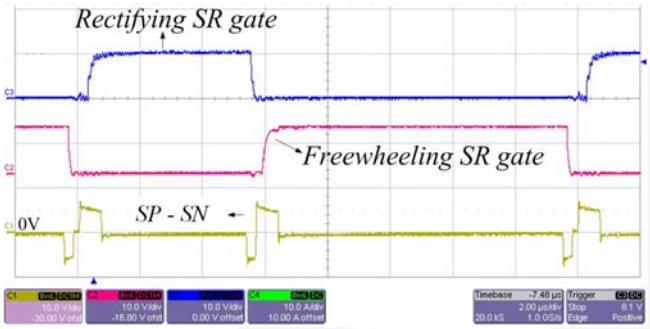

Figure 14. SR Gate is Driven by Primary-Side Control Signal Under CCM Operation

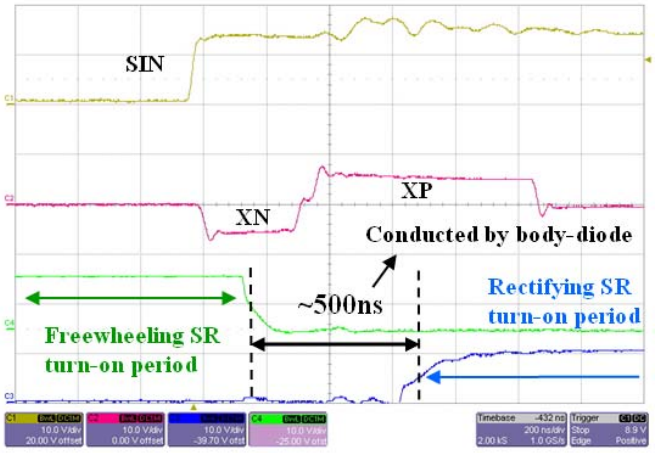

Figure 15. SIN Signal (Rising Edge) and SR Control Signal

Table 3. Efficiency Measurements at V_{AC}=115V on 300W PC Power with Schottky Diodes (FYP2006DN)

Load	Input Watts(W)	Output Watts(W)	Efficiency
100%	357.98	305.42	85.31%
50%	174.21	152.56	87.57%
20%	70.84	70.84	85.95%

Figure 15 and Figure 17 shows the SIN signal of FAN6210 and SR control signals of FAN6206 together. The efficiency test results are shown in Table 3 and Table 4. The significant difference between the SR MOSFET and the Schottky diode is shown in Table 4.

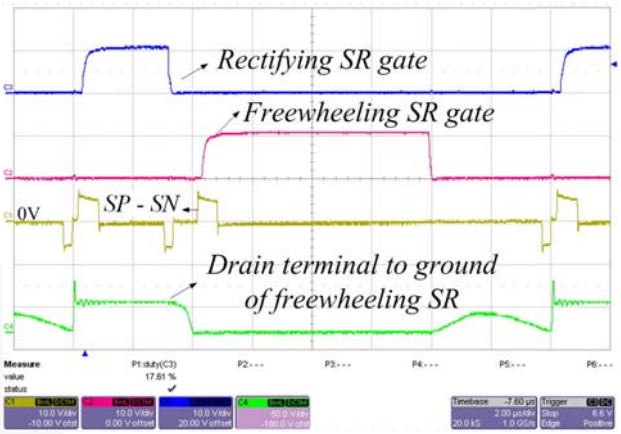

Figure 16. Freewheeling SR is Turned Off by LPC Mechanism Under DCM Operation

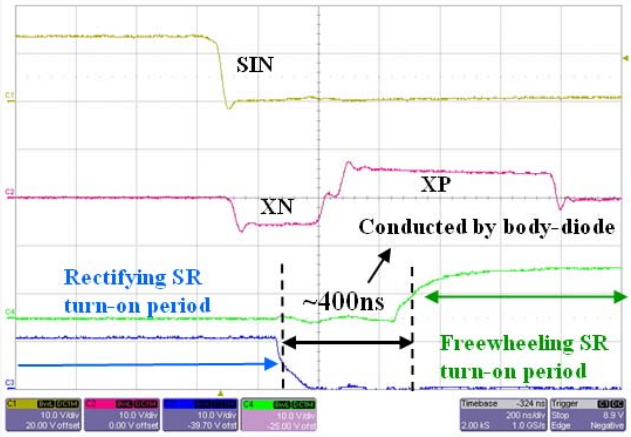

Figure 17.SIN Signal (Falling Edge) and SR Control Signal

Table 4. Efficiency Measurements at V_{AC}=115V on 300W PC Power with SRs (FDP5800)

Load	Input Watts (W)	Output Watts (W)	Efficiency	Vs. Schottky Diode
100%	347.02	305.43	88.01%	+2.70%
50%	169.75	152.69	89.94%	+2.40%
20%	69.24	61.04	88.15%	+2.20%

Related Resources

FAN6210 — Primary-Side Synchronous Rectifier (SR) Trigger Controller for Dual Forward Converter

FAN6206 — Highly Integrated Dual-Channel Synchronous Rectification Controller for Dual-Forward Converter

FAN4801 — PFC/PWM Controller Combination

FAN6751MR — Highly Integrated Green-Mode PWM Controller

SG6520 — PC Power Supply Supervisors

FDP5800 — N-Channel Logic Level PowerTrench® MOSFET 60V,80A, 6mΩ

FCP20N60 / FCPF20N60 — 600V N-Channel MOSFET

1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 — Small Signal Diode

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