# ON Semiconductor

# Is Now

**To learn more about onsemi™, please visit our website at**
**www.onsemi.com**

# AN-6103/D

# PCB Routing Methodology for SuperSpeed USB 3.1 Switch Family from ON Semiconductor

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

### Introduction

The introduction of USB Type−C has provided a significant launch opportunity for USB3.1 data rates across an array of platforms from portable to desktop and beyond. This proliferation of Type−C will certainly create challenges due to the high speed nature of the interface. High Speed USB2.0 presented enough of a system design challenge for tiny mobile device OEM's trying to pass USB eye compliance. A 10X or even 20X increase in data rates will propagate that challenge far beyond the issues that were raised with HS. PCB traces in these systems must be treated as sensitive transmission lines where low-loss impedance control is king. Every effort must be made to make these paths as ideal as possible to prevent signal loss and unwanted emissions that could infect other systems in the device.

The parameters that make a transmission line ideal are typically at odds with system designers that have many other variables to consider such as component placement, thermal dissipation and radio frequency concerns associated with wireless technologies. Also, the expertise of the person or persons making the decisions about system design may not be well educated in the art of controlling high frequency phenomenon. The priority of SuperSpeed circuits must be near the front of the line when laying out a system. This usually involves physically placing the associated components close in proximity using high quality, well controlled transmission lines that don't traverse PCB's with connectors and/or flex cables. If these rules are not followed additional circuitry such as re-drivers or re-clocking devices may be required, increasing the cost and complexity of the system.

High Speed USB has only two signals that need high frequency consideration, DP and DM. With only one pair the routing and placement of the PCB components and traces are relatively straight forward. SuperSpeed has four pairs of signals due to the duplex nature of the interface and the reversibility of the Type−C connector. Add to that a connector footprint that has not 5 but 24 pins to deal with. With this connector pad density the board designer is forced to route these SuperSpeed pairs on buried layers to avoid other components and crossing of other traces. This requires the use of vias in the transmission lines which will and add discontinuities to the path (in many other cases high speed traces could have been routed on surface layers without having to add vias). There are many considerations and rules that can be followed to minimize the parasitic effects of poor impedance control. This paper describes some of these methods.

### Procedure

The following is a typical list of parameters that affects the transmission line quality in a high frequency system:

1. *PCB Material* – There are an array of choices available for high frequency PCB construction. Standard FR4 is the material of choice for the vast majority of electronic systems worldwide. Cost is a significant factor in any consumer-driven device so there is reluctance to upgrade the PCB material, manufacturers will look for other ways to improve performance.
2. *Transmission Line Structure* – There are many styles of transmission line structure that can provide a controlled impedance path. The choice of structure may be dictated by board stack up, space availability or EMI related concerns. Typically these critical traces are not routed by auto routers and can be done manually.
3. *Trace Width* – The width of the trace can have a role in impedance control typically when the pad of a component is sized differently than the width of the carefully calculated trace width. Sometimes it's good practice to size the trace width close to the device pads it will be connecting to. This may be difficult because the dielectric thickness requirements may prohibit this.
4. *Layer Location and Vias* – Where in the stack up can be important for high speed transmission lines as their associated via construction can affect impedance. There are techniques to avoid transmission line stubs associated with through-vias.
5. *Trace Length* – Even well controlled transmission lines have parasitic losses associated with the capacitance, inductance and resistance of the trace. This is especially true when using lossy substrates such as FR4. Components associated with SuperSpeed should be co-located to minimize these losses.



September, 2017 − Rev. 2

Publication Order Number:
AN−6103/D

6. *Connectors* – Even coaxial or controlled impedance connectors have discontinuities and should be avoided if possible. In mobile systems these are usually paired with flex cable assemblies for the freedom of component placement.
7. *Sensitive Circuits* – SuperSpeed transmission lines should be shielded from other sensitive circuits to avoid unwanted crosstalk or emissions. This is sometimes difficult to do in mobile system design.

There has been a lot written on the subject of high speed PCB layout and there are lots of tools available to assist in the process of board design. The most basic tool available is the PCB trace impedance calculator. There are many available online and for purchase. We use a product from Polar Instruments called ‘Polar Instruments Si8000 Quick Solver’. This product provides vital information about impedance based on board stack up, trace geometries and board material. It has many popular trace structures to choose from that will suit almost any application.

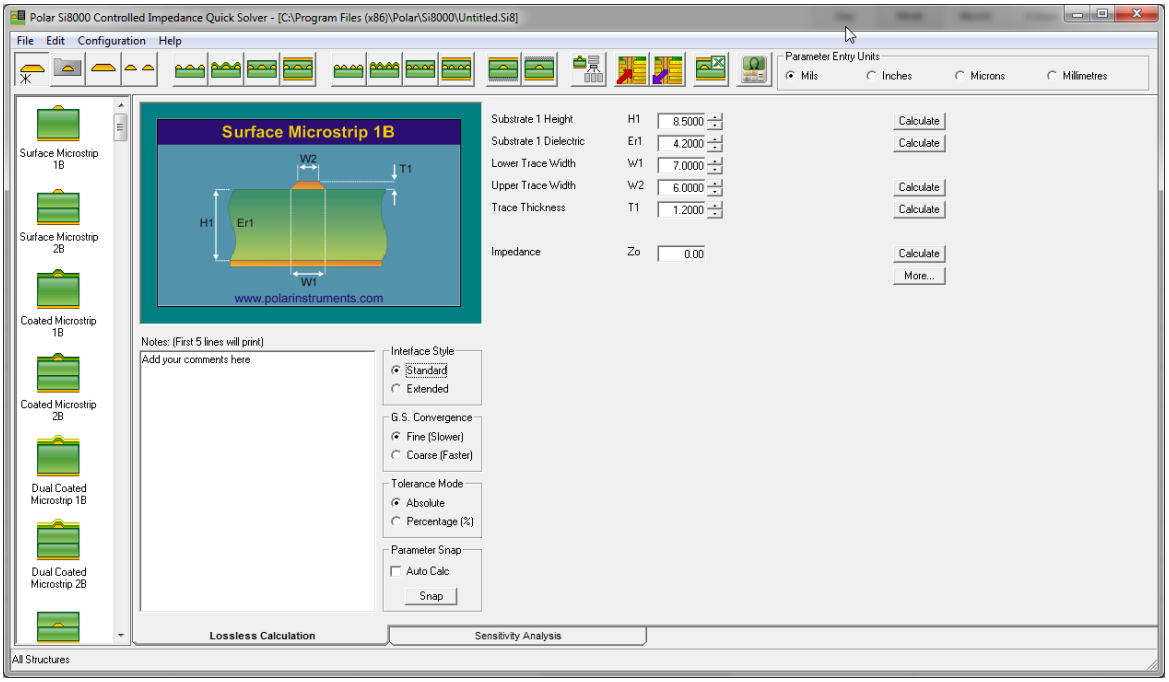


**Figure 1. Pi8000 Basic Menu**

As mentioned earlier there are many types of structures from which to choose. The two shown below are commonly used for differential routes in mobile device PCB’s. The choice of one over the other may depend on the routing density or other system-design related issues. The broadside approach works well with manual routing because it is easy to maintain differential trace lengths (one is on top of the other). The edge-coupled may be better suited for some designs due to stack up or layer availability. The main menu in the program has many entry boxes to enter specifics about the transmission line structure, including the dielectric constant $e_r$. The dielectric constant will be dependent on the PCB material, typically FR4 with a value from 4.2 to 4.5 depending on manufacturer. These variables can be modulated to experiment with various dimensions to suit the particular application need.

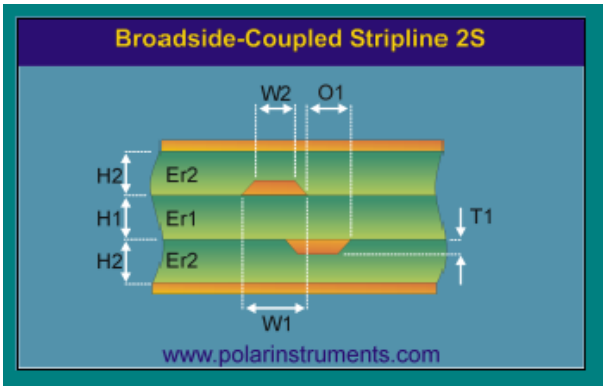


**Figure 2. Boardside Coupled Approach**

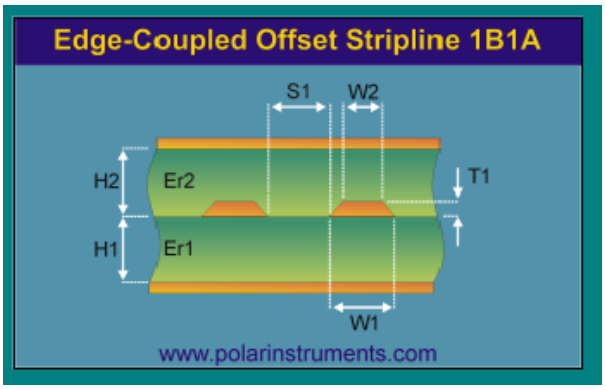


**Figure 3. Edge Coupled Approach**

For additional noise isolation and geometric options for impedance control, grounds may be included in the structures in a co-planar waveguide fashion as shown in the example above. The choice of structure sometimes comes down to what impedance can be maintained in a limited stack up situation. In many systems the PCB needs many layers but the overall thickness can't exceed a certain height (such as in a cellular telephone). Trade-offs must sometimes be made with trace width, dielectric thickness or relieving of metal on adjacent layers to compensate for additional needed thickness above or below the trace (as shown in the 2B2A example).

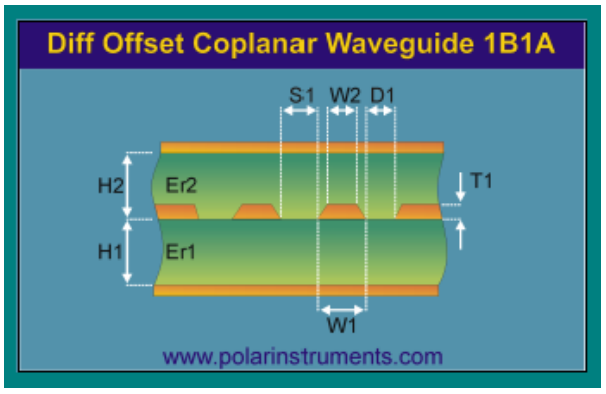


**Figure 4. Waveguide 1B1A Example**

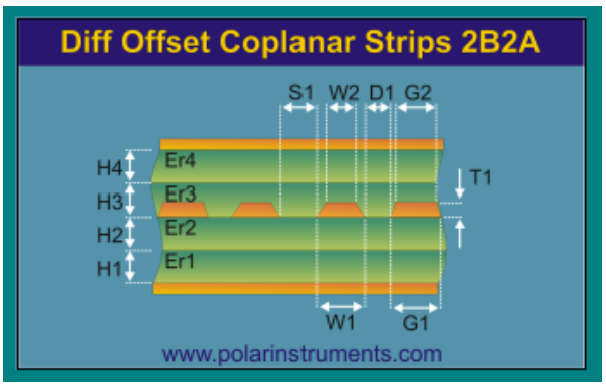


**Figure 5. Strips 2B2A Example**

For SuperSpeed USB the transmission line structure of choice is coupled differential. There are many forms of this structure based on board stackup, dielectric thickness, and how ground relates to the structure. For differential trace structures it is imperative that both traces in the differential pair maintain the same impedance and the same trace length. Changing trace direction and how the traces interact with adjacent signals is also a critical consideration with high speed signaling. Again, refer to the following illustrations from the USB−IF:

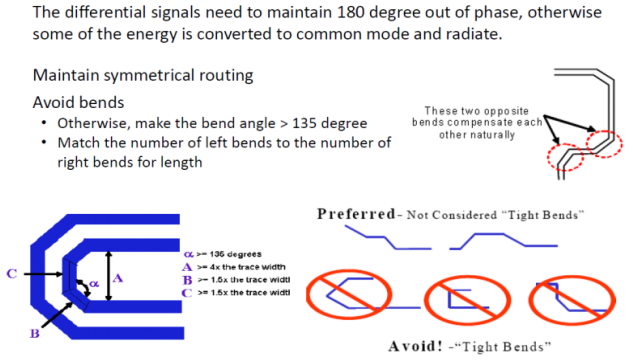


**Figure 6. Bending Rules**

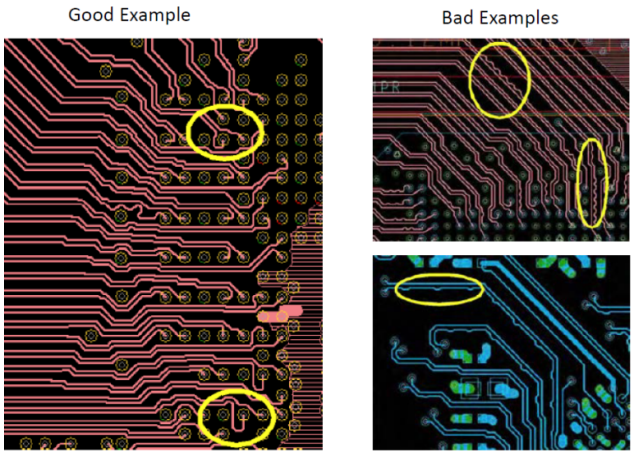


**Figure 7. Length Matching and Compensation**

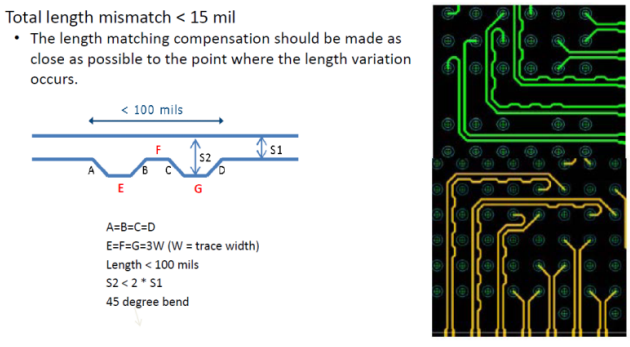


**Figure 8. Serpentine Routing Routine**

Another important factor in high speed system design is knowing how much loss can be tolerated in the system. For USB3.1 the USB−IF has specified the amount of loss that can be expected in the USB3.1 channel. The following diagrams are taken from the USB−IF presentation on system design:

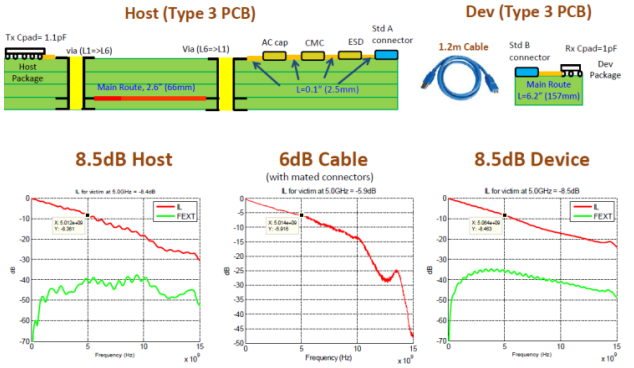


**Figure 9. USB−IF Specific Channel Lesses (23 dB Reference Channel Loss, Symmetric)**

In these cases the amount of loss is specified from the pin of the transmitting signal IC, across whatever board PCB traces, vias, connectors, etc. to the external cable to the receiving device with the same PCB, connector, etc. Having these defined quantities should be a good indicator of a board simulation or actual measurement to determine how your design will work in an end system.

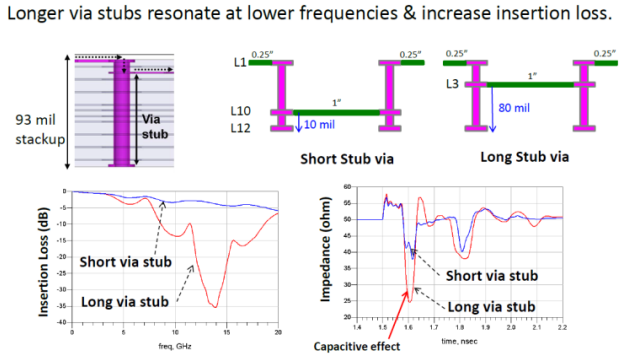


**Figure 10. PCB: Via Stub Discontinuity**

As seen in the Figure 10 the way in which vias are implemented can have a varying effect on the amount of discontinuity on the transmission line. Another approach in addition to the methods mentioned above are blind vias where they don't penetrate the entire board thickness, rather just the layers they're connected to. This method produces no stub:

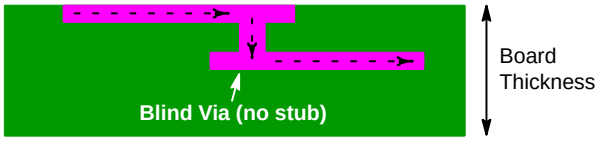


**Figure 11. Method Producing No Stub**

Crosstalk is another major concern for high speed systems. There are methods of routing that are better for reducing crosstalk, both near-end (NEXT) and far-end (FEXT). The illustrations below show some of the effects/benefits of layout techniques:

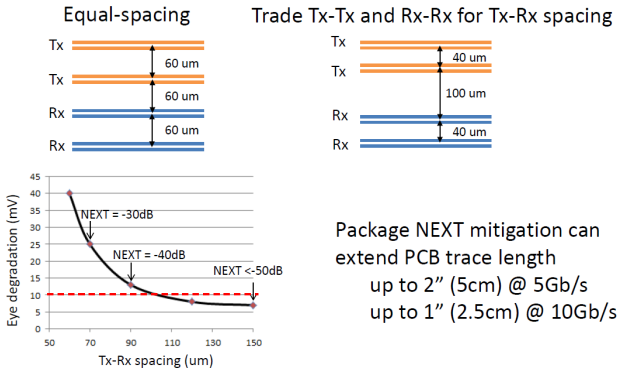


**Figure 12. Packages: NEXT Mitigation in Main Route**

- The interleaved (Tx-Rx-Tx-Rx) PCB main route reduces FEXT.
- 5Gb/s margin improvement:
  - 4" PCB (with internal cable): 10mV, 5ps
  - 10" PCB: 13mV, 12ps

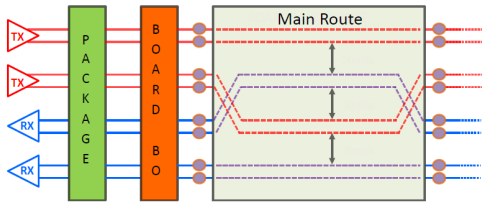


**Figure 13. PCB Further FEXT Mitigation in Main Route**

## Applications

- Smart Phones
- Tablets
- Notebooks
- Hard Drives
- Power Banks
- Routers
- Flash

## Protocols Supported

- USB 3.1 SuperSpeed (Gen 2), 10 Gbps
- PCI Express, Gen 3
- SATA
- Fibre Channel
- Display Port 1.3

## References

[1] USB 3.1 Developer Days Seminar Day 1 20140915.pdf
[2] USB 3.1 Developer Days Seminar Day 2 MECH 20140916.pdf
[3] Polar Instruments Si8000 Quick Solver

## Related Product Information

- *http://www.onsemi.com/PowerSolutions/parametrics.do?id=17642*
- *http://www.onsemi.com/PowerSolutions/product.do?id=FUSB340*



**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5817−1050

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative