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AN-6086

Design Consideration for Interleaved Boundary Conduction Mode PFC Using FAN9611/12

1. Introduction

This application note presents practical step-by-step design considerations for an interleaved Boundary-Conduction-Mode (BCM) Power-Factor-Correction (PFC) converter employing Fairchild PFC controllers FAN9611 and FAN9612. It includes designing the inductor and Zero-Current-Detection (ZCD) circuit, selecting the components, and closing the control loop. The design procedure is verified through an experimental 400W prototype converter.

The FAN9611/12 interleaved dual BCM PFC controller operates two parallel-connected boost power trains 180º out of phase, extending the maximum practical power level of this control technique from 200-300W to greater than 800W. Unlike the Continuous Conduction Mode (CCM) technique often used at this power level, BCM offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. Furthermore, the input and output filters can be made smaller due to ripple cancellation between the power stages and the effective doubling of the switching frequency. The advanced line feed-forward with peak detection circuit minimizes the output voltage variation during line transients. To guarantee stable operation with less switching loss at light load, the maximum switching frequency is clamped at 525kHz. Interleaved synchronization is maintained under all operating conditions. Protection functions include output over-voltage, over-current, open-feedback, under-voltage lockout, brownout protection, and secondary latching over-voltage protection.

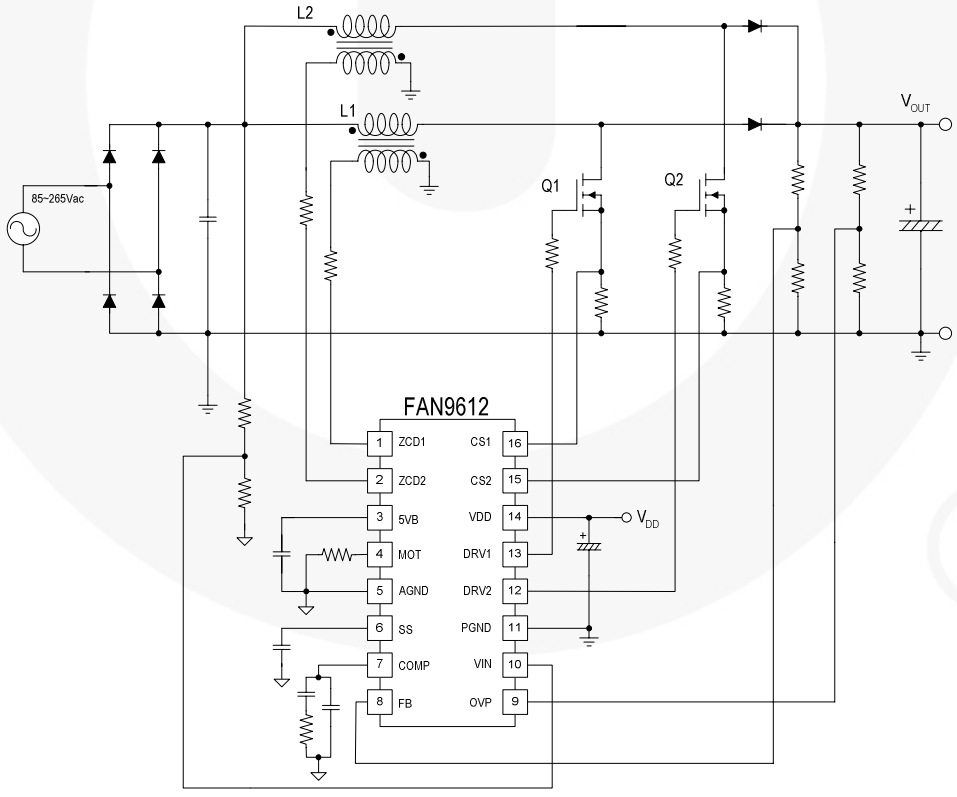


Figure 1. Typical Application Circuit of FAN9611 or FAN9612

2. Operation Principle of BCM Boost PFC Converter

The most widely used operation modes for the boost converter are the continuous conduction mode (CCM) and the boundary conduction mode (BCM). These two descriptive names refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. As the names indicate, the inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. Even though the BCM operation has higher RMS current in the inductor and switching devices, it allows better switching condition for the MOSFET and the diode. As shown in Figure 2, the diode reverse recovery is eliminated and a fast recovery diode is not needed. MOSFET is also turned on with zero current, which reduces the switching loss.

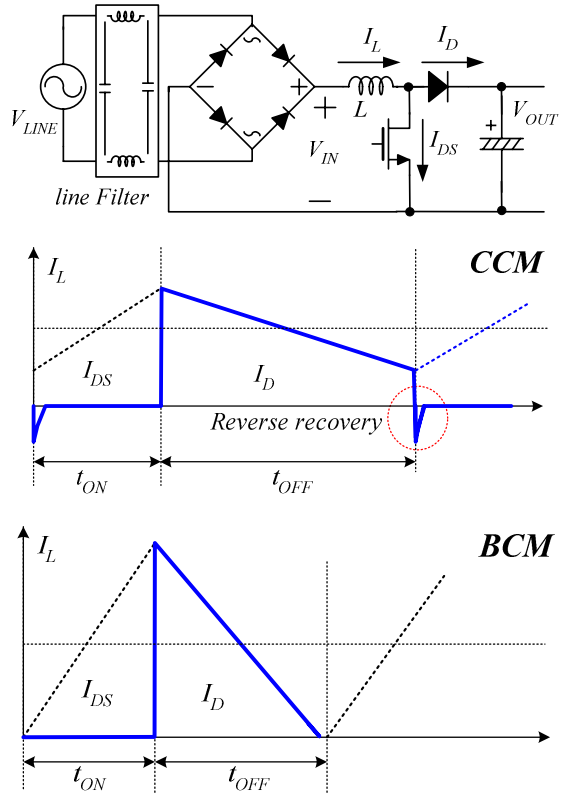


Figure 2. CCM vs. BCM Control

The fundamental idea of BCM PFC is that the inductor current starts from zero in each switching period, as shown in Figure 3. When the power transistor of the boost converter is turned on for a fixed time, the peak inductor current is proportional to the input voltage. Furthermore, since the current waveform is triangular, the average value in each switching period is also proportional to the input voltage. In the case of a sinusoidal input voltage, the input current of the converter follows the input voltage waveform with a very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation an ideal candidate for power factor correction.

A by-product of the BCM is that the boost converter runs with variable switching frequency that depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input current follows the sinusoidal input voltage waveform, as shown in Figure 3. The lowest frequency occurs at the peak of sinusoidal line voltage.

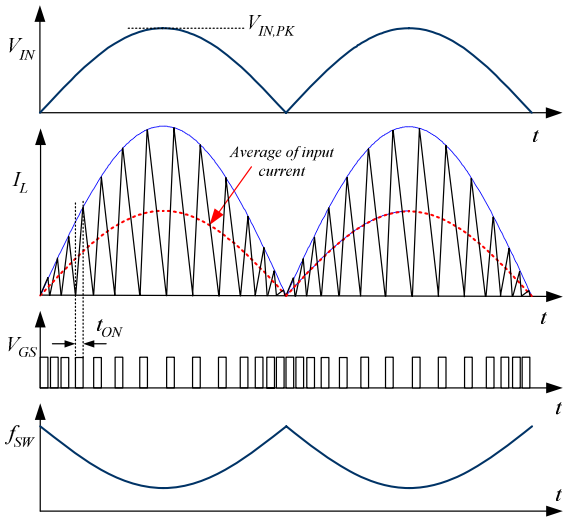


Figure 3. Operation Waveforms of BCM PFC

The voltage-second balance equation for the inductor is:

$$V_{IN}(t)\cdot t_{ON} = (V_{OUT} - V_{IN}(t))\cdot t_{OFF} \quad (1)$$

where $V_{IN}(t)$ is the rectified line voltage.

The switching frequency of BCM boost PFC converter is obtained as:

$$f_{SW} = \frac{1}{t_{ON}+t_{OFF}} = \frac{1}{t_{ON}}\cdot\frac{V_{OUT}-V_{IN}(t)}{V_{OUT}} = \frac{1}{t_{ON}}\cdot\frac{V_{OUT}-V_{IN,PK}\cdot|\sin(2\pi f_{LINE}t)|}{V_{OUT}} \quad (2)$$

where $V_{IN,PK}$ is the amplitude of the line voltage and f_{LINE} is the line frequency.

Figure 4 shows how the MOSFET on time and switching frequency changes as output power decreases. When the load decreases, as shown in the right side of Figure 4, the peak inductor current diminishes with reduced MOSFET on time and, therefore, the switching frequency increases. Since this can cause severe switching losses at light load condition, the maximum switching frequency of FAN9611/12 is limited to 525kHz.

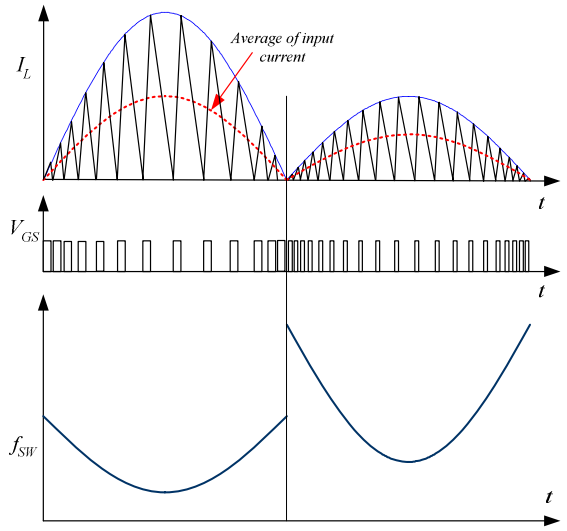


Figure 4. Frequency Variation of BCM PFC

Since the design of filter and inductor for a BCM PFC converter with variable switching frequency should be done at minimum frequency condition, it is worthwhile to examine how the minimum frequency of BCM PFC converter changes with operating conditions.

Figure 5 shows the minimum switching frequency, which occurs at the peak of line voltage, as a function of the RMS line voltage for three output voltage settings. It is interesting to note that, depending on where the output voltage is set, the minimum switching frequency may occur at the minimum or at the maximum line voltage. When the output voltage is approximately 405V, the minimum switching frequency is the same for both low line ($85V_{AC}$) and high line ($265V_{AC}$).

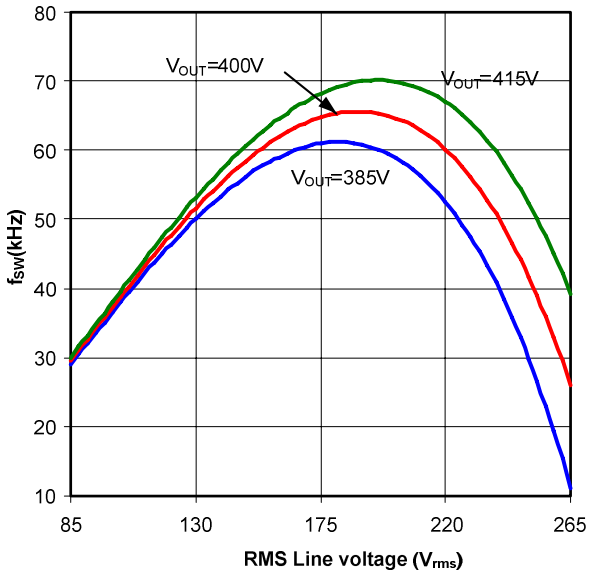


Figure 5. Minimum Switching Frequency vs. RMS Line Voltage (L = 390µH, P_{OUT} = 200W)

3. Interleaving of BCM Boost PFC

One important characteristic of a BCM boost converter is the high ripple current of the boost inductor, which goes from zero to a controlled peak value in every switching period. Accordingly, the power switch is also stressed with high peak currents. In addition, the high ripple current must be filtered by an EMI filter to meet high-frequency noise regulations enforced for equipment connected to the mains. These effects usually limit the practical output power level of the converter below 300W. However, operating two parallel-connected boost power stages 180º out of phase, as shown in Figure 6; the high peak current and over-sized EMI filter problems are solved, extending the maximum practical power level of this control technique to greater than 800W. This technique is called interleaving.

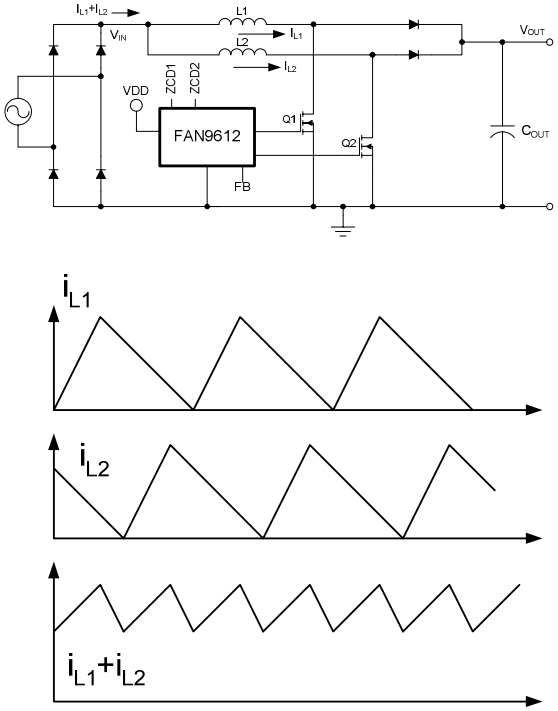


Figure 6. Interleaving Operation of BCM Boost PFC

Interleaving operation provides many advantages over the single BCM PFC operation. The losses are distributed in the switching devices, which also spreads the dissipated power and eases the thermal management of the power stage design. Interleaving also yields great benefits on EMI filter size reduction since the effective switching frequency seen at the input side of the converter is doubled, while the combined ripple current is minimized due to the ripple current cancellation, as shown in the waveforms of Figure 6.

4. Design Considerations

In this section, a design procedure is presented using the schematic in Figure 7 as a reference. A 400W PFC application with universal input range is selected as a design example. The design specifications are as follows:

- Line voltage range: 85~265V_{AC} (universal input), 50Hz
- Nominal output voltage and current: 400V/1A (400W)
- Holdup time requirement: Output voltage should not drop below 330V during one line cycle
- Output voltage ripple: less than 8V_{p-p}
- Minimum switching frequency: higher than 50kHz
- Control Bandwidth: 5~10Hz
- Brownout protection line voltage: 70V_{AC}

The design is for two identical converters, which deliver half of the total output power (200W), respectively. V_{DD} is assumed to be supplied from auxiliary power supply.

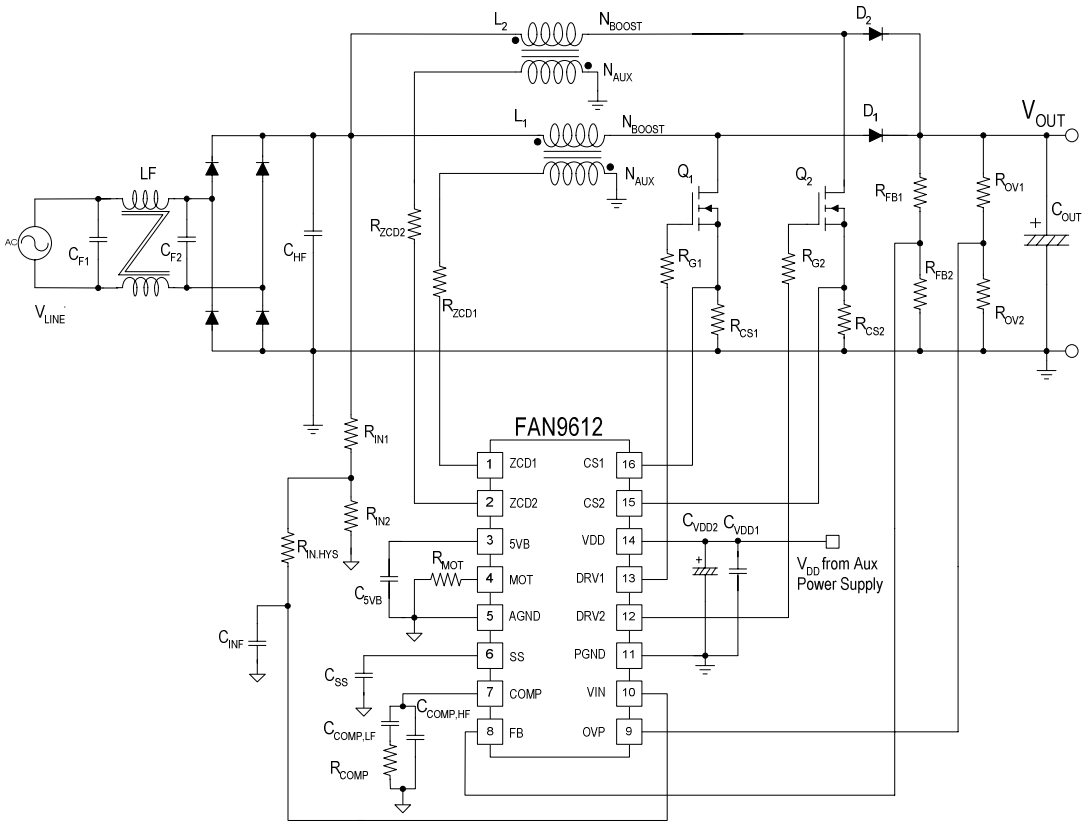


Figure 7. Reference Circuit for Design Example of Interleaving BCM Boost PFC

[STEP-1] Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. From Equation 2, the minimum frequency with a given line voltage and MOSFET on time is obtained as:

$$f_{SW,MIN} = \frac{1}{t_{ON}} \cdot \frac{V_{OUT} - \sqrt{2}V_{LINE}}{V_{OUT}} \tag{3}$$

where:
V_{LINE} is RMS line voltage;
t_{ON} is the MOSFET conduction time; and
V_{OUT} is the output voltage.

The MOSFET conduction time with a given line voltage at a nominal output power is given as:

$$t_{ON} = \frac{2 \cdot P_{OUT,CH} \cdot L}{\eta \cdot V_{LINE}^{\ 2}} \tag{4}$$

where:
η is the efficiency;
L is the boost inductance; and
$P_{OUT,CH}$ is the nominal output power per channel

Using Equation 4, the minimum switching frequency of Equation 3 can be expressed as:

$$f_{SW,MIN} = \frac{\eta \cdot V_{\mathrm{LINE}}^{\ 2}}{2 \cdot P_{OUT,CH} \cdot L} \cdot \frac{V_{OUT} - \sqrt{2}V_{\mathrm{LINE}}}{V_{OUT}} \tag{5}$$

Therefore, once the output voltage and minimum switching frequency are set, the inductor value is given as:

$$L = \frac{\eta \cdot V_{LINE,MINF}{}^2}{2 \cdot P_{OUT,CH} \cdot f_{SW,MIN}} \cdot \frac{V_{OUT} - \sqrt{2}V_{LINE,MINF}}{V_{OUT}} \quad (6)$$

where $V_{LINE,MINF}$ is the RMS line voltage that results in minimum switching frequency.

For universal input range, $V_{LINE,MINF}$ is the maximum line voltage ($265V_{AC}$) when V_{OUT} is set at lower than 405V; while $V_{LINE,MINF}$ is minimum line voltage ($85V_{AC}$) when V_{OUT} is set at higher than 405V.

As the minimum frequency decreases, the switching loss is reduced, while the inductor size and line filter size increase. Thus, the minimum switching frequency should be determined by the trade-off between efficiency and the size of magnetic components. The minimum switching frequency must be above the minimum frequency of FAN9611/12, which is set at 16.5kHz to prevent audible noise.

Once the inductance value is decided, the maximum peak inductor current at the nominal output power is obtained as:

$$I_{L.PK} = \frac{2\sqrt{2} \cdot P_{OUT,CH}}{\eta \cdot V_{LINE,MIN}} \quad (7)$$

where $V_{LINE,MIN}$ is the minimum line voltage.

The number of turns of boost inductor should be determined considering the core saturation. The minimum number is given as:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L}{A_e \cdot \Delta B} \quad (8)$$

where is A_e is the cross-sectional area of core and ΔB is the maximum flux swing of the core in Tesla. ΔB should be set below the saturation flux density.

Figure 8 shows the typical B-H characteristics of ferrite core from TDK (PC45). Since the saturation flux density (ΔB) decreases as the temperature increases, the high temperature characteristics should be considered.

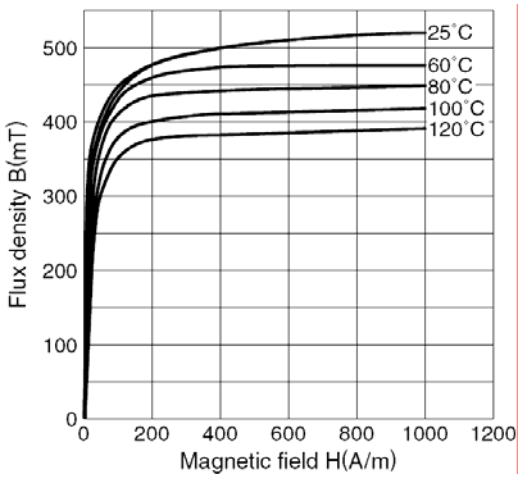


Figure 8. Typical B-H Curves of Ferrite Core

(Design Example) Since the output voltage is 400V, the minimum frequency occurs at high-line ($265V_{AC}$) and full-load condition. Assuming the efficiency is 95% and selecting the minimum frequency as 52kHz, the inductor value is obtained as:

$$L = \frac{\eta \cdot V_{LINE,MINF}{}^2}{2 \cdot P_{OUT,CH} \cdot f_{SW,MIN}} \cdot \frac{V_{OUT} - \sqrt{2}V_{LINE,MINF}}{V_{OUT}}$$

$$= \frac{0.95 \cdot 265^2}{2 \cdot 200 \cdot 52 \times 10^3} \cdot \frac{400 - \sqrt{2} \cdot 265}{400} = 202\mu H$$

The maximum peak inductor current at nominal output power is calculated as:

$$I_{L,PK} = \frac{2\sqrt{2} \cdot P_{OUT,CH}}{\eta \cdot V_{LINE,MIN}} = \frac{2\sqrt{2} \cdot 200}{0.95 \cdot 85} = 7A$$

Assuming PQ3230 core (PC45, A_e=161mm^2) is used and setting ΔB as 0.3T, the primary winding should be:

$$N_{BOOST} \geq \frac{I_{L,PK} \cdot L}{A_e \cdot \Delta B} = \frac{7 \cdot 202 \times 10^{-6}}{161 \times 10^{-6} \cdot 0.3} = 29 turns$$

Thus, the number of turns (N_{BOOST}) of boost inductor is determined as 30 turns.

[STEP-2] Inductor Auxiliary Winding Design

Figure 9 shows the inductor current and voltage waveforms of a BCM boost converter. FAN9611/12 indirectly detects the inductor zero current point using an auxiliary winding of the boost inductor. Since the zero current detection (ZCD) circuit in FAN9611/12 is designed to turn on the MOSFET when the slope of auxiliary winding voltage becomes zero, no special consideration for timing delay is required for the auxiliary winding design.

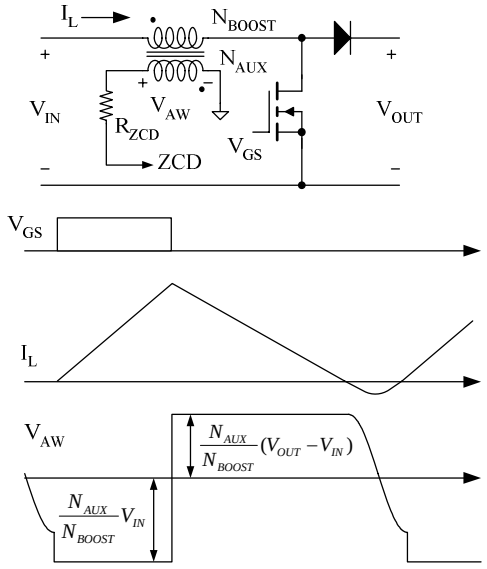


Figure 9. ZCD Detection Waveforms

The voltage of the ZCD pin is clamped near zero and the resistor R_{ZCD} limits the current of the ZCD pin below 1mA as:

$$R_{ZCD} > \frac{V_{OUT}}{1mA} \cdot \frac{N_{AUX}}{N_{BOOST}} \quad (9)$$

For low-power applications, such as adaptors, the supply voltage (V_{DD}) for FAN9611/12 is supplied by auxiliary winding of inductor, as shown in Figure 10. Since the auxiliary winding voltage varies extensively within half of line cycle, DC blocking capacitor (C_B) is used to guarantee stable V_{DD} voltage.

When supplying V_{DD} using the auxiliary winding, the turns ratio should be determined as:

$$N = \frac{N_{BOOST}}{N_{AUX}} \cong \frac{V_{OUT}}{2V_Z} \quad (10)$$

where V_Z is the Zener diode voltage for V_{DD}.

The reason for setting the turns ratio such that peak-to-peak voltage of auxiliary winding is around twice of V_Z is to guarantee stable V_{DD} supply without under-voltage lockout (UVLO) during startup.

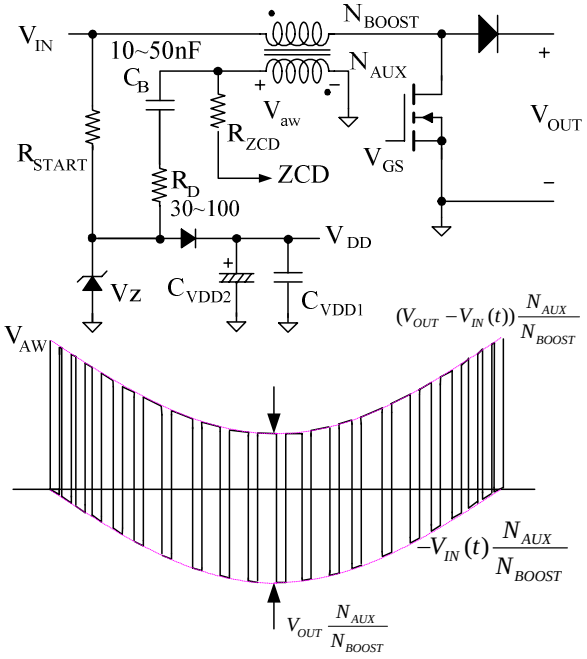


Figure 10. V_{DD} Supply Circuit using Auxiliary Winding

The average current through the startup resistor should be larger than the startup current (100μA), determined as:

$$I_{START} = \frac{2\sqrt{2}V_{LINE,MIN}}{\pi R_{START}} > 100\mu A \quad (11)$$

The startup resistor also should be determined by considering the minimum startup time, which is given as:

$$t_{START} = \frac{V_{ON}C_{DD}}{(\frac{2\sqrt{2}V_{LINE,MIN}}{\pi R_{START}} - 100\mu A)} \quad (12)$$

where V_{ON} is UVLO start voltage for V_{DD} and C_{DD} is the total capacitance of capacitors connected to the V_{DD} pin.

Typically 20~50μF of electrolytic capacitor (C_{VDD2}) is used together with 2~4μF of bypass capacitor (C_{VDD1}).

The power consumption in the startup resistor is obtained as:

$$P_{LOSS} = \frac{V_{LINE,MAX}^{\ 2}}{R_{START}} \quad (13)$$

(Design Example) Selecting the turns ratio of the inductor (N_{BOOST}/N_{AUX}) as 10, N_{AUX} is obtained as 3 and the value of R_{ZCD} is given as:

$$R_{ZCD} > \frac{V_{OUT}}{1mA} \cdot \frac{N_{AUX}}{N_{BOOST}} = \frac{400}{1mA} \cdot \frac{3}{30} = 40k\Omega$$

R_{ZCD} is selected as 47kΩ.

Assuming that V_{DD} is supplied from auxiliary power supply, V_{DD} supply circuit using the auxiliary winding is not included in this example.

[STEP-3] Design V_{IN} Sense Circuit

Since the RMS value of AC line voltage is directly proportional to the peak of the line voltage, FAN9611/12 detects the peak value of input voltage to sense the RMS value of the line voltage, which permits a simple voltage divider for line voltage sensing, as shown in Figure 11. The detected line voltage information is used for line under-voltage lockout (UVLO), and line feed-forward for PWM control.

When the peak of V_{IN} pin voltage drops below 0.95V, the line UVLO (brownout protection) is triggered and FAN9611/12 stops operating. The RMS value of the line voltage that causes line UVLO is given as:

$$V_{LINE.UVLO} = \frac{R_{IN1} + R_{IN2}}{R_{IN2}\sqrt{2}} \cdot 0.95 \qquad (V_{AC}) \quad (14)$$

The internal switched current source allows UVLO hysteresis on line voltage as:

$$V_{LINE,HYS} = \frac{R_{IN1} + R_{IN,HYS}(\frac{R_{IN1}}{R_{IN2}} + 1)}{\sqrt{2}} \cdot 2\mu A \ (V_{AC}) \quad (15)$$

From Equation 15, $R_{IN,HYS}$ with a given hysteresis of line voltage is obtained as:

$$R_{IN,HYS} = (\frac{\sqrt{2}V_{LINE.HYS}}{2\mu A} - R_{IN1}) \cdot \frac{R_{IN2}}{R_{IN1} + R_{IN2}} \quad (16)$$

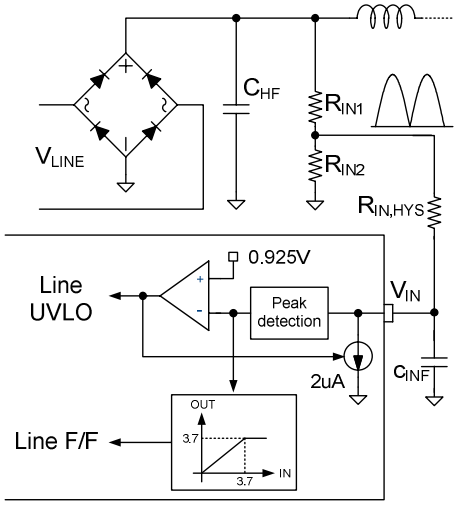


Figure 11. Input Voltage Sensing

The line peak detection circuit is saturated when V_{IN} exceeds 3.7V, as depicted in Figure 11. Therefore, line feedforward does not work for V_{IN} higher than 3.7V, as illustrated in Figure 12. The minimum brownout protection trip point that allows proper line feedforward operation for universal line range is $66V_{AC}$ ($265V_{AC}$×0.925/3.7). When the brownout protection threshold is lower than $68V_{AC}$ for universal range input, line feedforward can be lost for high line and, therefore, the limited output power increases as line voltage increases:

$$P_{OUT}^{MAX.NO.FF} = P_{OUT}^{MAX} \cdot (\frac{V_{IN}}{3.7})^2 \quad (17)$$

Another effect of V_{IN} sensing saturation is that the phase management threshold as a percentage of nominal output power increases as peak of V_{IN} increases above 3.7V because the line feedforward does not work above 3.7V.

Since FAN9611/12 uses peak detection for the line voltage sensing, it is typical to use a small capacitor (C_{INF}) to bypass switching noise. To minimize the effect of sensing delay, the RC time constant between R_{IN2} and C_{INF} should be smaller than 5% of AC line period.

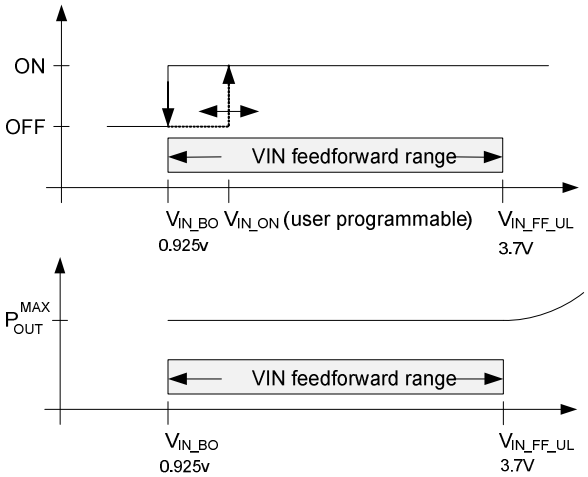


Figure 12. V_{IN} Feedforward Range

(Design Example) Setting the brown-out protection threshold at $70V_{AC}$ and selecting R_{IN1}=2MΩ, R_{IN2} is obtained as:

$$R_{IN2} = \frac{R_{IN1}}{(\sqrt{2}V_{LINE,UVLO}/0.925-1)} = \frac{2\times10^6}{\sqrt{2}\cdot70/0.925-1} = 18.9k\Omega$$

Assuming the hysteresis for brownout protection is $3V_{AC}$, $R_{IN,HYS}$ is obtained as:

$$R_{IN,HYS} = (\frac{\sqrt{2}V_{LINE.HYS}}{2\mu A} - R_{IN1}) \cdot \frac{R_{IN2}}{R_{IN1}+R_{IN2}} = (\frac{\sqrt{2}\cdot3}{2\times10^{-6}} - 2\times10^6) \cdot \frac{18.9\times10^3}{2\times10^6+18.9\times10^3} = 1.1k\Omega$$

$R_{IN.HYS}$ can be omitted since the hysteresis of $2.8V_{AC}$ is obtained without $R_{IN,HYS}$ from Equation 15. C_{INF} is selected as 10nF, which results in RC time constant as:

$$\tau = (R_{IN2}+R_{IN.HYS})\cdot C_{INF} = 18.9\times10^3\cdot10\times10^{-9} = 189\mu s$$

[STEP-4] Determine MOT Pin Resistor

The on time of the gate drive signal is proportional to the compensation voltage as shown in Figure 13. The compensation voltage is internally clamped at 4.3V where the maximum on time is obtained. The Maximum On Time (MOT) of the gate drive signal of each channel is programmed by the resistor on the MOT pin as:

$$t_{ON,MAX} = R_{MOT}\cdot230\times10^{-12}(\frac{R_{IN1}+R_{IN2}}{R_{IN2}\sqrt{2}V_{LINE}})^2 \quad (18)$$

As can be observed in Equation 18, the maximum on time is inversely proportional to the square of line voltage due to the line feed-forward operation.

The MOT resistor should be determined by considering the output power since the maximum on time limits the maximum output power during overload condition as:

$$P_{MAX,CH} = K_{MAX}\cdot P_{OUT,CH} = \frac{V_{LINE}^2\cdot\eta}{2L}t_{ON,MAX} \quad (19)$$

where $P_{MAX,CH}$ is the limited maximum output power per channel and K_{MAX} is maximum power limiting factor, which is a ratio between the limited maximum output power and nominal output power.

Considering the tolerances of inductor, resistor, and controller variation; it is typical to set the limited maximum power as 20~30% higher than the nominal output power (K_{MAX} = 1.2~1.3).

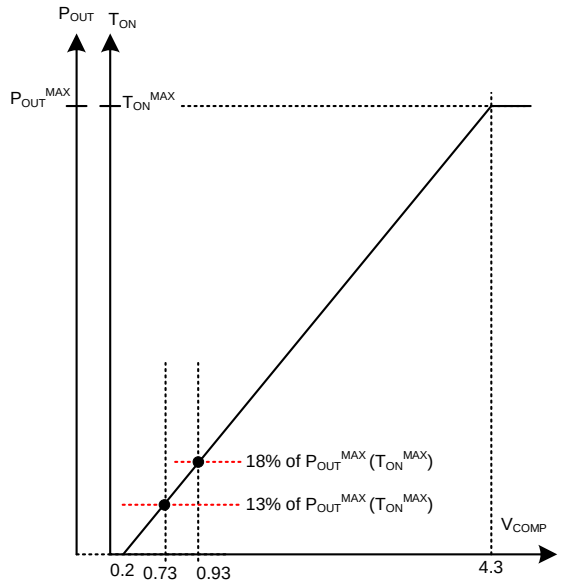


Figure 13. V_{COMP} vs. On Time of Gate Drive Signal

FAN9611/12 determines the phase management according to the COMP pin voltage (0.73V and 0.93V). Since the COMP pin voltage is proportional to the output power, the power levels for phase shedding and adding are given as percentages of limited maximum power, as shown in Figure 13. Thus, the maximum power limiting factor affects the actual phase management thresholds as percentages of nominal output power, as shown in Figure 14, which shows an example where the maximum power limit is 170% of the nominal output power. In that case, the actual phase management thresholds are 22% and 31% of nominal output power, which can maximize the efficiency at 20% of nominal load for 80-plus efficiency requirement. In this way, the phase management thresholds can be adjusted upward by adjusting the maximum on time (through R_{MOT}).

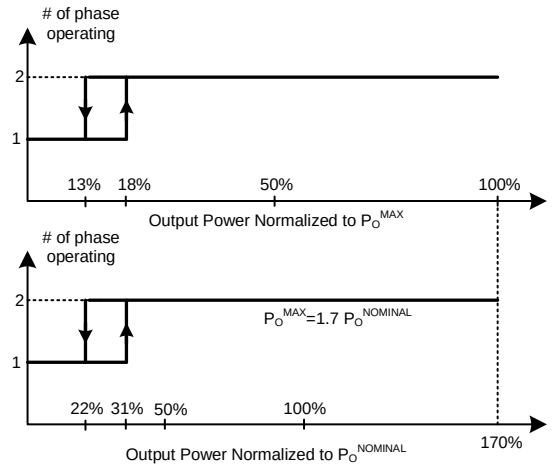
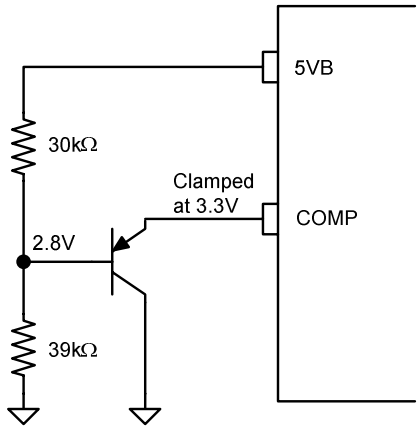


Figure 14. Phase Management Threshold

When the resulting maximum power limit to obtain the desired phase management threshold is too high compared to the nominal output power, the maximum power limit level can be reduced using clamping circuit on COMP pin, as shown in Figure 15. The COMP pin voltage is clamped at 3.3V and the resulting maximum power limit level is reduced from 170% to 130% of nominal output power.



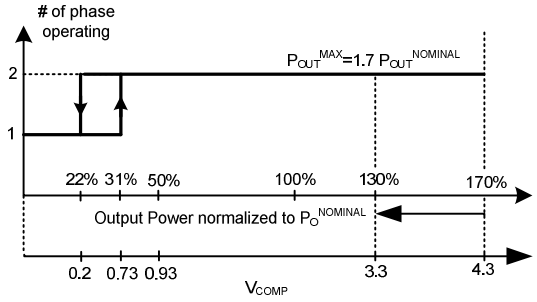


Figure 15. COMP Voltage Clamping Circuit and Phase Management Threshold

After determining the limited maximum output power, the boost inductor maximum flux density should be examined to make sure that the inductor is not saturated during overload condition. The maximum flux density of boost inductor during overload condition is given by:

$$B_{\max} = \frac{I_{L,PK} \cdot K_{MAX} \cdot L}{A_e \cdot N_{BOOST}} \quad (20)$$

(Design Example) Setting the limited output power as 120% of nominal output power, the maximum on time is given as:

$$t_{ON,MAX} = \frac{P_{MAX,CH} \cdot 2L}{V_{LINE,MIN}{}^2 \cdot \eta} = \frac{(K_{MAX} \cdot P_{OUT,CH}) \cdot 2L}{V_{LINE,MIN}{}^2 \cdot \eta}$$
$$= \frac{(1.2 \cdot 200) \cdot 2 \cdot 202 \times 10^{-6}}{85^2 \cdot 0.95} = 14.1\mu s$$

Then, the resistor on MOT pin is obtained as:

$$R_{MOT} = \frac{t_{ON,MAX}}{230 \times 10^{-12}} \left(\frac{R_{IN2}\sqrt{2}V_{LINE,MIN}}{R_{IN1} + R_{IN2}}\right)^2$$
$$= \frac{14.1 \times 10^{-6}}{230 \times 10^{-12}} \left(\frac{18.9 \cdot \sqrt{2} \cdot 85}{18.9 + 2000}\right)^2 = 78k\Omega$$

The maximum flux density during overload condition is obtained as:

$$B_{max} = \frac{I_{L,PK} \cdot K_{MAX} \cdot L}{A_e \cdot N_{BOOST}} = \frac{7 \cdot 1.2 \cdot 202 \times 10^{-6}}{161 \times 10^{-6} \cdot 30}$$
$$= 0.35\ tesla$$

[STEP-5] Design Feedback Circuit

To regulate the output voltage to a desired value, the voltage divider for feedback should be designed to result in 3V to the feedback (FB) pin, expressed as:

$$\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot V_{OUT} = 3V \quad (21)$$

(Design Example) Selecting R_{FB1} as 1MΩ, R_{FB2} is obtained as:

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{3} - 1} = \frac{1 \times 10^6}{\frac{400}{3} - 1} = 7.56k\Omega$$

[STEP-6] Design OVP Circuit

FAN9611/12 has two levels of over-voltage protection (OVP) for the output. Non-latching OVP is combined with the feedback (FB) pin and trips when the output voltage exceeds 108% of its nominal value. The latching OVP uses dedicated pin and trips when the OVP pin voltage exceeds an independent threshold of 3.5V, expressed as:

$$\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot V_{OUT,LATCH} = 3.5V \quad (22)$$

When the latching OVP is combined with FB pin, it trips at 115% of the nominal output voltage.

(Design Example) Selecting OVP level as 472V and R_{OV1} as 2MΩ, R_{OV2} is obtained as:

$$R_{OV2} = \frac{R_{OV1}}{\frac{V_{OUT,LATCH}}{3.5} - 1} = \frac{2 \times 10^6}{\frac{472}{3.5} - 1} = 14.9k\Omega$$

[STEP-7] Determine current sensing resistor

It is typical to set the pulse-by-current limit level a little higher than the maximum inductor current at maximum power limit condition as:

$$I_{CS,LIM} \geq 2\sqrt{2} \cdot \frac{P_{MAX,CH}}{V_{LINE,MIN} \cdot \eta} \quad (23)$$

Then, the sensing resistor is selected as:

$$R_{CS} = \frac{0.2}{I_{CS.LIM}} \quad (24)$$

(Design Example)

$$I_{CS,LIM} \geq 2\sqrt{2} \cdot \frac{P_{MAX,CH}}{V_{LINE,MIN} \cdot \eta} = 2\sqrt{2} \cdot \frac{200 \cdot 1.2}{85 \cdot 0.95} = 8.4A$$

Choosing $I_{CS.LIM}$ as 9.1A (10% margin on 8.4A), the sensing resistor is selected as:

$$R_{CS} = \frac{0.2}{I_{CS.LIM}} = \frac{0.2}{9.1} = 0.022\Omega$$

[STEP-8] Output Capacitor Selection

The output voltage ripple should be considered when selecting the output capacitor. Figure 16 shows the twice line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

$$C_{OUT} > \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot V_{OUT,RIPPLE}} \quad (25)$$

where I_{OUT} is total nominal output current of two boost PFC stage and $V_{OUT,RIPPLE}$ is the peak-to-peak output voltage ripple specification.

Since too large ripple on the output voltage may cause premature OVP during normal operation, the peak-to-peak ripple specification should be smaller than 15% of the nominal output voltage.

The holdup time also should be considered when determining the output capacitor as:

$$C_{OUT} > \frac{2P_{OUT} \cdot t_{HOLD}}{V_{OUT}{}^2 - V_{OUT,MIN}{}^2} \quad (26)$$

where:
P_{OUT} is total nominal output power of two boost PFC stage ($2P_{OUT,CH}$);

t_{HOLD} is the required holdup time; and

$V_{OUT,MIN}$ is the allowable minimum output voltage during the holdup time.

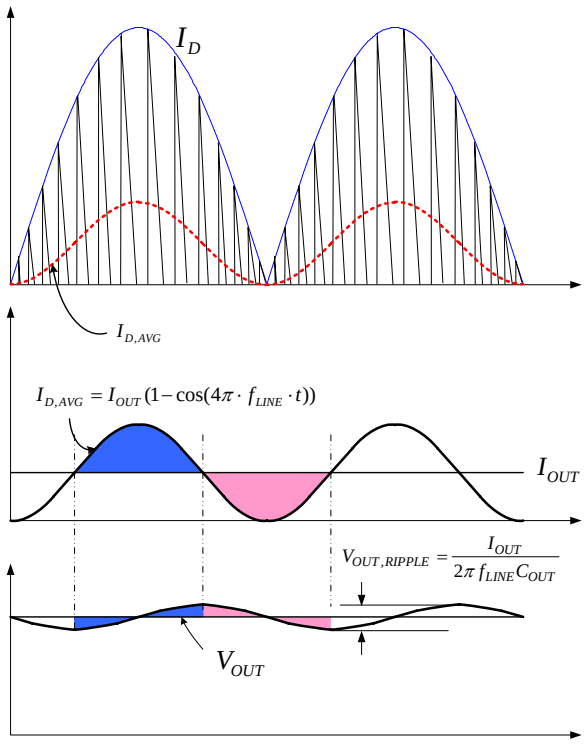


Figure 16. Output Voltage Ripple

(Design Example) With the ripple specification of $8V_{p-p}$, the capacitor should be:

$$C_{OUT} > \frac{I_{OUT}}{2\pi \cdot f_{LINE} \cdot V_{OUT,RIPPLE}} = \frac{1}{2\pi \cdot 50 \cdot 8} = 398\mu F$$

Since minimum allowable output voltage during one cycle line (20ms) drop-outs is 330V, the capacitor should be:

$$C_{OUT} > \frac{2P_{OUT} \cdot t_{HOLD}}{V_{OUT}^2 - V_{OUT,MIN}^2} = \frac{2 \cdot 400 \cdot 20 \times 10^{-3}}{400^2 - 330^2} = 313\mu F$$

Thus, two 220µF capacitors in parallel are selected for the output capacitor.

[STEP-9] Design Compensation Network

The boost PFC power stage can be modeled as shown in Figure 17. Since FAN9611/12 employs line feed-forward, the power stage transfer function becomes independent of the line voltage. Then, the power stage can be modeled as a voltage-controlled current source supplying RC network.

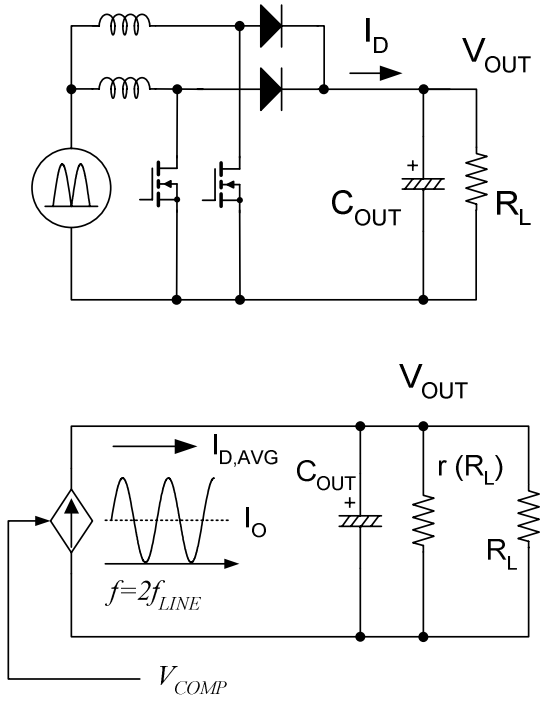


Figure 17. Small Signal Modeling of the Power Stage

By averaging the diode current during the half line cycle, the low frequency behavior of the voltage controlled current source of Figure 17 is obtained as:

$$I_{D,LF} = I_{OUT} \cdot K_{MAX} \cdot \frac{(V_{COMP} - 0.2)}{4.1} \quad (27)$$

where I_{OUT} is total nominal output current corresponding to P_{OUT}, V_{COMP} is compensation pin voltage, 0.2V is PWM offset voltage and 4.1 is error amplifier control range (refer to Figure 13).

Then, the low-frequency, small-signal, control-to-output transfer function is obtained as:

$$\frac{\hat{v}_{OUT}}{\hat{v}_{COMP}} = \frac{I_{OUT} \cdot K_{MAX}}{4.1} \cdot \frac{R_L}{2} \cdot \frac{1}{1 + \frac{s}{2\pi f_P}} \quad (28)$$

where $f_P = \frac{2}{2\pi \cdot R_L C_{OUT}}$ and

R_L is the output load resistance in a given load condition.

Figure 18 shows the variation of the control-to-output transfer function for different loads. As can be seen, the characteristics at frequencies above the pole are unchanged while the pole moves as load changes. Since the low frequency gain increases as load decreases, the light load condition is the worst condition for feedback loop compensation. Assuming the load resistance is infinite, the control-to-output transfer function at light load condition is obtained from Equation 28 as:

$$\frac{\hat{v}_{OUT}}{\hat{v}_{COMP}}\Big|_{@LIGHT,LOAD} \cong \frac{I_{OUT} \cdot K_{MAX}}{4.1} \cdot \frac{1}{sC_{OUT}} \quad (29)$$

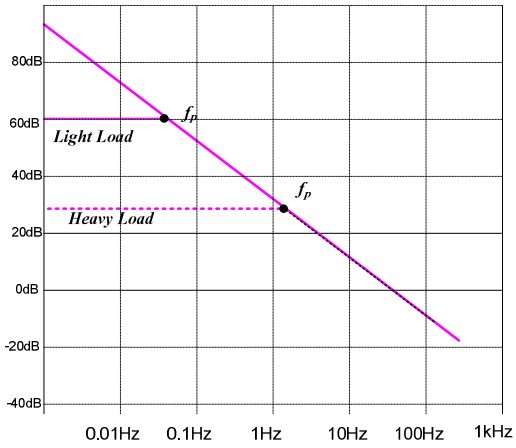


Figure 18. Control-to-Output Transfer Function

Proportional and integration (PI) control with high frequency pole is typically used for compensation, as shown in Figure 19. The compensation zero (f_{CZ}) introduces phase boost, while the high frequency compensation pole (f_{CP}) attenuates the switching ripple.

The transfer function of the compensation network is obtained as:

$$\frac{\hat{v}_{COMP}}{\hat{v}_{OUT}} = \frac{2\pi f_I}{s} \cdot \frac{1+\frac{s}{2\pi f_{CZ}}}{1+\frac{s}{2\pi f_{CP}}} \tag{30}$$

$$f_I = \frac{3}{V_{OUT}} \cdot \frac{80\mu A/V}{2\pi \cdot C_{COMP,LF}},$$

where $f_{CZ} = \frac{1}{2\pi \cdot R_{COMP} \cdot C_{COMP,LF}}$,

$$f_{CP} = \frac{1}{2\pi \cdot R_{COMP} \cdot C_{COMP,HF}}$$

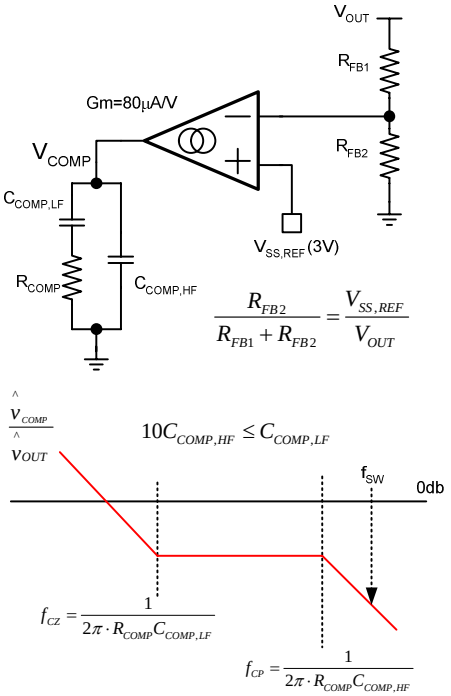


Figure 19. Compensation Network

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_C) around 1/10~1/5 of line frequency. Since the control-to-output transfer function of power stage has -20dB/dec slope and -90° phase at the crossover frequency, as shown in Figure 20; it is required to place the zero of the compensation network (f_{CZ}) around the crossover frequency so that 45° phase margin is obtained. Then, the capacitor $C_{COMP,LF}$ is determined as:

$$C_{COMP,LF} = \frac{80\mu A/V \cdot I_{OUT} \cdot K_{MAX}}{4.1 \cdot C_{OUT} \cdot (2\pi f_C)^2} \cdot \frac{3}{V_{OUT}} \tag{31}$$

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

$$R_{COMP} = \frac{1}{2\pi \cdot f_C \cdot C_{COMP,LF}} \tag{32}$$

(b) Place compensator high-frequency pole (f_{CP}) at least a decade higher than f_C to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter so noise can be effectively attenuated. Then, the capacitor $C_{COMP,HF}$ is determined as:

$$C_{COMP,HF} = \frac{1}{2\pi \cdot f_{CP} \cdot R_{COMP}} \tag{33}$$

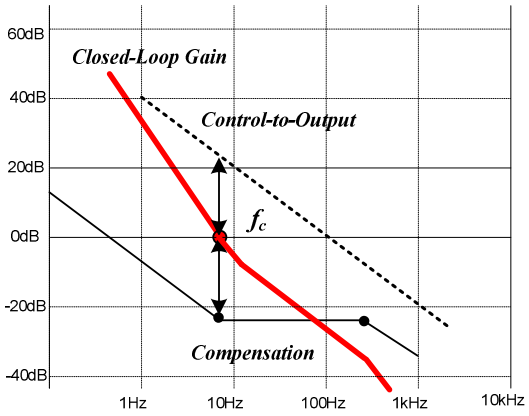


Figure 20. Compensation Network Design

(Design Example) Choosing the crossover frequency (control bandwidth) at 5Hz, $C_{COMP,LF}$ is obtained as:

$$C_{COMP,LF} = \frac{80\mu A/V \cdot I_{OUT} \cdot K_{MAX}}{4.1 \cdot C_{OUT} \cdot (2\pi f_C)^2} \cdot \frac{3}{V_{OUT}} = \frac{10^{-4} \cdot 1 \cdot 1.2}{4.1 \cdot 440 \times 10^{-6} \cdot (2\pi \cdot 5)^2} \cdot \frac{3}{400} = 405nF$$

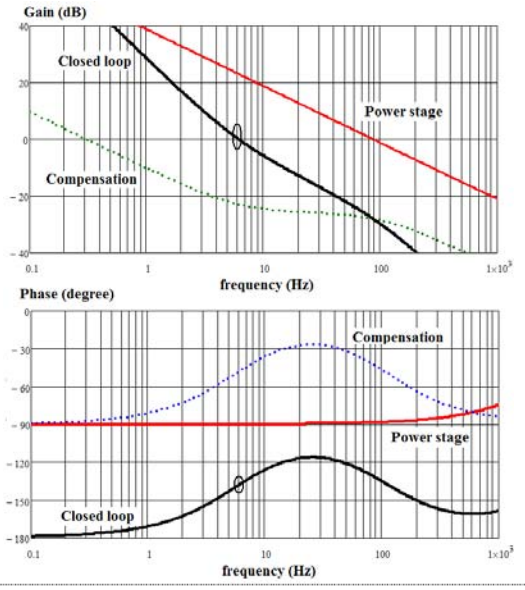
Actual $C_{COMP,LF}$ is determined as 390nF since it is the closest value among the off-the-shelf capacitors. Then, R_{COMP} is obtained as:

$$R_{COMP} = \frac{1}{2\pi \cdot f_C \cdot C_{COMP,LF}} = \frac{1}{2\pi \cdot 5 \cdot 390 \times 10^{-9}} = 82k\Omega$$

Selecting the high-frequency pole as 120Hz, $C_{COMP,HF}$ is obtained as:

$$C_{COMP,HF} = \frac{1}{2\pi f_{CP} \cdot R_{COMP}} = \frac{1}{2\pi \cdot 120 \cdot 82 \times 10^3} = 16.3nF$$

Actual $C_{OMP,HF}$ is determined as 15nF since it is the closest value among the off-the-shelf capacitors. These components result in a control loop with a bandwidth of 6Hz and phase margin of 45° as below. The actual bandwidth is a little larger than the asymptotic design



[STEP-10] Soft-Start Capacitor Selection

FAN9611/12 employs closed-loop soft-start, where the reference of the error amplifier is gradually increased to the final value corresponding to the nominal output voltage. The reference is also actively managed during the soft-start period to prevent the reference running away from the feedback voltage. The slope of the voltage reference is made a function of the error amplifier output voltage (V_{COMP}), i.e. the output power of the converter. The soft-start time is then adjusted according to load condition.

It is typical to set he maximum rising speed of the soft-start capacitor such that it is 30%~60% of that of the output voltage, defined by the maximum power limit as:

$$0.3 \cdot \frac{I_{OUT} \cdot K_{MAX}}{C_{OUT} \cdot V_{OUT}} < \frac{5\mu A}{C_{SS} \cdot V_{SS,REF}} < 0.6 \cdot \frac{I_{OUT} \cdot K_{MAX}}{C_{OUT} \cdot V_{OUT}} \quad (34)$$

where $V_{SS,REF}$ is the final value of soft-start capacitor voltage. Then, the condition for the soft-start capacitor is given as:

$$\frac{5\mu A \cdot C_{OUT} \cdot V_{OUT}}{0.6 \cdot I_{OUT} \cdot K_{MAX} \cdot V_{SS,REF}} < C_{SS} < \frac{5\mu A \cdot C_{OUT} \cdot V_{OUT}}{0.3 \cdot I_{OUT} \cdot K_{MAX} \cdot V_{SS,REF}} \quad (35)$$

(Design Example) Since two 220µF capacitors in parallel are selected for the output capacitor:

$$\frac{5\mu A \cdot C_{OUT} \cdot V_{OUT}}{0.6 \cdot I_{OUT} \cdot K_{MAX} \cdot V_{SS,REF}} < C_{SS} < \frac{5\mu A \cdot C_{OUT} \cdot V_{OUT}}{0.3 \cdot I_{OUT} \cdot K_{MAX} \cdot V_{SS,REF}}$$

$$406nF < C_{SS} < 813nF$$

Thus, a 470nF capacitor is selected for the soft-start capacitor.

[STEP-11] Line Filter Capacitor Selection

It is typical to use small bypass capacitors across bridge rectifier output stage to filter the switching current ripple, as shown in Figure 21. Since the impedance of the line filter inductor at line frequency is negligible compared to the impedance of the capacitors, the line frequency behavior of the line filter stage can be simply modeled, as shown in Figure 21. Even though the bypass capacitors absorb switching ripple current, it also generates circulating capacitor current, which leads the line voltage by 90°, as shown in Figure 22. As observed, the circulating current through the capacitor is added to the load current and generates displacement between line voltage and line current.

The displacement angle is given by:

$$\theta = \tan^{-1}\left(\frac{\eta \cdot V_{LINE,MAX}^{\ 2} \cdot 2\pi f_{LINE} \cdot C_{EQ}}{P_{OUT}}\right) \quad (36)$$

where C_{EQ} is the equivalent capacitance that appears across the AC line ($C_{EQ}=C_{F1}+C_{F2}+C_{HF}$).

The resultant displacement factor is:

$$DF = \cos(\theta) \quad (37)$$

Since the displacement factor is related to power factor, the capacitors in the line filter stage should be selected carefully. With a given minimum displacement factor (DF_{MIN}) at full load condition, the allowable effective input capacitance is obtained as:

$$C_{EQ} < \frac{P_{OUT}}{\eta \cdot V_{LINE,MAX}^{\ 2} \cdot 2\pi f_{LINE}} \cdot \tan(\cos^{-1}(DF_{MIN})) \quad (38)$$

(Design Example) Assuming the minimum displacement factor at full load is 0.99, the equivalent input capacitance is obtained as:

$$C_{EQ} < \frac{P_{OUT}}{\eta \cdot V_{LINE,MAX}{}^2 \cdot 2\pi f_{LINE}} \cdot \tan(\cos^{-1}(DF_{MIN}))$$
$$< \frac{400}{0.95 \cdot 265^2 \cdot 2\pi \cdot 50} \cdot \tan(\cos^{-1}(0.99)) = 2.7\mu F$$

Thus, the sum of the capacitors in the input side should be smaller than 2.7μF.

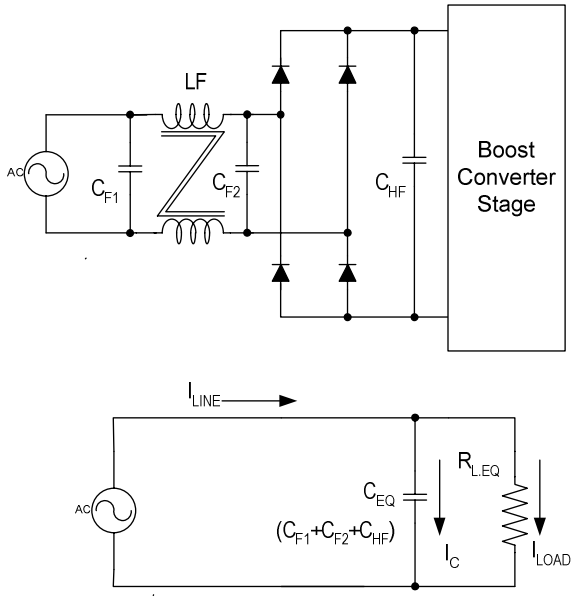


Figure 21. Equivalent Circuit of Line Filter Stage

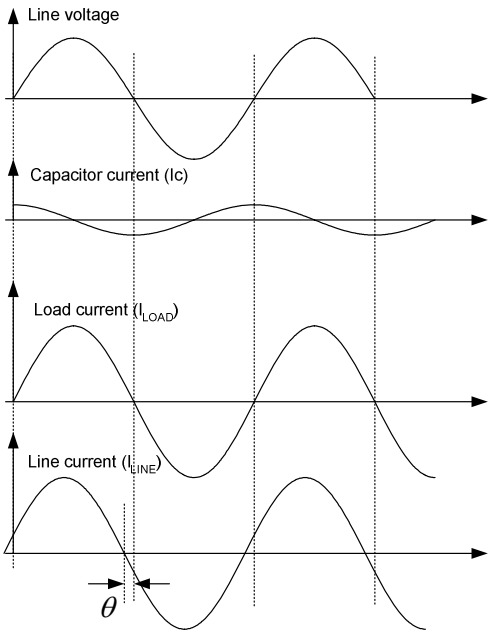


Figure 22. Line Current Displacement

PCB Layout Guidelines

For high-power applications, two or more PCB layers are recommended to effectively use the ground pattern to minimize the switching noise interference from the two high-frequency outputs. The following guidelines are recommended for all layout designs, but especially strongly for the single-layer PCB designs.

Power Ground and Analog Ground

- Power ground (PGND) and analog ground (AGND) should meet at one point only.
- All the control components should be connected to AGND without sharing the trace with PGND.
- The return path for the gate drive current and V_{DD} capacitor should be connected to the PGND pin.
- The ground loops between the driver outputs (DRV1/2), MOSFETs, and PGND should be minimized.
- Adding the by-pass capacitor for noise on the V_{DD} pin is recommended. It should be connected as close to the pin as possible.

Gate Drive Pattern

- The gate drive pattern should be wide enough to handle 1A peak current.
- The gate drive pattern should be as short as possible to minimize interference.

Current Sensing

- Current Sensing should be as short as possible.
- To minimize switching noise, current sensing should not make a loop.

Input Voltage Sensing (V_{IN})

- Since the impedance of voltage divider is large and FAN9611/12 detects the peak of the line voltage, the VIN pin can be sensitive to the switching noise. Therefore, the trace connected to this pin should not cross traces with high di/dt to minimize the interference.
- The noise bypass capacitor for V_{IN} should be connected as close to the pin as possible.

Figure 23 shows the single-layer PCB example, where the FAN9611/12 is on the bottom of PCB (SOIC package).

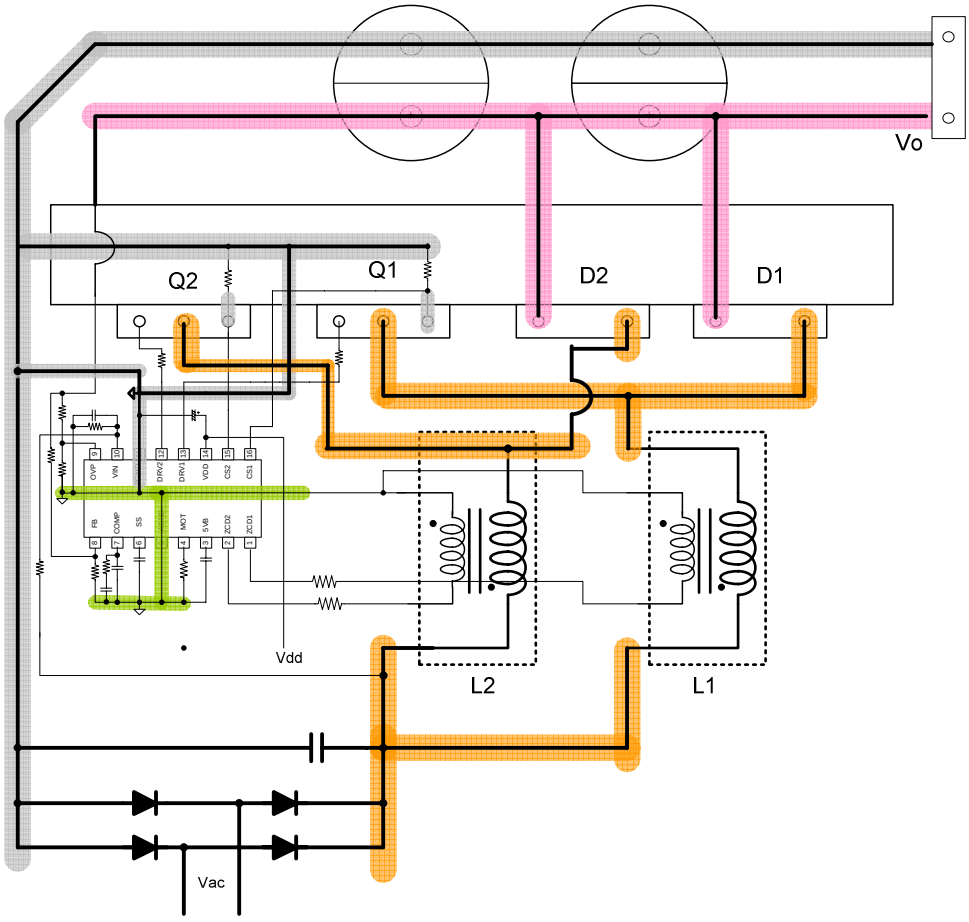


Figure 23. Single-Layer PCB Layout Example

Design Summary

Figure 24 shows the final schematic of the 400W interleaved BCM Boost PFC design example. PQ3230 cores are used for the boost inductors.

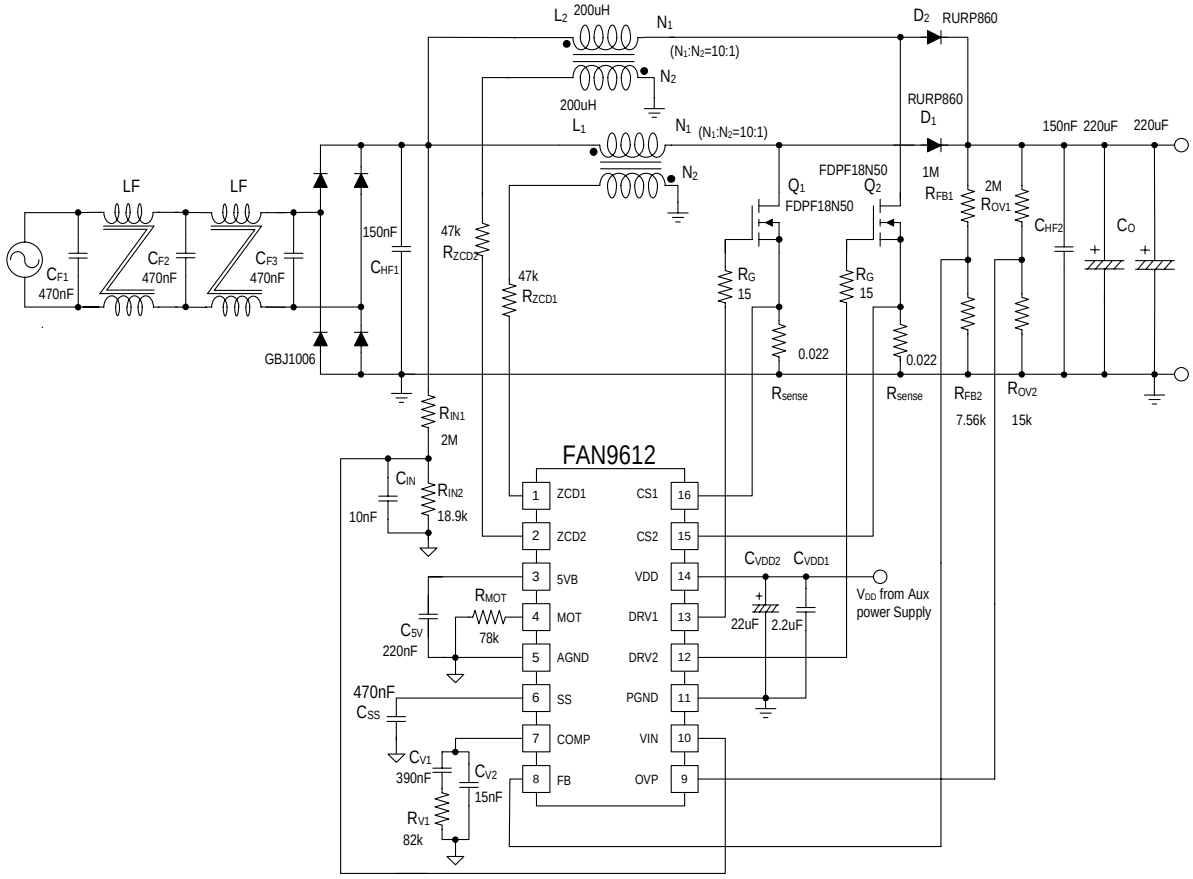


Figure 24. Final Schematic of Design Example

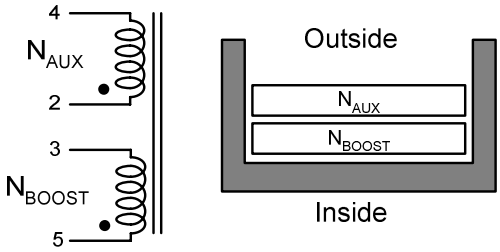


Figure 25. Boost Inductor Specification

Table 1. Winding Specification

	Pin	Diameter / Thickness	Turns
N1	5 → 3	0.1mm × 100 (Litz wire)	30
Insulation Tape		0.05mm	3
N2	2 → 4	0.2mm	3
Insulation Tape		0.05mm	3

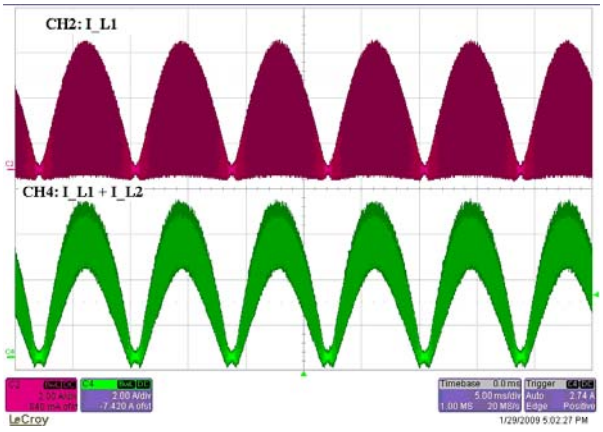
Core: PQ3230 (Ae=161 mm^2)
Bobbin: PQ3230
Inductance: 200μH

6. Experimental Verification

To show the validity of the design procedure presented in this application note, the converter of the design example was built and tested. All the circuit components are used as designed in the design example.

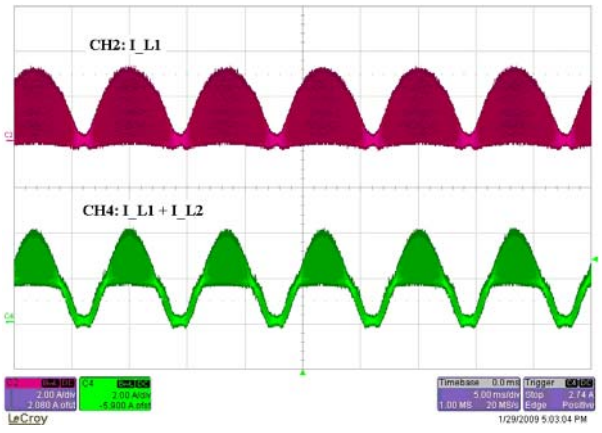
Figure 26 and Figure 27 show the inductor current ripple cancellation for $115V_{AC}$ and $230V_{AC}$ condition, respectively. As can be observed, the sum of two inductor currents has very small ripple due to the interleaving operation.

Figure 28 shows the brown-out protection. As designed, the protection trips when the line voltage drops below $70V_{AC}$. Figure 29 and Figure 30 show the soft-start waveforms at full load for $115V_{AC}$ and $230V_{AC}$ line voltage, respectively. As observed, there is no overshoot on the output voltage during startup. Figure 31 shows the measured efficiency for $115V_{AC}$ and $230V_{AC}$ line voltage. The full-load efficiency is 96.4% and 98.2% for $115V_{AC}$ and $230V_{AC}$, respectively. The power factor is shown in Table 2. The power factor at full load is 0.993 and 0.988 for $115V_{AC}$ and $230V_{AC}$, respectively.



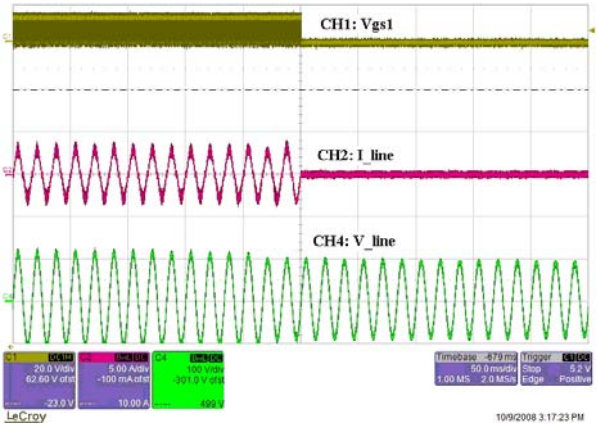
CH2: Inductor current I_{L1} (5A/div)
CH4: Sum of two inductor current $I_{L1}+I_{L2}$ (5A/div)

Figure 26. Inductor Current Waveforms at $115V_{AC}$



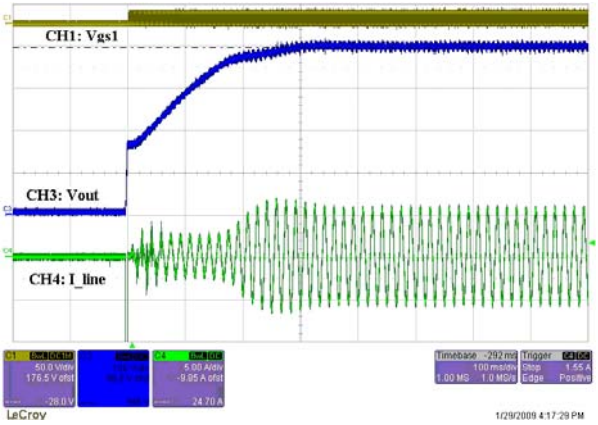
CH2: Inductor current I_{L1} (5A/div)
CH4: Sum of two inductor current $I_{L1}+I_{L2}$ (5A/div)

Figure 27. Inductor Current Waveforms at $230V_{AC}$



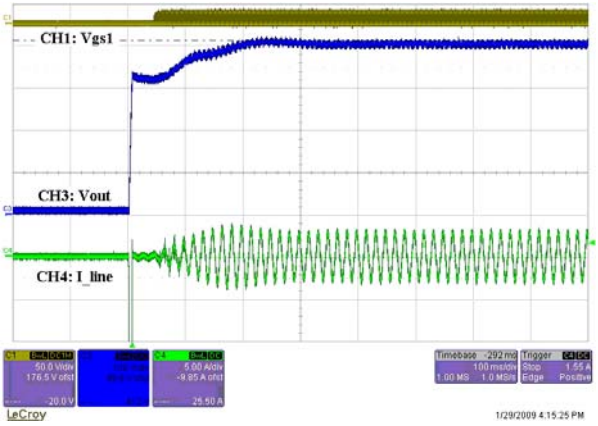
CH1: Gate drive signal V_{GS1} (20V/div)
CH2: Line current (5A/div), CH4: Line voltage (100VA/div)

Figure 28. Brownout Protection



CH1: Gate drive signal V_{GS1} (20V/div)
CH3: Output voltage (100V/div)
CH4: Line current (5A/div)

Figure 29. Soft-Start Waveforms at Full-Load and $115V_{AC}$ Line Condition



CH1: Gate drive signal V_{GS1} (20V/div)
CH3: Output voltage (100V/div)
CH4: Line current (5A/div)

Figure 30. Soft-Start Waveforms at Full-Load and $230V_{AC}$ Line Condition

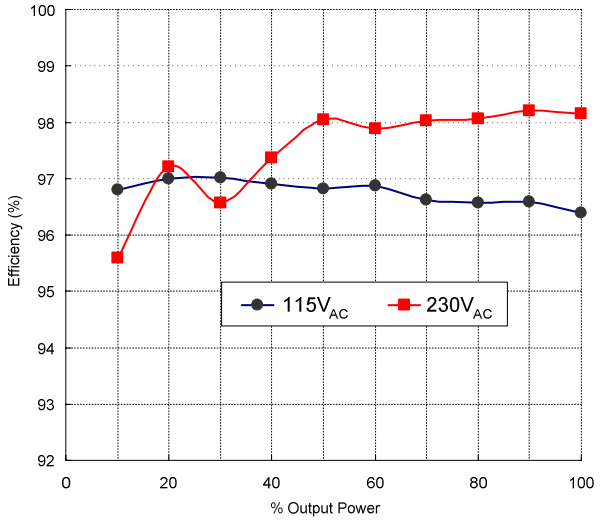


Figure 31. Measured Efficiency

Table 2. Measured Power Factor

Line Voltage	100% Load	75% Load	50% Load
$115V_{AC}$	0.993	0.990	0.984
$230V_{AC}$	0.988	0.983	0.974

Definition of Terms

η is the efficiency.
ΔB is the maximum flux swing of the core at nominal output power in Tesla.
A_e is the cross-sectional area of core.
B_{MAX} is the maximum flux density of boost inductor at maximum output power in Tesla.
C_{DD} is the total capacitance of capacitors connected to the V_{DD} pin.
f_C is the crossover frequency.
f_{CP} is the high frequency compensation pole to attenuate the switching ripple.
f_{CZ} is the compensation zero.
f_{LINE} is the line frequency.
$f_{SW,MIN}$ is the minimum switching frequency.
$I_{CS,LIM}$ is the pulse-by-pulse current limit level determined by sensing resistor.
$I_{L,PK}$ is the maximum peak inductor current at the nominal output power.
I_{OUT} is total nominal output current of two boost PFC stages.
$I_{OUT,MAX}$ is the maximum output current, which corresponds to P_{MAX}.
K_{MAX} is maximum power limiting factor (a ratio between the limited maximum output power and nominal output power).
L is the boost inductance.
N_{AUX} is the number of turns of auxiliary winding in boost inductor.
N_{BOOST} is the number of turns of primary winding in boost inductor.
P_{MAX} is the limited maximum output power of two boost PFC stages ($2P_{MAX,CH}$).
$P_{MAX,CH}$ is the limited maximum output power per channel.
P_{OUT} is total nominal output power of two boost PFC stages ($2P_{OUT,CH}$).
$P_{OUT,CH}$ is the nominal output power per channel.
t_{HOLD} is the required hold-up time.
$t_{ON,MAX}$ is the maximum on time determined by the MOT resistor.
V_{COMP} is compensation pin voltage.
$V_{IN}(t)$ is the rectified line voltage.
$V_{IN,PK}$ is the amplitude of line voltage.
V_{LINE} is RMS line voltage.
$V_{LINE,HYS}$ is the hysteresis RMS line voltage of brownout protection.
$V_{LINE,MAX}$ is the maximum RMS line voltage.
$V_{LINE,MIN}$ is the minimum RMS line voltage.
$V_{LINE,MINF}$ is the RMS line voltage that results in minimum switching frequency.
$V_{LINE,OVP}$ is the line OVP trip point in RMS.
V_{ON} is UVLO start voltage for V_{DD}.
V_{OUT} is the PFC output voltage.
$V_{OUT,LATCH}$ is the output OVP trip point.
$V_{OUT,MIN}$ is the allowable minimum output voltage during the hold-up time.
$V_{OUT,RIPPLE}$ is the peak-to-peak output voltage ripple.
$V_{REF,SS}$ is the reference voltage for soft-start and feedback compensation.

References

[1] Fairchild Datasheet FAN9611 / FAN9612 *Interleaved Dual BCM, PFC Controller*

[2] Fairchild Application Note AN-6027, *Design of Power Factor Correction Circuit Using FAN7530*

[3] Fairchild Power Seminar 2008-2009 Paper, *Understanding Interleaved Boundary Conduction Mode PFC Converters*

[4] Fairchild Evaluation Board User Guide FEB279, *400W Evaluation Board using FAN9612 ((AN-8018)*

[5] Fairchild Application Note AN-8021, *Building Variable Output Voltage Boost PFC Converters Using FAN9611/12*

[6] Fairchild Evaluation Board User Guide FEB301, *400W Single-Layer Evaluation Board using FAN9612 (AN-8026)*

Related Datasheets

FAN9611 / FAN9612 — Interleaved Dual BCM PFC Controllers

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