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Application Note AN-6014

Green Current Mode PWM Controller FAN7602

1. Introduction

The FAN7602 is a BCDMOS fixed-frequency current-mode PWM controller designed for off-line power supplies. To reduce the power loss at a light load and no load, the FAN7602 operates in the burst mode and it includes a start-up switch to reduce the loss of the IC start-up circuit. Because of the internal start-up switch and the burst mode operation, it is possible to supply 0.5W output load with under 1W input power when the input line voltage is 265V. On no load condition, the input power is under 0.3W.

The FAN7602 offers a latch protection pin for the system protection, like over-voltage protection or/and thermal shut-down. The internal V_{CC} over-voltage protection function shuts down the IC when the supply voltage reaches 19V. Furthermore, the internal soft-start function is provided and the soft-start time is 10ms. It provides LUVP (Line Under-Voltage Protection) function for AC brown-in and brown-out protection. OLP (Over Load Protection) protects the power supply system against excessive load if the OLP condition continues over 22ms. The switching frequency is internally fixed a 65kHz and ±2kHz frequency modulation (FM) is implemented for lower EMI. The frequency of FM is 125Hz. And the Latch/Plimit pin can be used to limit the output power over the entire input voltage range constantly.

Figure 1 shows the block diagram of the FAN7602.

The FAN7602 contains the following blocks:

- Start-up circuit and soft-start
- Clock with frequency modulation
- Current sense and feedback with power limit
- Overload protection
- Burst mode
- Line under-voltage protection
- Latch protection
- Output drive

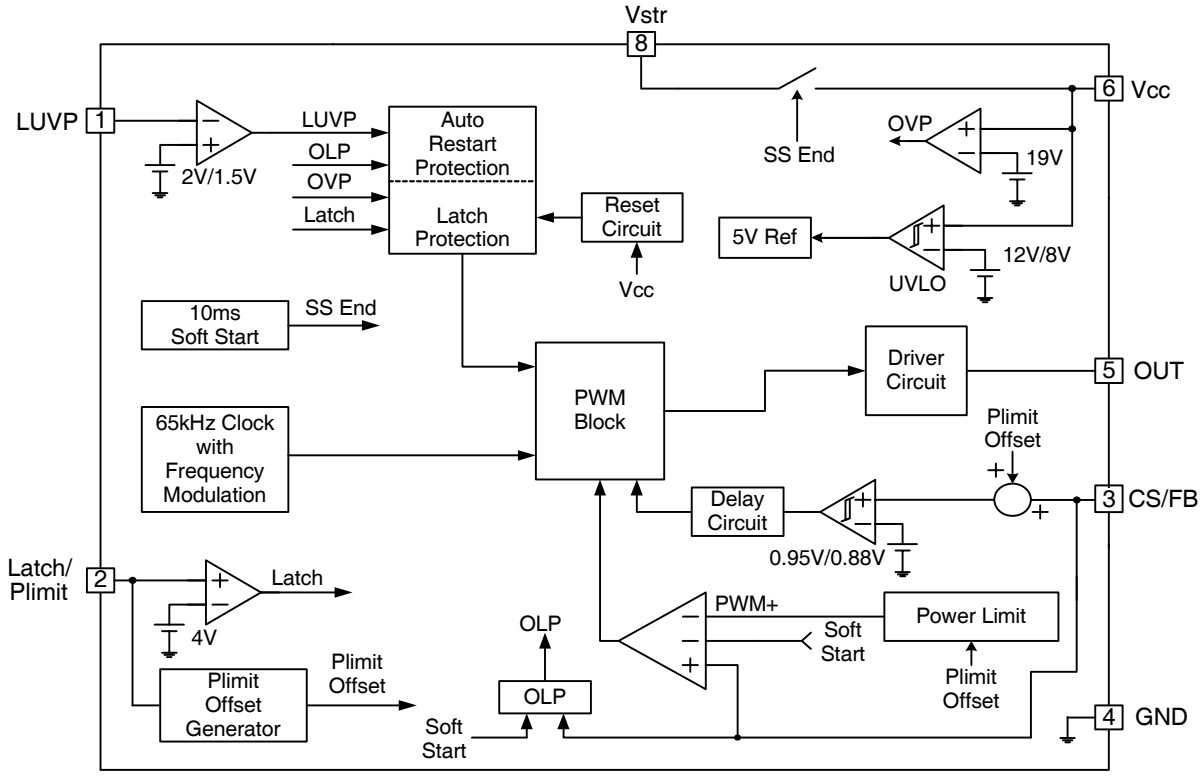


Figure 1. Internal Block Diagram of the FAN7602

2. Device Block Description

2.1 Start-up Circuit and Soft-start

The FAN7602 contains a start-up switch to reduce the power loss of the external start-up circuit in conventional PWM converters. The internal start-up circuit charges the V_{CC} capacitor with 1mA current source if the AC line is connected and the start-up switch is turned off 5ms after the soft-start ends, as shown in Fig. 2. The soft-start function starts when the V_{CC} voltage reaches the start-threshold voltage of 12V and ends when the internal soft-start voltage reaches 1V. The internal start-up circuit starts charging the V_{CC} capacitor again if the V_{CC} voltage is lowered to the minimum operating voltage of 8V. Then the UVLO block shuts down the output drive circuit and some blocks to reduce the IC operating current and the internal soft-start voltage drops to zero. If the V_{CC} voltage reaches the start-threshold voltage, the IC starts switching again and the soft-start block works.

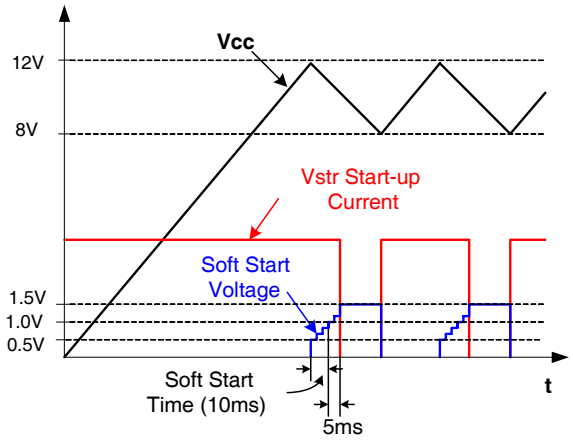


Figure 2. Start-up Current and V_{CC} Voltage

Figure 3 shows a typical start-up sequence for the FAN7602. The V_{CC} voltage should be higher than the minimum operating voltage during the start-up to enter the steady state. If the V_{CC} voltage is higher than 19V, the over-voltage protection function works and this is a latch protection. There is 5.5µs delay in the over-voltage protection circuit and it is reset when the V_{CC} voltage goes below 5V.

The V_{CC} capacitor can be selected according to the soft-start time and the total gate charge (Qg) of the MOSFET. During the soft-start time (Tss), the V_{CC} capacitor is charged by 1mA Vstr start-up current from the Vstr pin and the V_{CC} capacitor is discharged by 1mA (typ.) IC operating current and the MOSFET gate drive current. The MOSFET gate drive current is Qg•fsw. Qg increases according to the MOSFET drain source voltage, therefore the drive current is maximum when the input line voltage is highest. During the soft-start time, the converter output voltage is very low, so little current is supplied to the V_{CC} capacitor from the V_{CC} winding. The V_{CC} capacitor must be large enough to supply enough current during the soft-start time at start-up. The value of the V_{CC} capacitor is determined by (1) considering the worst case. 3.6V is the minimum UVLO hysteresis voltage, 1.5mA is the maximum IC operating current, 15ms is the maximum soft-start time and 0.7mA is the minimum Vstr start-up current.

$$C_{Vcc} > \frac{Tss \cdot (I_{OP} - I_{str} + Q_g \cdot f_{sw})}{3.6V} > \frac{15ms \cdot (1.5mA - 0.7mA + Q_g \cdot 65kHz)}{3.6V} \quad (1)$$

Figure 4 shows the V_{CC} voltage at start-up with a 10µF capacitor and a FQPF8N60C MOSFET when the input line voltage is 265V. As shown in the figure, 10µF is enough for start-up but 22µF is used in the demo board because the UVLO works in the burst mode at no load condition. The V_{CC} capacitor value should be increased if the UVLO works in the burst mode to prevent input power increase.

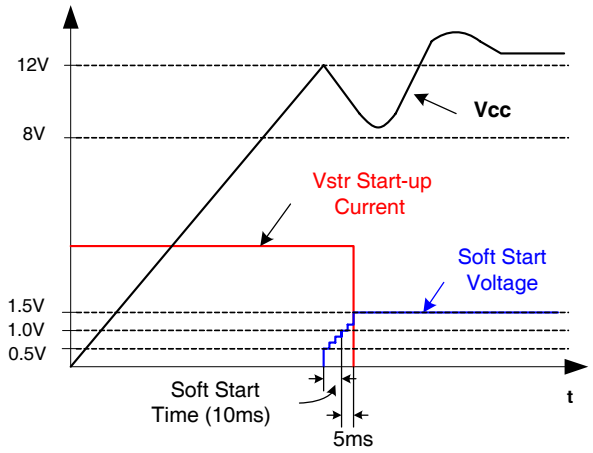


Figure 3. Typical Start-up Sequence for FAN7602

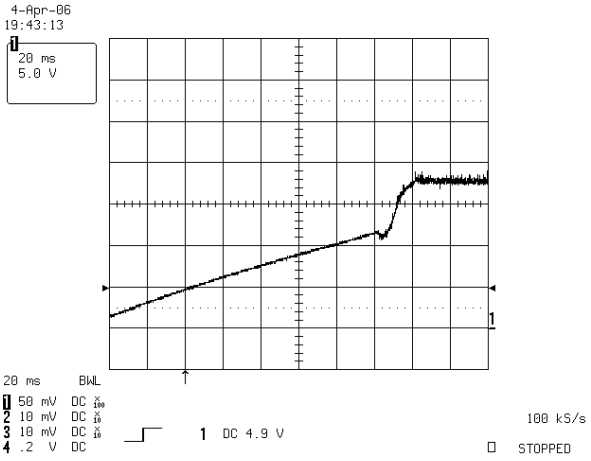


Figure 4. V_{CC} Voltage Waveform at Start-up

Figure 5 shows the internal soft-start voltage during start-up. It starts from 0.5V and becomes 1V after 10ms and is clamped to 1.5V after 15ms.

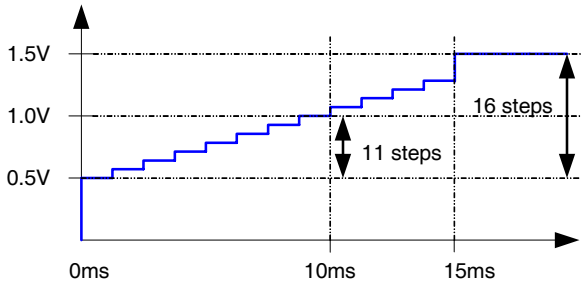


Figure 5. Internal Soft-start Voltage

2.2 Clock with Frequency Modulation

The oscillator frequency is set internally and there is frequency modulation (FM) function to reduce EMI. The average frequency is 65kHz and the modulation frequency is ±2kHz. The frequency varies from 63kHz to 67kHz with 16 steps. A frequency step is 250Hz and FM frequency is 125Hz, as shown in Fig. 6.

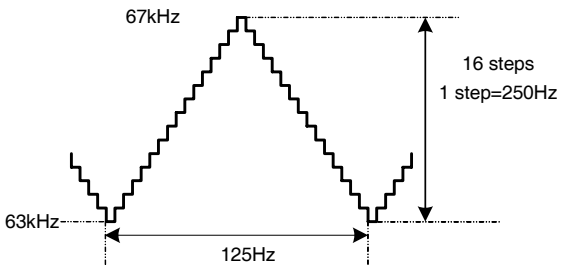


Figure 6. Frequency Modulation

2.3 Current Sense and Feedback with Power Limit

The FAN7602 performs the current sensing for the current mode PWM and the output voltage feedback with only one pin, pin 3. To achieve the two functions with one pin, an internal LEB (Leading Edge Blanking) circuit to filter the current sense noise is excluded because the external RC filter is necessary to add the output voltage feedback information and the current sense information.

Figure 7 shows the current sense and feedback circuits. R_S is the current sense resistor to sense the switch current. The current sense information is filtered by an RC filter composed of R_F and C_F. According to the output voltage feedback information, I_{FB} charges or stops charging C_F to adjust the offset voltage. If I_{FB} is zero, C_F is discharged through R_F and R_S, lowering the offset voltage. Figure 8 shows typical voltage waveforms of the CS/FB pin. The current sense waveform is added to the offset voltage as shown in the figure. The CS/FB pin voltage is compared with PWM+ that is 1V-Plimit offset, as shown in Fig. 8. If the CS/FB voltage meets PWM+, the output driver is shut off. As shown in Fig. 8, if the feedback offset voltage is low, the switch on-time is increased. On the contrary, if the feedback offset voltage is high, the switch on-time is decreased. In this way, the duty cycle is controlled according to the load condition.

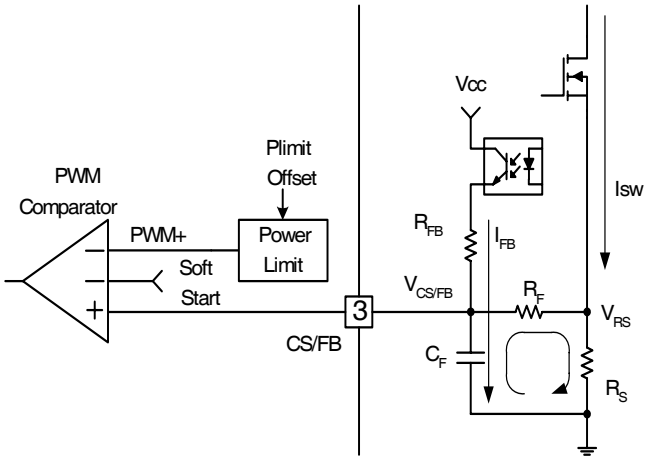


Figure 7. Current sense and Feedback Circuits

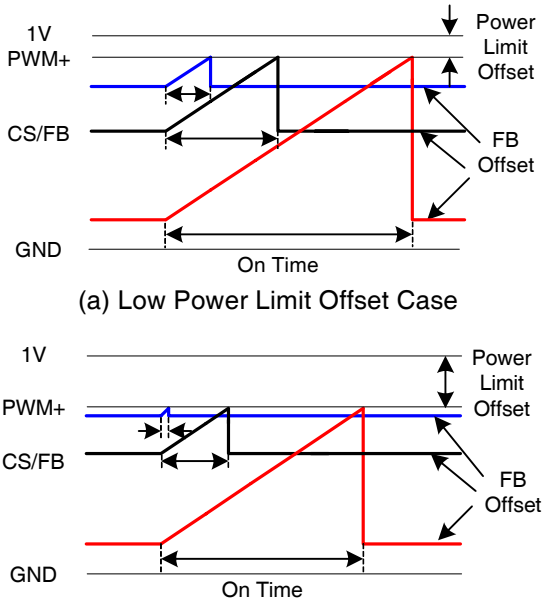


Figure 8. CS/FB Voltage Waveforms

In general, the maximum output power increases as the input voltage increases because the current slope during switch on-time increases. To limit the converter output power constantly, the power-limit function is included in the FAN7602. Sensing the converter input voltage through the Latch/Plimit pin, the Plimit offset voltage is subtracted from 1V, as shown in Fig. 8. Because the Plimit offset voltage is subtracted from 1V, the switch on-time decreases as the Plimit offset voltage increases. If the converter input voltage increases, the switch on-time decreases, controlling the output power constant. The offset voltage is proportional to the Latch/Plimit pin voltage and the gain is 0.16. If the Latch/Plimit voltage is 1V, the offset voltage is 0.16V. The input voltage can be sensed by a resistive voltage divider.

Because R_{FB} and R_F work as a voltage divider for the current sense voltage V_{Rs}, the current sense information is decreased by (2). Selecting the current-sense resistor, this reduction should be considered.

$$V_{CS/FB} = \frac{R_{FB}}{R_{FB}+R_F} \cdot V_{R_S} \quad (2)$$

Figure 9 shows the reduction of the current sense information when R_{FB} is 6kΩ and R_F is 1kΩ.

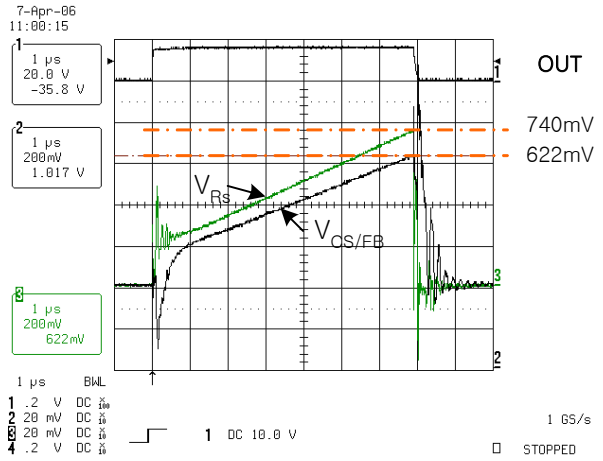


Figure 9. CS/FB Waveform Reduction

2.4 Overload Protection

The FAN7602 contains the overload protection function. If the output load is higher than the rated output current, the output voltage drops and the feedback error amplifier is saturated. Then the offset of the CS/FB voltage representing the feedback information is almost zero. That means that the offset voltage can be used to detect the OLP condition. As shown in Fig. 10, the CS/FB voltage is compared with 50mV reference during the internal clock signal is high and if the voltage is lower than 50mV, the OLP timer starts counting. If this condition persists for 22ms, the timer generates an OLP signal and this protection is reset by the UVLO.

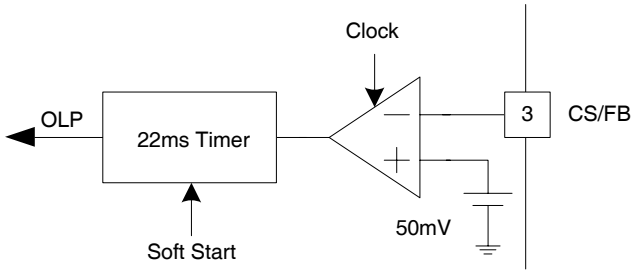


Figure 10. Overload Protection Circuit

For the flyback converter, if the converter operates in continuous current mode, the offset voltage represents the feedback information perfectly. In discontinuous mode, the offset voltage has some difference with the feedback information because there is some resonance after the transformer current reaches zero as shown in Fig. 11. There can be some difference in the OLP current level between CCM and DCM, but the difference is not great.

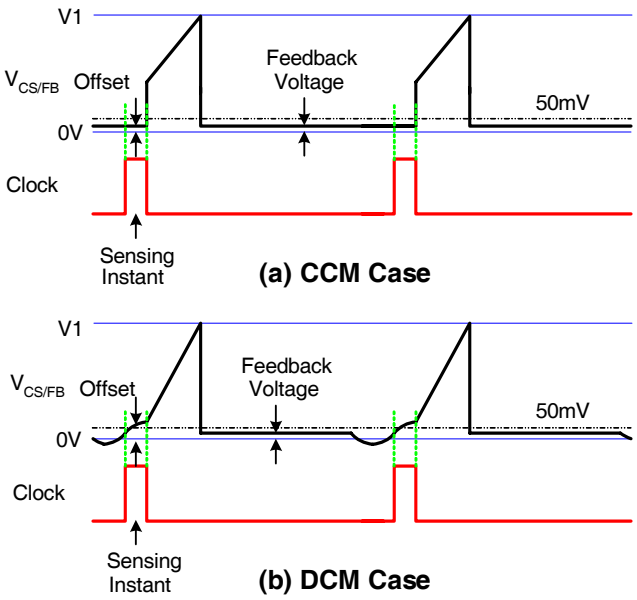


Figure 11. OLP Waveforms

2.5 Burst Mode

The FAN7602 contains the burst mode block to reduce the power loss at a light load and no load like the FAN7601. A hysteresis comparator senses the offset voltage of the Burst+ for the burst mode sensing, as shown in Fig. 12. The Burst+ is the sum of the CS/FB voltage and Plimit offset voltage. The FAN7602 enters the burst mode when the offset voltage of the Burst+ is higher than 0.95V and exits the burst mode when the offset voltage is lower than 0.88V. The offset voltage is sensed during the switch off-time. In the burst mode block, there are four switching cycles of delay to filter the noise entering the burst mode. By this burst mode, under 1W power consumption can be achieved in the stand-by mode. Figure 13 shows typical burst mode waveforms. The input power with 0.5W load is under 1W when the input voltage is 265Vac.

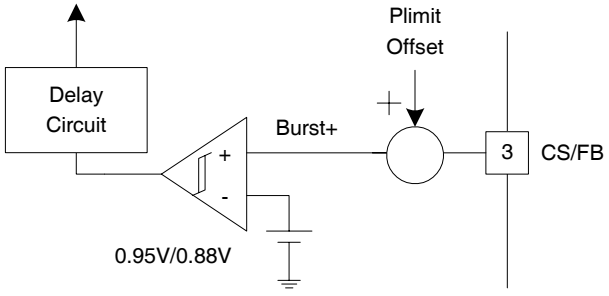


Figure 12. Burst Mode Block

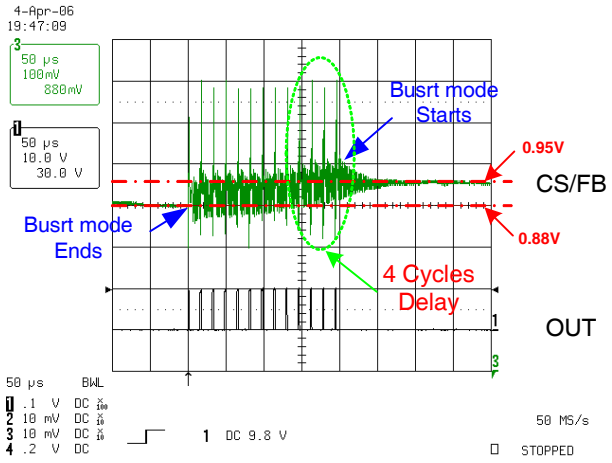


Figure 13. Typical Burst Mode Waveforms

2.6 Line Under-Voltage Protection

If the input voltage of the converter is lower than the minimum operating voltage, the converter input current increases too much, causing component failure. Therefore if the input voltage is low, the converter should be protected. In the FAN7602, the LUVP circuit senses the input voltage using the LUVP pin and if this voltage is lower than 2V, LUVP signal is generated. The comparator has 0.5V hysteresis. As shown in Fig. 14, the LUVP pin needs a filter capacitor to filter the input voltage ripple. If this filter is not enough, the LUVP function works unintentionally at lowest input voltage. The filter time constant is R_{in1}*C_{in} because R_{in2} is much higher than R_{in1} and a proper value for the time constant is about 10ms. Because R_{in2} value must be high to reduce the power loss, a 10MΩ resistor is used in the demo board. R_{in1} and C_{in} values can be calculated by (3). If the minimum AC line voltage is 85Vac, the calculated R_{in1} is 167kΩ and the used value is 180kΩ. Figure 15 shows a typical start-up waveform of the LUVP pin when the line voltage is 85Vac and the output load is 4A. Before the IC starts switching, the DC_link voltage is the peak value of the AC line voltage, 118.3V. If the IC starts switching, the DC_link voltage has a ripple and the minimum voltage of the DC_link voltage drops by 22% of the peak value. The LUVP pin voltage drops by 13% of the peak value, from 2.05V to 1.78V, due to the averaging effect of the filter. The LUVP protection works when the AC line voltage is 72Vac at full load. If a RC filter with 5ms time constant is used, the LUVP protection level is increased to 73Vac because the ripple of the LUVP pin voltage increases.

$$R_{in1} > \frac{2 \cdot R_{in2}}{\sqrt{2} \cdot V_{line}}\min \qquad C_{in} \approx \frac{10ms}{R_{in1}} \qquad (3)$$

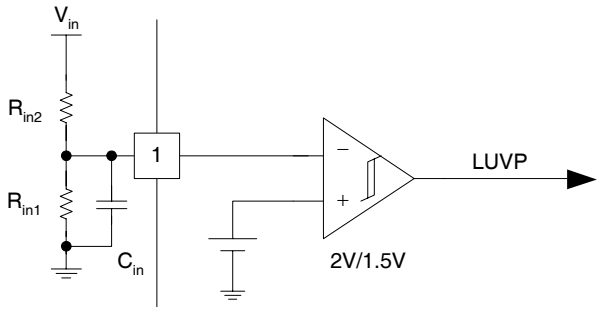


Figure 14. LUVP Circuit

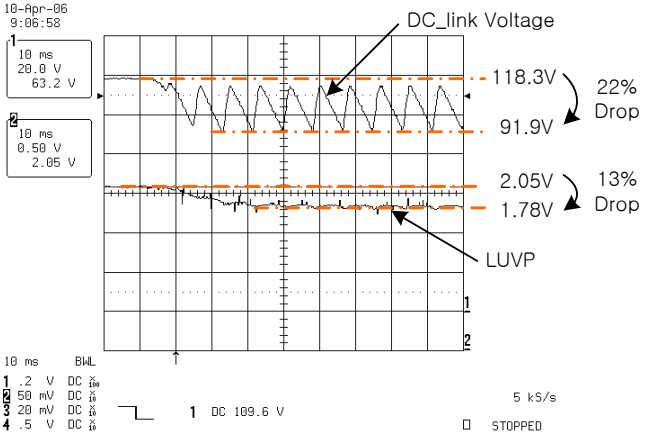


Figure 15. LUVP Start-up Waveform

If the LUVP signal is generated, IC output is shut down, then the output voltage feedback loop is saturated and the OLP works. If the LUVP condition persists more than 22ms, the protection is reset by UVLO. If the LUVP time is less than 22ms, the LUVP is released by the LUVP comparator, as shown in Fig. 16.

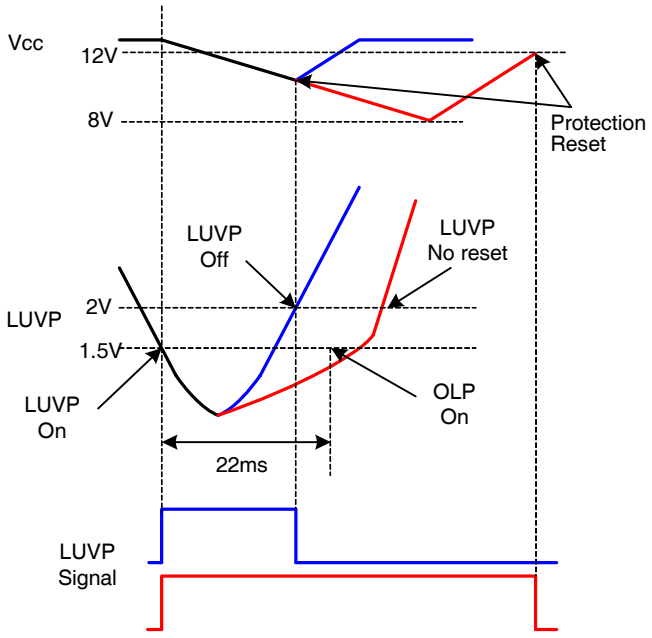


Figure 16. LUVP Waveforms

2.7 Latch Protection

The latch protection is provided to protect the system against abnormal conditions using the Latch/Plimit pin. The Latch/Plimit pin can be used for the output over-voltage protection or other protections. If the Latch/Plimit pin voltage is made higher than 4V by an external circuit, the IC is shut down. The latch protection is reset when the V_{CC} voltage is lower than 5V.

Figure 17 shows an output over-voltage protection circuit. If the output voltage exceeds the sum of the zener diode voltage and the photo coupler forward voltage drop, the capacitor is charged. If the Latch/Plimit pin voltage is higher than 4V, the IC is shut down.

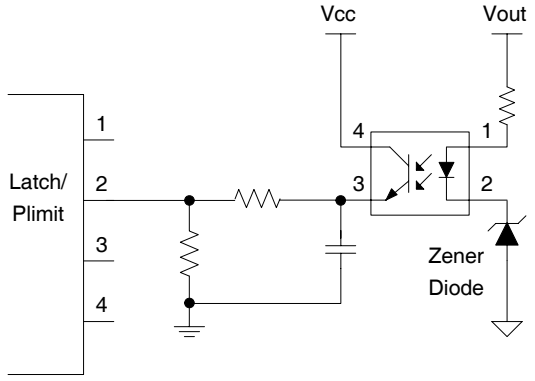


Figure 17. Output Over-Voltage Protection Circuit

2.8 Output Drive

The FAN7602 contains a single totem-pole output stage, designed specifically for a direct drive of a power MOSFET. The drive output is capable of up to peak 450mA sourcing current and peak 600mA sinking current with typical rise and fall times of 45ns and 35ns respectively with a 1nF load. The output drive capability can be improved by adding one PNP bipolar transistor, as shown in Fig. 18.

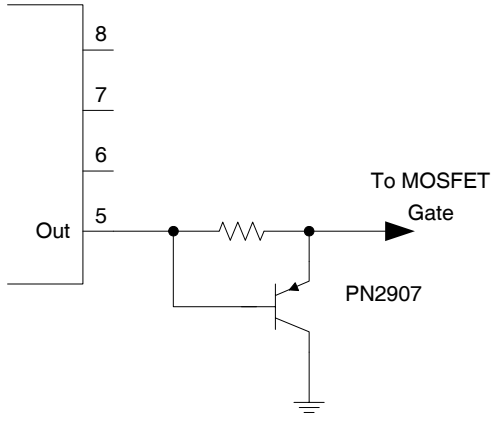


Figure 18. Circuit to Improve the Turn-off Characteristic

3. Design Method

The design method of the flyback converter is well described in the FPS (Fairchild Power Switch) application note AN4137; therefore the detailed design guide lines are not included in this application note. Please refer to AN4137 for more information.

Because the main differences between FPS and FAN7602 are the feedback circuit and MOSFET current sensing, the feedback loop design method and current sensing resistor selection guide-lines are included.

Some design considerations, such as snubber design and PCB layout recommendation, are described as well.

3.1 MOSFET Current Sense Resistor Selection

Once the turns ratio of the transformer is determined, the peak MOSFET current can be calculated. The sensed current information must be lower than 1V. If the resistance is too high, the required output power cannot be delivered because the MOSFET current is limited to a lower value. The resistance can be determined by (4) if the power limit function is not used grounding the Latch /Plimit pin.

$$R_S < \frac{1V \cdot (R_{FB} + R_F)/R_{FB}}{\frac{P_{in}}{Vdc\_\min \cdot D_{\max}} + \frac{Vdc\_\min}{2L_m} \cdot \frac{D_{\max}}{fsw}} \quad (4)$$

If the power limit function is used, the OCP level decreases from 1V to 1V- $V_{Latch/Plimit}$*K_{Plimit}. The current sense resistor should be determined by (5) at the lowest input line.

$$R_S < \frac{(1V - V_{Latch/Plimit} \cdot K_{Plimit}) \cdot (R_{FB} + R_F)/R_{FB}}{\frac{P_{in}}{Vdc\_\min \cdot D_{\max}} + \frac{Vdc\_\min}{2L_m} \cdot \frac{D_{\max}}{fsw}} \quad (5)$$

3.2 Feedback Loop Design

Because the current sensing and output voltage feedback is performed using one pin, the CS/FB pin, the control loop design is somewhat different from that of FPS.

For CCM operation, the control to output transfer function of the flyback converter using current mode control is given by (6).

$$G_{VC} = \frac{\hat{v}_O}{\hat{v}_{FB}} = \frac{R_L V_{DC}(N_P/N_S)}{Rs(2V_{RO}+V_{DC})} \cdot \frac{(1+s/w_z)(1-s/w_{rz})}{1+s/w_p} \quad (6)$$

The definitions of the symbols are shown in AN4137. The pole and zeros of (6) are defined as follows.

$$w_Z = \frac{1}{R_e C_O}, w_{rz} = \frac{R_L (1\text{-}D)^2}{D L_m (N_S / N_P)^2} \quad \text{and } w_p = \frac{(1+D)}{R_L C_O} \tag{7}$$

where, R_e is the ESR of C_o.

The transfer function of the feedback compensation network shown in Fig. 19 is obtained by (8).

$$\frac{\hat{v}_{FB}}{\hat{v}_O} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + s/w_{pc}} \tag{8}$$

where,

$$w_i = \frac{R_F}{R_1 R_G C_F}, w_{zc} = \frac{1}{(R_C + R_1) C_C}, w_{pc} = \frac{1}{R_F C_F}$$

As described in AN4137, the stability over all the operating ranges can be guaranteed by designing the feedback loop with more than 45 degrees of phase margin in low input voltage and full load condition.
The procedure to design the feedback loop is as follows, as described in AN4137.

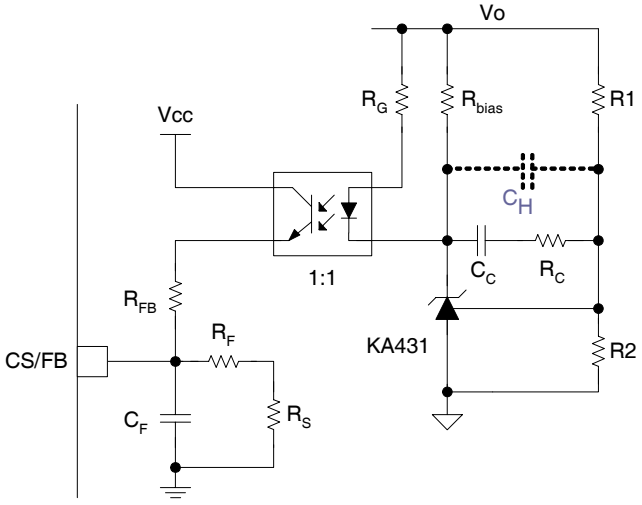


Figure 19. Output Voltage Compensation Circuit

(a) Determine the crossover frequency (f_c). For CCM fly back, set f_c below 1/3 of RHP (right half plane) zero to minimize the effect of the RHP zero. For DCM, f_c can be placed at a higher frequency, since there is no RHP zero.

(b) When an additional LC filter is employed, the crossover frequency should be placed below 1/3 of the corner frequency of the LC filter, since it introduces a -180 degrees phase drop. Never place the crossover frequency beyond the corner frequency of the LC filter. If the crossover frequency is too close to the corner frequency, the controller should be designed to have a phase margin greater than 90 degrees when ignoring the effect of the additional LC filter.

(c) Determine the DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at f_c.

(d) Place a compensator zero (f_{zc}) around f_c /3.

(e) Place a compensator pole (f_{pc}) around $3f_c$. As shown in (6), the compensator pole is placed by the current sense RC filter, R_F and C_F. There can be some restriction choosing R_F and C_F values because of the RC filter's delay time. Then f_{pc} is placed at much higher frequency than $3f_c$. In that case, the high-frequency switching noise might not be filtered, causing system instability. If the RC filter is not enough as a compensator pole, C_H should be added, as shown in Fig. 19. The value of C_H should be around 1/10 of C_C. If there is no problem without C_H, C_H is not necessary.

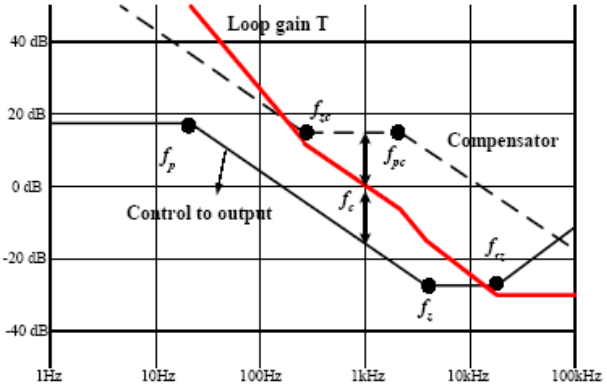


Figure 20. Compensator Design

When determining the feedback circuit components, there are some restrictions, detailed below.

(a) The voltage divider network of R1 and R2 should be designed to provide 2.5V to the reference pin of the KA431. If the resistance of R1 is too low, the power loss of the voltage divider increases and this loss increases the stand-by power. To limit the power loss of the voltage divider less than 5mW, R1 should be selected by (9) and R2 is given by (10).

$$R1 \geq \frac{V_O \times (V_O\text{-}2.5)}{5\text{mW}} \tag{9}$$

$$R2 = \frac{2.5 \times R1}{V_O\text{-}2.5} \tag{10}$$

(b) The FAN7602 does not contain the LEB circuit, but an RC filter should be used to filter the turn-on switching noise and to add the MOSFET current sense information and the feedback information. The RC time constant should be 100ns~300ns, according to the output power. R_F determines the maximum I_{FB} current level. The offset

of the CS/FB pin voltage is maximum when the output load is no load and the average offset voltage is around 1V. V_{CC} must supply 1V/R_F current to control the offset voltage constantly. If R_F value too low, V_{CC} voltage drops too much and then UVLO works. R_F should be high enough; 1kΩ is appropriate for R_F limiting V_{CC} supply current under 1mA, then C_F ranges from 100pF to 330pF. The RC filter causes some sensing delay, so the peak value of the filtered information is less than that of the real current information. The higher capacitance causes the more difference as shown in Fig. 21. The red dotted line is the current waveform when the capacitance is low and the blue dotted line is the current waveform when the capacitance is high. Because the real current peak of the blue line is higher than that of the red line, more energy is transferred to the secondary side. The stand-by power is lower with higher capacitance. If the capacitance is too high, there can be an audible noise problem.

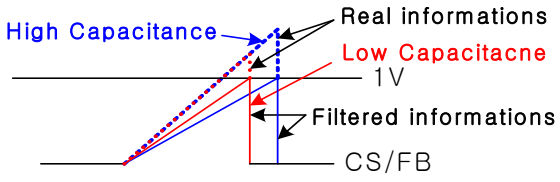


Figure 21. Current Sense Waveforms

(c) According to the load condition of the converter, the feedback current (I_{FB}) changes to control the output voltage constantly, as shown in Fig. 22. The CS/FB voltage is around 1V at no load condition. If the CS/FB voltage is 1V, I1 is 1V/(R_F+R_S) and I_{FB} should equal to I_1. If I_{FB} flows through R_{FB}, it causes a voltage drop, V_{Rfb}. If the value of R_{FB} is too high, then the output voltage is not regulated at no load because the offset voltage of the CS/FB pin is lower than necessary because V_{Rfb} is too high.

$$R_{FB} = \frac{6V}{1V} R_F \qquad (11)$$

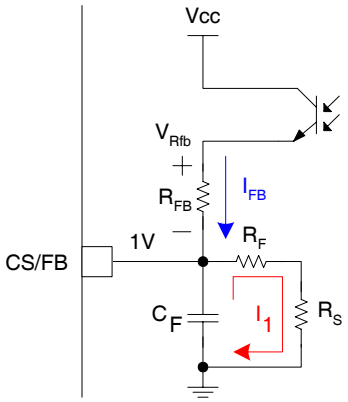


Figure 22. R_{FB} Selection Method

If the value of R_{FB} is too low, there can be delay of feedback loop during load step change. R_{FB} should be designed by (11), considering V_{CC} minimum voltage of 8V and considering 2V margin. If R_F value is 1kΩ, R_{FB} value should be 6kΩ.

(d) The resistors R_{bias} and R_G should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage. In general, the minimum cathode voltage and current for the KA431 are 2.5V and 1mA, respectively. Therefore, R_{bias} and R_G should be designed to satisfy the following conditions:

$$\frac{V_O - V_{OP} - 2.5}{R_G} > \frac{1V}{R_F} \qquad (12)$$

$$\frac{V_{op}}{R_{bias}} > 1mA \qquad (13)$$

where, Vop is opto-diode forward drop.

3.3 V_{CC} Circuit Design

An adequate IC supply voltage is 12V, considering the minimum operating voltage of 8V and the over-voltage protection level of 19V. The V_{CC} voltage is supplied by the V_{CC} winding and it varies according to the input voltage and output load condition. The V_{CC} voltage is lowest when the input voltage is highest and the load is no load. The V_{CC} voltage is highest when the input voltage is lowest and the load is full load. The number of V_{CC} winding can be obtained by considering the ratio of the output voltage and V_{CC} voltage. After determining the number of V_{CC} winding, R_{Vcc} should be optimized to cover the entire operating range. If the V_{CC} voltage falls below 8V and enters into UVLO operation, even the R_{Vcc} is zero, the number of V_{CC} winding should be increased. If the number of V_{CC} winding is increased, V_{CC} voltage can reach OVP level at full load. Therefore R_{Vcc} should be optimized to cover the entire operating range after changing the number of V_{CC} winding. If it is impossible to find out proper R_{Vcc} value, a resistor and a zener diode can be used as shown in Fig. 23 to slow down the increase of the V_{CC} voltage. R_Z should be optimized if the OVP function is necessary. Too small R_Z could clamp the V_{CC} voltage much lower than the OVP level disabling the OVP function and too large R_Z could make the OVP work in normal operating range.

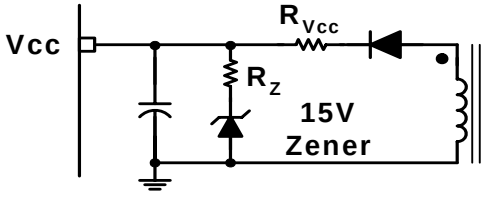


Figure 23. Zener Clamped V_{CC} Circuit

Another circuit for preventing OVP operation at full load is

shown in Fig. 24. A resistor is connected between MOSFET gate and ground to increase V_{CC} current when duty increases. Too small R_d can cause UVLO operation at no load and too large R_d can cause OVP operation at full load.

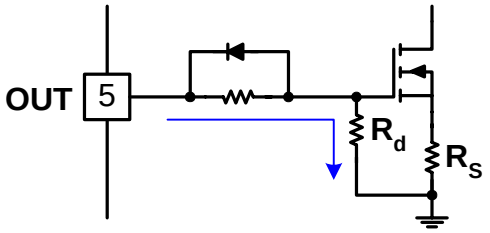


Figure 24. Dummy Resistor Connection

3.4 Diode RC Snubber Design

The snubber of the secondary diode can be designed by the following steps.

(a) Measure the original resonance period (Tr) of the diode voltage without RC filter, as shown in Fig. 25.

(b) Find a capacitor (Cdsn) value that makes the resonance period double (2*Tr) when connected in parallel with the diode, as shown in Fig. 26.

(c) Calculate the snubber resistor (Rdsn) by (14).

$$Rdsn = \frac{3 \cdot Tr}{2\pi \cdot Cdsn} \quad (14)$$

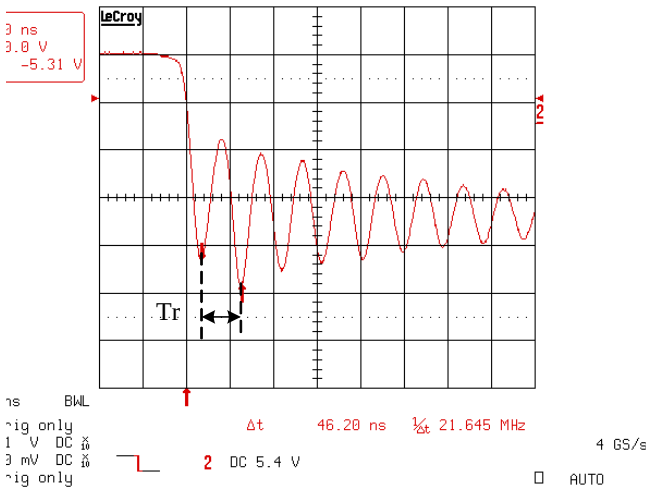


Figure 25. Diode Voltage without C_{dsn}

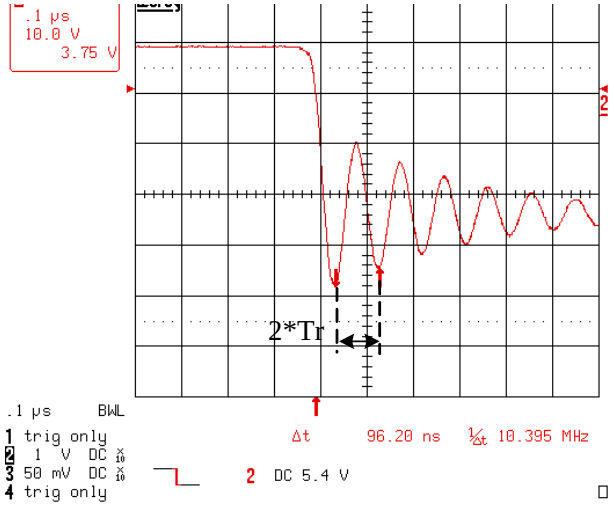


Figure 26. Diode Voltage Connecting C_{dsn}

3.5 MOSFET RCD Snubber Design

AN4147 describes the design guidelines for RCD snubber of the flyback converter, but it does not consider the snubber capacitance of the secondary diode and the MOSFET Coss. In a real case, when the MOSFET turns off, the energy stored in the leakage inductance discharges the snubber capacitor of the secondary diode and the MOSFET Coss until Vds is charged to Vin + nVo. During this discharging time, the energy stored in the leakage inductance decreases and the peak value of the snubber charging current decreases from Ipeak to Isn_peak, as shown in Fig. 28. Therefore the peak voltage of the snubber is lower than the calculated value, using the equations in AN4147. If you use the values calculated by AN4147, the snubber design is most conservative. Use the values calculated by AN4147, then increase R_{SN} value step by step, checking the voltage of the C_{SN} to reduce the power loss of the R_{SN}. If R_{SN} is too high, the MOSFET V_{ds} voltage spike is too high. The MOSFET V_{ds} voltage should not exceed the MOSFET rating even though the converter output is shorted.

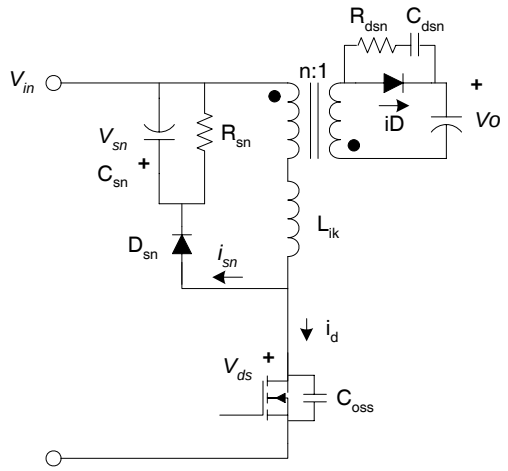


Figure 27. Flyback Converter with Snubbers

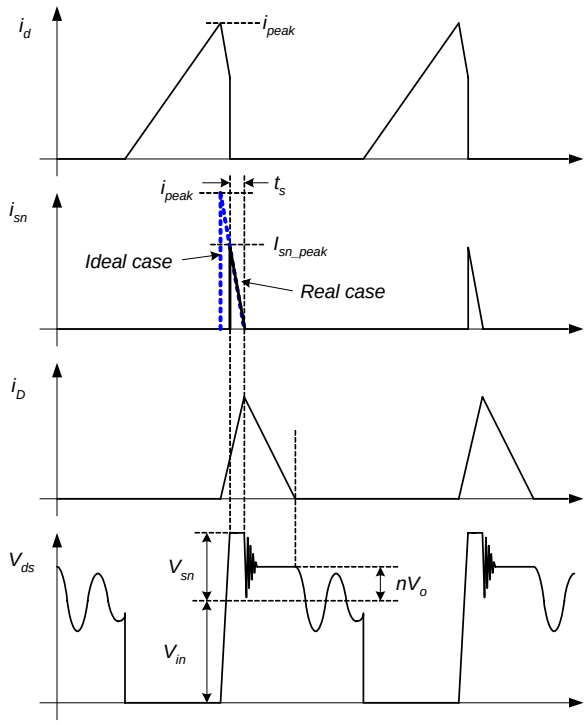


Figure 28. Waveforms Related with RCD Snubber

3.6 Transformer Audible Noise

Because the FAN7602 operates in the burst mode at a light load and no load, it has a switching period and a non-switching period. Figure 29 shows the gate voltage and the output voltage at no load. The burst operation frequency is about 82~100Hz. The burst operation frequency varies according to the load condition and the frequency is in the range of the audible frequency. Therefore the transformer may generate the audible noise. Because the audible noise comes from the movement of the transformer coils, it is important to prevent the movement of the coils. Varnishing the transformer tightly helps reduce the audible noise. If the varnishing is not tight, there can be some audible noise. If the current sense filter size decreases, the MOSFET current peak decreases then audible noise decreases, but the stand-by power increases.

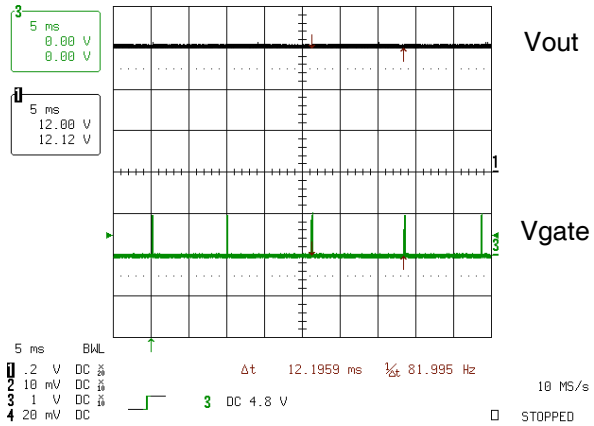


Figure 29. Burst Mode Operation Waveforms

For more information, please refer to AN4148.

3.7 Power Limit Resistors Design

If the flyback converter operates in CCM mode, the maximum output current increases as the input voltage increases. Figure 30 shows the CS/FB pin voltage when the input voltage is 85Vac and Fig. 31 shows the CS/FB pin voltage when the input voltage is 265Vac with 4A load. With the same output load, the feedback offset voltages are different. One is 236mV and the other is 418mV; a difference of 182mV. This means that more current can be delivered when the input voltage is 265Vac, compared with the 85Vac case, because the feedback offset voltage decreases as the output load increases. The maximum currents when the input voltages are 85Vac and 265Vac, are 5A and 7A respectively. The Plimit offset voltage should be subtracted from 1V as shown in Fig. 8.

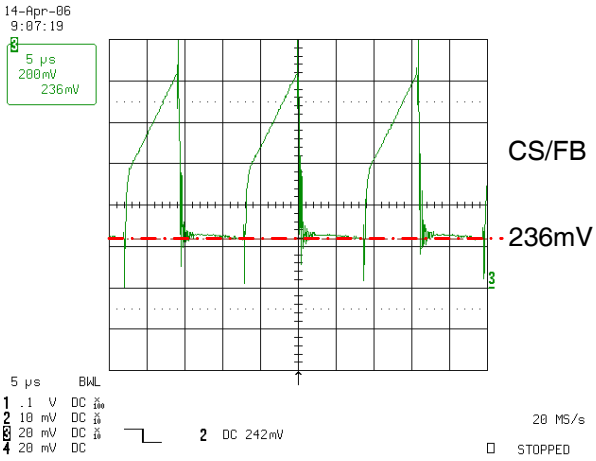


Figure 30. CS/FB Waveform (Io=4A, Vin=85Vac)

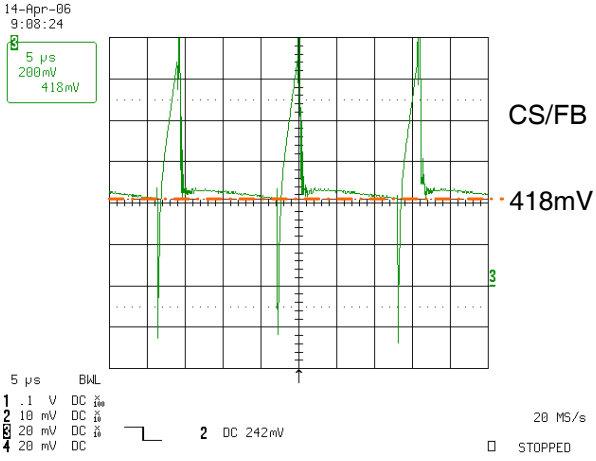


Figure 31. CS/FB Waveform (Io=4A, Vin=265Vac)

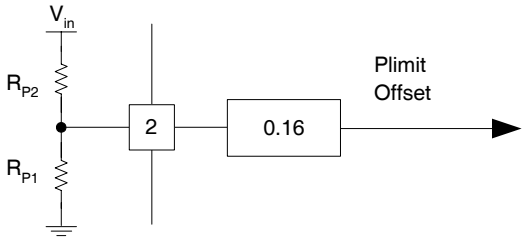


Figure 32. Power Limit Circuit

The power limit resistor value can be obtained by (15) considering 200ns turn-off delay.

$$R_{P1} = \frac{1 - R_S \cdot (I_{pk}^{Vdc\_max} - Vdc\_max / L_m \cdot 200ns) \cdot \frac{6}{7}}{0.16 \cdot Vdc\_max} \cdot R_{P2} \quad (15)$$

3.7 Layout Recommendation

The PCB layout is very important for analog power applications. For stable operation, the power ground and the signal ground should be connected only at the GND pin and the power ground line should be thick enough, as shown in Fig. 33.

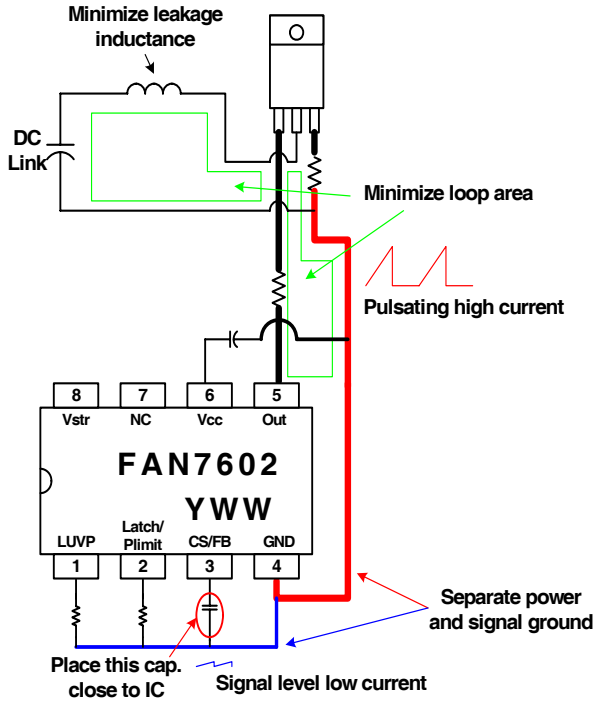


Figure 33. PCB Layout Recommendation

If the power ground and the signal ground are mixed as shown in Fig. 34, the IC can work abnormally.

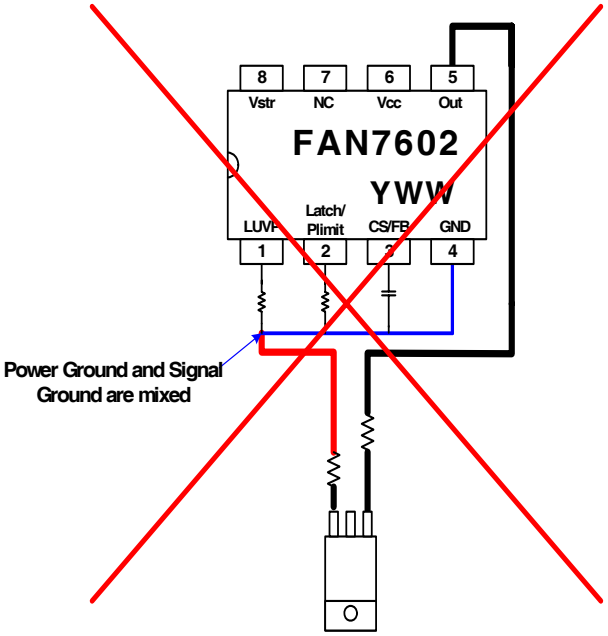


Figure 34. Bad PCB Layout Example

4. Design Example

A 48W adapter, using the flyback topology, is designed to illustrate the design procedure. The system parameters used for the design are as follows:

- Maximum output power (Po): 48W
- Input voltage range: 85Vrms~265Vrms
- Output voltage (Vo): 12V
- AC line frequency (fac): 60Hz
- Adapter efficiency (η): > 80%
- DC link capacitor: 150μF
- Maximum duty: 45%
- Ripple factor: 0.39
- Saturation flux density: 0.26T
- V_{CC} voltage: 12V
- Maximum Vsn: 150V

Figure 35 shows the designed application circuit diagram. Table 1 shows the test results and table 2 shows the 48W adapter demo board components list. As can be seen in the table, the input power is less than 0.3W in the whole input voltage range at no load. The power is measured with a power meter from Voltech, PM3000A.

Table 1. Experimental Results

	Input Power			
Output Power	**85Vac**	**110Vac**	**220Vac**	**265Vac**
No load	99.6mW	107.8mW	173.3mW	213.5mW
0.5W	770.4mW	778.9mW	862.8mW	907.1mW
OLP Point	4.32A	4.59A	4.4A	4.14A

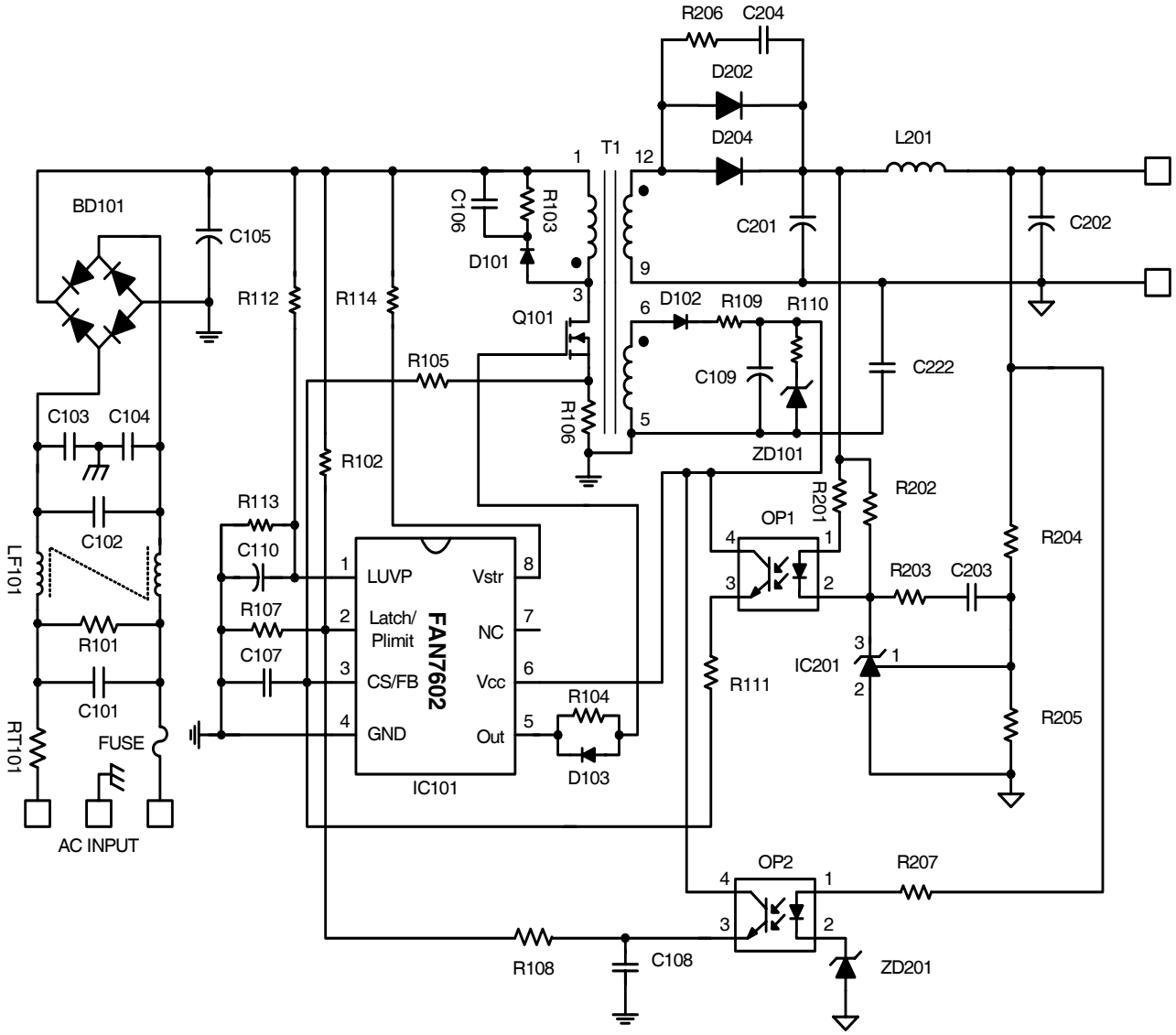
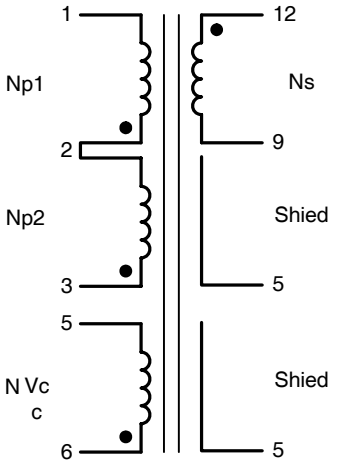


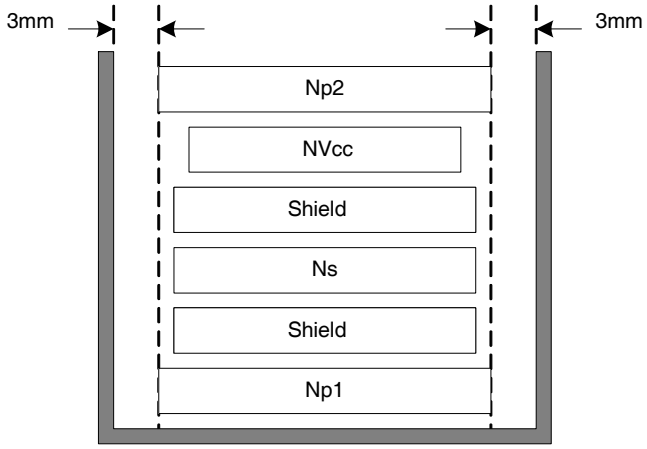
Figure 35. Application Circuit Diagram

Table 2. 48W Adaptor Demo Board Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			**Capacitor**		
FUSE	1A/250V		C101	220nF/275V	Box Cap.
NTC			C102	150nF/275V	Box Cap.
RT101	5D-9		C103, C104	102/1kV	Ceramic
Resistor			C105	150μF/400V	Electrolytic
R102, R112	10MΩ	1/4W	C106	103/630V	Film
R103	56kΩ	1/2W	C107	271	Ceramic
R104	150Ω	1/4W	C108	103	Ceramic
R105	1kΩ	1/4W	C109	22μF/25V	Electrolytic
R106	0.5Ω	1/2W	C110	473	Ceramic
R107	56kΩ	1/4W	C201, C202	1000μF/25V	Electrolytic
R108	10kΩ	1/4W	C203	222	Ceramic
R109	0Ω	1/4W	C204	102	Ceramic
R110	1kΩ	1/4W	C222	222/1kV	Ceramic
R111	6kΩ	1/4W	**MOSFET**		
R113	180kΩ	1/4W	Q101	FQPF8N60C	Fairchild
R114	50kΩ	1/4W	**Filter**		
R201	1.5kΩ	1/4W	LF101	23mH	0.8A
R202	1.2kΩ	1/4W	L201	10μH	4.2A
R203	20kΩ	1/4W	**Diode**		
R204	27kΩ	1/4W	D101, D102	UF4007	Fairchild
R205	7kΩ	1/4W	D103	1N5819	Fairchild
R206	10Ω	1/4W	D202, D204	FYPF2010DN	Fairchild
R207	10kΩ	1/4W	ZD101, ZD201	1N4744	Fairchild
IC			BD101	KBL06	Fairchild
IC101	FAN7602	Fairchild	**TNR**		
IC201	KA431	Fairchild	R101	471	470V
OP1, OP2	H11A817B	Fairchild			

5. Transformer Specification





5.1 Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Np1	3 → 2	$0.3^{\phi} \times 2$	31	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 2 Layers				
Shield	5	Copper Tape	0.9	Not Shorted
Insulation: Polyester Tape t = 0.03mm, 2 Layers				
Ns	12 → 9	$0.65^{\phi} \times 3$	10	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 2 Layers				
Shield	5	Copper Tape	0.9	Not Shorted
Insulation: Polyester Tape t = 0.03mm, 2 Layers				
N_{Vcc}	6 → 5	$0.2^{\phi} \times 1$	10	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 2 Layers				
Np2	2 → 1	$0.3^{\phi} \times 2$	31	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.03mm, 2 Layers				

5.2 Electrical Specification

	Pin	Value	Remarks
Inductance	1 - 3	600μH	100KHz, 1V
Leakage	1 - 3	15μH	2nd shorted

- Core: EER2828
- Bobbin: EER2828
- Ae: 82.1 [mm^2]

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