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Application Note 6004

500W Power-Factor-Corrected (PFC) Converter Design with FAN4810

This application note describes the theory of operation and step-by-step process to design a high performance Power Factor Corrected (PFC) power supply using the FAN4810 controller IC. A complete application circuit is shown in Figure 10 and an evaluation board using this design is available from Fairchild Sales. The evaluation board provides 500W at 400VDC and 1.25A, while operating from 90V to 264VAC line input.

Selection of Power Train Components

The FAN4810 can be used in any active PFC pre-regulator employing Continuous Conduction Mode (CCM) that has to comply with the IEC 3000-3-2 standard. This section of the application note covers calculation parameters and selection of pre-regulator power train components: boost inductor, output capacitor and semiconductors.

Selecting the Value of the Boost Inductor

The FAN4810 operates in a continuous conduction code to minimize peak current and maximize available power. The value boost inductance found by setting ΔI, the peak-to- peak value of high-frequency current, is typically in the area of 20% of the peak value of the maximum line current.

$$I_{\_LINE\_PK} = \frac{\sqrt{2}P_{IN}}{V_{MIN}} \quad (1) \qquad P_{IN} = \frac{P_O}{\eta} \quad (2)$$

Where $I_{\_LINE\_PK}$ is a peak value of input current occurred at low line, V_{MIN} is RMS value of minimum line voltage, P_O is output power and η is efficiency. Value $I_{\_LINE\_PK}$ will define value of ΔI , where dI is the specified percentage rate. I_L_{MAX} is the inductor maximum current.

$$\Delta I = dI \times I_{\_LINE\_PK} \quad (3)$$

$$I\_L_{MAX} = I_{\_LINE\_PK} + \frac{\Delta I}{2}$$

Another factor influencing inductor selection is duty cycle **D** and switching frequency $\mathbf{f_S}$.

$$D = \frac{V_O - \sqrt{2}V_{MIN}}{V_O} \quad (4) \qquad L = \frac{D \times \sqrt{2}V_{MIN}}{f_S \times \Delta I} \quad (5)$$

Selecting the Value of the Bulk Capacitor

A major factor affecting bulk capacitor selection is hold up time (T_{hld}). "Hold-up-time" is a time during which output of power supply remains in specified range, after interruption of AC power. Energy J_{thd} stored in the bulk capacitor supplies the down-steam converter during power disruption. Voltage across bulk capacitor drops during hold-up time, as capacitor discharges. You should calculate the minimum bus voltage $\mathbf{V_{O\_MIN}}$, where output voltage stays in regulation, transformer properly resets and components stress are inside the derating guidelines.

$$J_{THD} = P_O \times T_{HLD} \quad J_{THD} = \frac{1}{2}(C \times V_O^2 - C \times V_{O\_MIN}^2)$$

$$C = \frac{2 \times P_O \times THLD}{V_O^2 - V_{O\_MIN}^2} \quad (6)$$

Setting the Oscillator Frequency

Resistor R6 and capacitor C18 set the oscillator frequency. Let's assume a value of C18 = 470 pF. The following equation determines the value of R6

$$R6 = \frac{1}{C18 \times 0.51 \times f_S} \quad (7)$$

Selecting Parameters of Gain Modulator Input Circuits

The FAN4810 Gain Modulator employs three inputs:

1. **A current representing a profile of input voltage**. This current is proportional to the instantaneous value of the input voltage at any given time. This current programmed by resistor R1, see Fig 1.

2. **A voltage proportional to the average value of the line voltage**. To obtain this voltage the input voltage is filtered and scaled. A two-stage filter consists of resistors R2,R3,R4 and capacitors C2,C3.

3. **Output of voltage error amplifier**.

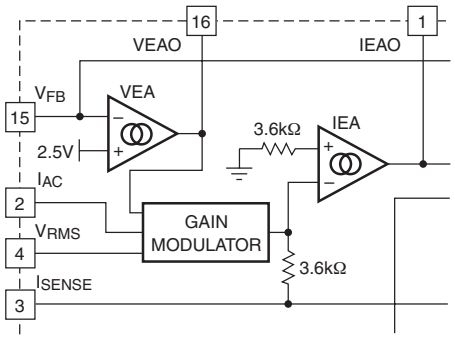

Figure 1. Gain Modulator and Voltage Error Amplifier

The program resistor for Pin 2 (I_{AC}) current input of the Gain Modulator is based on the following formula:

$$R1 \geq \frac{\sqrt{2} \times V_{MIN} \times G_{MAX} \times R_{MO}}{V_{GM\_OUT\_MAX}} \quad (8)$$

Where $\mathbf{G_{MAX}}$ is the maximum gain of the Gain Modulator, $\mathbf{R_{MO}}$ is the output resistor of Gain Modulator and $\mathbf{V_{GM\_OUT\_MAX}}$ is the maximum output voltage of the Gain Modulator. See the FAN4810 Datasheet for reference.

The voltage divider and necessary filters for providing the scaled value of average input voltage for the Gain Modulator Pin 4 (V_{RMS}) input are shown in Figure 2.

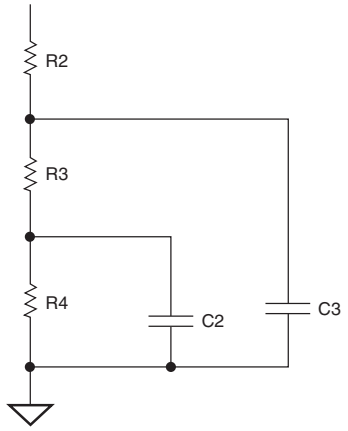

Figure 2. Two-Stage Filter Schematic

This resistive divider ratio should provide 1.1V at the lowest line voltage. The value of 1.1V is chosen based on the FAN4810 datasheet and Gain Modulator Transfer Characteristic presented in Figure 3. The characteristic curve includes two segments: the right segment is the area of normal operation conditions with line voltages from 80VAC to 264VAC and the left segment is the area of brown-out conditions where the line voltage drops below 80VAC. Maximum gain occurs at V_{RMS}(V) =1.1V, see curve in Figure 3. The V_{RMS}(V) of 1.1V, corresponding to the maximum gain, defines the criteria selection or resistor divider.

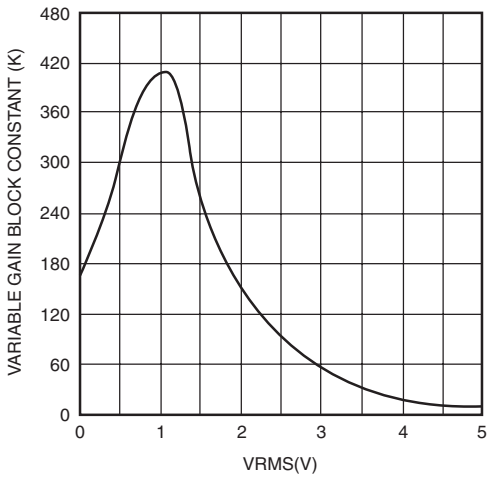

Figure 3. Gain Modulator Transfer Characteristic

The voltage at Pin 4 sets V_{RMS} and must be well-filtered and yet able to respond well to transient line voltage changes. A two-stage RC low pass filter consisting of R2, R3, R4, C3 and C2 as shown in Figure. 2 is selected to meet this requirement. The resisitive divider ratio gives an average DC voltage of 1.1 volts at Pin 4 at minimum line voltage.

$$V_{AV} = \frac{2}{\pi}\sqrt{2}V_{MIN} \quad (9)$$

Vav is the value of average line voltage and V_{MIN} is the minimum RMS value of line voltage. Assume R2=R1 and R3=100k. These values are a common choice for Fairchild PFC applications.

$$I_{RD1} = \frac{V_{AV} - V_{GM\_IN\_MAX}}{R2 + R3} \quad (10) \qquad R4 = \frac{V_{GM\_IN\_MAX}}{I_{RD1}} \quad (11)$$

Where $V_{GM\_IN\_MAX}$ =1.1V and I_{RD1} is the current flowing through the divider.

$$R_{TOTAL} = R2 + R3 + R4 \quad (12)$$

$$C3 = \frac{R_{TOTAL}}{2 \times \pi \times f1 \times R2(R3 + R4)} \quad (13)$$

$$C2 = \frac{\left(1 + \frac{R4 \times R_{TOTAL}}{R2(R3 + R4)}\right)}{2 \times \pi \times f2 \times R4} \quad (14)$$

Two poles circuits presented in Figure 2 has demonstrated good performance with f_1 = 15Hz and f_2 = 23Hz.

Selection Parameters of Current Sense Circuit

A current sense circuit includes a current sense resistor and a filter.

Selection of Current Sense Resistor

The voltage drop across the current sense resistor should not exceed the maximum output voltage of the gain modulator, whose output is connected to the inverting input of the current error amplifier. See Figure 5. The non-inverting input of the current error amplifier is connected to the ground and its inverting input acts as a summing node for summing the Gain Modulator output with the negative voltage on the current sense resistor as shown in Figure 4.

$$R5 = \frac{V_{GM\_OUT\_MAX}}{I\_L_{-MAX}} \quad (15) \qquad I\_L_{-MAX} = I_{-LINE\_PK} + \frac{\Delta I}{2}$$

Selection of Current Sense Filter

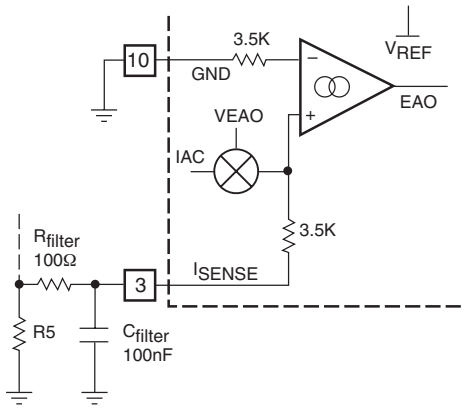

Figure 4: Current Sense Amplifier Circuit

The current sense filter is needed to protect the I_{sense} pin from voltage surges at start-up caused by a high inrush current and to enhance Total Harmonic Distortion (THD) performance when a small boost inductor is used and is operating in Discontinuous Conduction Mode (DCM) at light loads.

$$f\_cf = \frac{1}{2 \times \pi \times R16 \times C19} \quad (16)$$

The f_cf filter frequency should be set between f_S and $f_S/6$; $f_S/6 < f\_cf < f_S$.
R16 = 100 Ω or less is recommended.

Selection Parameters of Current Error Amplifier Compensation Network

The FAN4810 employs two control loops for power factor correction: a current control loop and a voltage control loop. The current control loop shapes current based on the reference signal from the I_{AC} Pin 2. The voltage loop stabilizes output voltage and defines THD balance.

The output of the Gain Modulator is a current proportional to the output of the error amplifier and full sine current I_{AC} on Pin 2 and is inverse-proportional to the V_{RMS} voltage on Pin 4. Output current of the Gain Modulator generates a voltage on internal resistor R_{MO} (3.6k). This voltage subtracts from the voltage on sense resistor R5. The difference between the resulting voltage on the inverting pin of the current error amplifier and virtual ground on the non-inverting pin generates an output voltage that is applied to the non-inverting input of comparator. The ramp signal applied to the inverting input of the comparator controls the output signal on Pin 12. For example, if the output voltage is decreasing, the output of the current error amplifier increases the duty cycle. Increasing the duty cycle will in turn increase the output voltage, thereby closing the control loop.

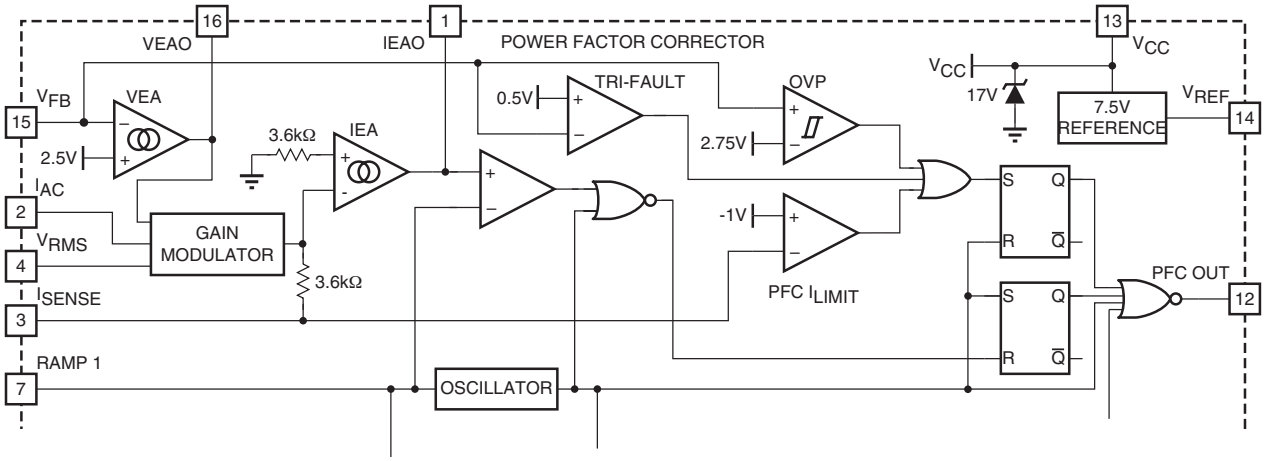

Figure 5. FAN4810 PFC Block Diagram

Figure 6 shows a simplified block-diagram of the current control loop. The PWM block is comprised of a comparator, flip-flop and output MOSFET driver. The voltage-controlled voltage source combines input voltage source, rectifier, MOSFET, and boost diode. The current control loop is closed around the LR5 pole, essentially eliminating the inductor from consideration during voltage control loop analysis.

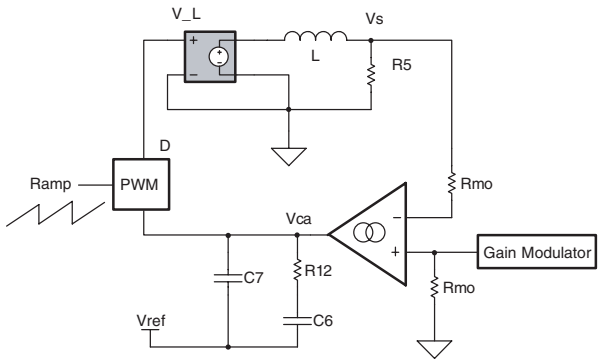

Figure 6. Simplified Diagram of Current Loop

Now determine the transfer function between Vs on the sense resistor and V_{CA} output of the current amplifier or transfer function of open loop system. This transfer function will be a combination of the transfer function of the boost and PWM blocks of the open loop system.

The duty cycle, voltage applied to the boost inductor, and the inductor current are determined by the following expressions:

$$D = \frac{V_{CA}}{V_{RAMP}} \qquad V\_L = D \times V_O \qquad I\_L = \frac{V\_L}{\omega \times L}$$

Voltage across the sense resistor is given by:

$$V_S = \frac{D \times V_O \times R_S}{\omega \times L} = \frac{V_{CA} \times V_O \times R_S}{V_{RAMP} \times \omega \times L}$$

The current loop transfer function is given by the following expression:

$$\frac{V_S}{V_{CA}} = \frac{V_O \times R_S}{V_{RAMP} \times \omega \times L} = \frac{V_O \times R_S}{V_{RAMP} \times 2 \times \pi \times f_S \times L}$$

In this case, the open loop gain of current loop (GPWM_BOOST)is:

$$G_{PWM\_BOOST} = \frac{V_O \times R_S}{V_{RAMP} \times 2 \times \pi \times f_S \times L}$$

Figure 7 presents the key bode plots of the current control loop. The bottom curve is the gain of the PWM-boost section as a function of frequency. The LR pole produces a curve with a slope of -20 dB/dec. Fairchild recommends a crossover frequency defined as 1/10 of the switching frequency, fs. To ensure stability of the converter and fast transient response, the gain plot of close loop system should intersect the frequency axis at the crossover frequency (**fc_cl**) with a slope of -20 dB/dec. A type two compensation network is selected. Assume placement of the zero at **fcl_z=0.2*fcl** and the placement of the pole at **fcl_p=10*fcl**.

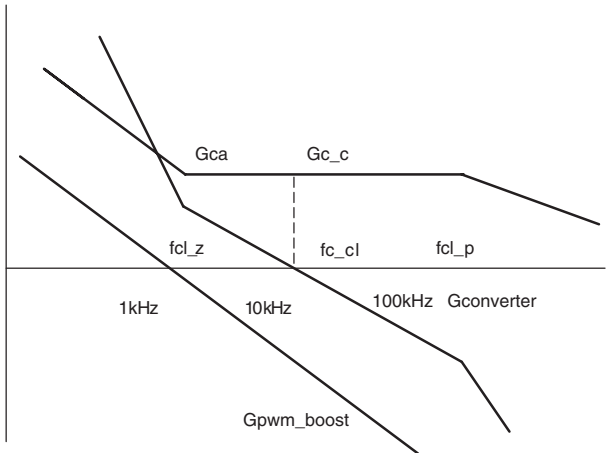

Figure 7. Current Control Loop Bode Plots

For the conditions listed above, an open loop system will have the following gain at crossover frequency.

$$G_{PWM\_BOOST} = \frac{V_O \times R_S}{V_{RAMP} \times 2 \times \pi \times f_{C\_CL} \times L} \qquad (17)$$

The peak-to-peak value of V_{RAMP} is the difference between the peak voltage and the peak valley values. These parameters are listed in the FAN4810 datasheet.

In Log scale $G_{PWM\_BOOST\_LG} = 20 \times \log (G_{PWM\_BOOST})$ (18)

Gain of the current error amplifier at crossover frequency is found from the following expression.

$$Gc\_c = 10^{\frac{|Gpwm\_boost\_lg|}{20}} \qquad (19)$$

This gain ensures that the closed loop Gain plot will intersect the frequency axe on the Bode plots at unity gain.
The current error amplifier is the transconductance amplifier, with the transconductance value of g_ca. Refer to the FAN4810 Datasheet. The value of R12 can be determined from following operation:

$$R12 = \frac{Gc\_c}{g\_ca} \quad (20) \qquad C6 = \frac{1}{2 \times \pi \times fcl\_z \times R12} \quad (21)$$

$$C7 = \frac{1}{2 \times \pi \times fcl\_p \times R12} \quad (22)$$

The values of C6 and C7 can be found based on the zero and pole expressions for a type-two compensation network at frequencies **fcl_z** and **fcl_p**.

Selection Parameters of Voltage Error Amplifier Compensation Network

This section discusses the selection of the voltage divider and compensation of the voltage error amplifier.

Selection of Resistor Divider

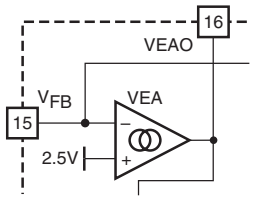

Figure 8. Resistor Divider

The non-inverting input of the error amplifier connects to a 2.5V reference voltage as shown in Figure 8. Output of the voltage divider should set at this voltage level. We are recommending R8=2.37k, in this case a second resistor R8 can be found from following formula.

$$I_{RD2} = \frac{V_{REF}}{R8} \qquad R7 = \frac{V_{BUS} - V_{REF}}{I_{RD2}}$$

Voltage Loop Compensation

Figure 9 shows a simplified block diagram of the voltage loop control. This approach is based on the notion that the voltage control loop can be characterized by the voltage controlled current source feeding output capacitor. We assume that the current loop generates full sine current waveforms that feed capacitor C5 and a resistive load. The voltage error amplifier controls the amplitude of this current and the entire voltage loop closed around the current loop. In other words, the voltage controlled current source combined together with the input voltage source, rectifier, boost inductor, and diode generates full sine waveforms with a magnitude proportional to the output of the voltage error amplifier.

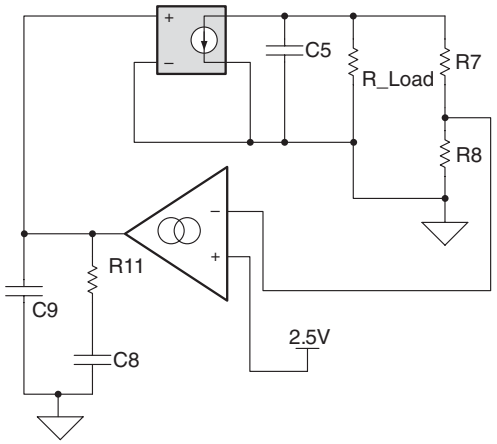

Figure 9. Simple Diagram of Voltage Loop

To prevent increasing the amplitude of third harmonics in the current waveform and to decrease distortion the bandwidth of the voltage control loop should be kept in a range from 10 Hz to 30 Hz. Low bandwidth will minimize the appearance of second harmonics in the input of the current loop and limited THD.

The main reason for using a low-bandwidth voltage control loop is due to the phase difference between the waveforms of the input voltage and ripple voltage on the output of PFC, as shown in Figure 17. The reactive nature of the PFC load determines the phase difference. If not attenuated, the ripple voltage appears on the input and output of the gain modulator and the current waveforms can be distorted. Roll-off capacitor C9 is usually used for second harmonic attenuation. However, too low of a bandwidth of the voltage loop can create transient response problems, so some second harmonic ripple is acceptable. This approach helps to determine a compromise between THD and transient response requirements.

Assuming crossover frequency **fc_vl= 30** Hz for the voltage loop and location of a zero at **fvl_z=3** Hz, we will place a voltage loop pole at the crossover frequency.

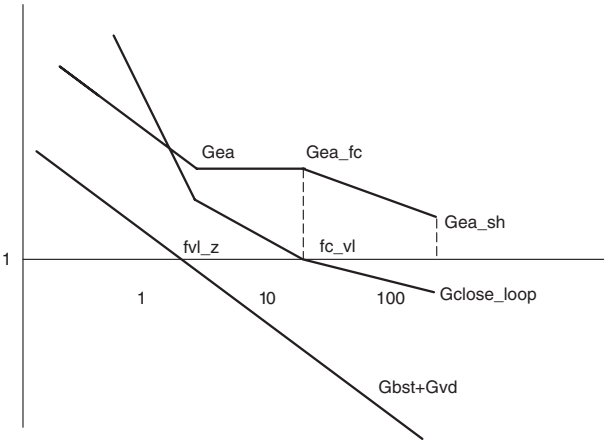

Figure 10. Voltage Loop Bode Plots

Let's find the second harmonic voltage ripple (V_{R_SH}) across bulk capacitor C5.

$$I_{IN\_AV} = \frac{P_{IN}}{V_O} \quad (25) \qquad Z_{O\_SH} = \frac{1}{2 \times \pi \times 2 \times f\_ln \times C5} \quad (26)$$

$$V_{R\_SH} = I_{IN\_AV} \times Z_{O\_SH} \quad (27) \qquad dV_{EA} = V_{EA\_OVH} - V_{EA\_OVL} \quad (28)$$

Where **f_ln** is the line frequency, $\mathbf{Z_{O\_SH}}$ is the impedance of the bulk capacitor at the second harmonic, $\mathbf{V_{R\_SH}}$ is the second harmonic ripple voltage, $\mathbf{dV_{EA}}$ is the output voltage range of the voltage error amplifier, $\mathbf{V_{EA\_OVH}}$ and $\mathbf{V_{EA\_OVL}}$ are the voltage error amplifier's maximum and minimum output voltages respectively.

According to the block diagram in Figure 9, the combined gain of the voltage error amplifier and the resistor divider can be shown as:

$$G_{VD\_EA} = \frac{dV_{EA} \times THD}{V_{R\_SH}} \quad (29)$$

Where **THD** is the total harmonics balance and $\mathbf{dV_{EA}}$ is the output range of the voltage amplifier.

$$G_{VD} = \frac{R8}{R7 + R8} \quad (30)$$

$\mathbf{G_{VD}}$ is the voltage divider gain.

The following equation shows the gain of the voltage error amplifier at the second harmonic.

$$G_{EA\_SH} = \frac{Gvd\_ea}{Gvd} \qquad Z_{EA\_SH} = \frac{G_{EA\_SH}}{g\_va} \quad (31)$$

$\mathbf{G_{EA\_SH}}$ and $\mathbf{Z_{EA\_SH}}$ are error amplifier gain and impedance at second harmonic frequency. **g_va** is voltage error amplifier transconductance. To ensure sufficient roll-off of voltage gain at second harmonic frequency C9 is found from the following expression.

$$C9 = \frac{1}{2 \times \pi \times 2 \times f\_ln \times Z_{EA\_SH}} \quad (32)$$

To find the values of R11 and C8, use the same approach described above in a current loop. The following formula defines gain of the boost section at crossover frequency (G_{BT_FCS}).

$$G_{BST\_FC} = \frac{I_{IN\_AV} \times \frac{1}{2 \times \pi \times fc\_vl \times C5}}{dV_{EA}} \quad (33)$$

A log equivalent of G_{BT_FCS} is:

$$G_{BST\_FC\_LOG} = 20*\log(G_{BST\_FC}) \quad (34)$$

The gain of the voltage divider in log form is shown in equation 35.

$$G_{VD\_LOG} = 20*\log(G_{VD}) \quad (35)$$

The gain of the error amplifier in log form is determined by the following expression:

$$G_{EA\_FC\_LOG} = -(G_{BST\_FC\_LOG} + G_{VD\_LOG}) \quad (36)$$

The gain of the error amplifier at cross-over frequency is:

$$G_{EA\_FC} = 10^{\frac{Gea\_fc\_log}{20}} \quad (37)$$

$$R11 = \frac{0.9 \times G_{EA\_FC}}{g\_ea} \quad (38) \qquad C8 = \frac{1}{2 \times \pi \times fvl\_z \times R11} \quad (39)$$

This concludes the calculation and selection of power and control components for PFC applications based on the FAN4810 IC.

Step-by-step Instructions for Selecting External Components for a PFC Circuit

A PFC design tool is also available on Fairchild's web site. See www.fairchildsemi.com/xxxx for details.

Example Design of a FAN4810 Controller with the Following Specifications

Po= 500W	Output power
V_{MIN} = 80 VAC	Minimum voltage RMS
V_{MAX} = 264 VAC	Maximum voltage RMS
η = 0.93	Efficiency
Vo = 400 VDC	Output (bus) voltage nominal value
V_{O_MIN}= 300 VDC	Output (bus) voltage minimal value
f_S = 100 kHz	Switching frequency
T_{HDL} = 20 ms	Hold-up time
THD = 5%	Total Harmonics Distortion
$dI_{\_RIPPLE}$ = 20%	Ripple current
f_ln = 60 Hz	Line frequency

FAN4810 specifications

t_D = 500 ns	Oscillator dead time
V_{RAMP} = 2.5V	Oscillator Ramp Valley to Peak voltage
R_{MO} = 3.6k	Gain modulator output resistor
$V_{GM\_OUT\_MAX}$ = 0.75V	Gain modulator output voltage
G_{max} = 2	Gain Modulator maximum gain
$V_{GM\_IN\_MAX}$ = 1.1 V	Gain Modulator input voltage that produces maximum gain
V_{REF_EA} = 2.5 V	Voltage Error Amplifier reference voltage
V_{EA_OVH} = 6.7V	Voltage Error Amplifier maximum output voltage
V_{EA_OVL} = 0.1V	Voltage Error Amplifier minimum output voltage
g_ea = 65 uS	Voltage Error Amplifier transconductance
g_ca = 100 uS	Current Error Amplifier transconductance
R_{GND} = 3.6 k	Current Error Amplifier termination resistor
V_{REF} = 7.5V	Reference voltage

Selecting the Power Components

Value of boost inductor L1 calculated based on formulas (1), (2), (3), (4), (5).

P_{IN} = 537. 6 W $I\_L_{MAX\_PK}$ = 10.45 A $I_{\_LINE\_PK}$ = 9.5A D = 0.717 dI = 1.9A

Calculated value of L1 is 426 µH. Value of inductor L1 = 420 µH is selected.

The value of bulk capacitor C5 is selected based on formula (6). The calculated value of C5 = 2.857 µF. A standard value of C5 = 330 µF/450V is selected for the bulk capacitor.

The value of the current sense resistor selected is based on formula (15). The calculated value is 0.072 Ω. A standard value R5 = 0.050 Ω is selected for the current sense resistor. Parameters of current sense filter selected based on (16) R17 = 100 Ω, C19 = 0.047µF. Corner frequency of the filter, calculated based on (16) is 33.8 kHz, that is inside the specified range between 16.6 kHz and 100 kHz.

The boost diode D1 and switch Q1 are chosen for a voltage rating of 500V or greater to withstand safely the 400V boost potential. Current $I\_L_{MAX\_PK}$ = 10.45 A is also the peak current for the boost diode D1 and switch Q1.

It is very difficult to recommend particular semiconductors for specific applications, because these decisions are usually made based on the unpredictable factors such as customer's inventory, airflow, and size of the heatsink. Refer to Table 1 for recommended MOSFETs, IGBTs and diodes.

Selecting Control Components

For setting the oscillator frequency value, R6 is calculated based on formula (7) and the assumption C18 = 470 pF, yields R6 = 41720 Ω. Let's select a standard value R6 = 41.2 k.

Selecting Parameters of Gain Modulator Input Circuit

R1 is based on formula (8). To minimize the voltage rating of each resistor, two 453K resistors in series are selected for R1. The calculated value of R8 = 1.06 M.

Let's use the same resistors that were selected above for R2, R2 = 906 k and R3=100 k. R4 can be found using formulas (9), (10), and (11). Vav = 72.1V, Ird1 = 70.5 µA, R4 = 15.67 k. R4 = 15.8 k selected.

The value of capacitors C3, C2 are calculated based on formulas (12), (13), and (14). Using these formulas C3 = 1.035E-7 F and C2 = 5.11E-7 F. Standard values C3 = 0.1 µF and C2 = 0.47 µF are selected.

Selection Parameters of Current Error Amplifier Compensation Network

Let's set fc_cl = 10.0 kHz, fcl_z = 2.0 kHz, fc_p = 100 kHz.

The value of R12 can be calculated based on (17) – (20). G_{PWM_BOOST} = 0.303, $G_{PWM\_BOOST\_LG}$ = -10.4, and Gc_c = 3.3. R12 is determined to be 32.986 k. We will use a standard value of R12 = 33.2 k. The values of C6 and C7 are determined from (21) and (20). From these equations C6 is found to be 2.392E-9 F and C7 is found to be 4.79E-11 F. We will use 2.2 nF and 47 pF for C6 and C7, respectively

Selection Parameters of Voltage Error Amplifier Compensation Network

Let's assume R7 = 2.37 k, R8 is determined by (23, 24). From equation 23, I_{RD2} is found to be 1.055E-3 A, R7 is determined to be 3.768E+5 Ω. To reduce the voltage across each resistor, R7 is composed of three resistors of 127 k each.

To determine the value of resistor C9, a number of intermediate variables should be calculated. Using expressions (25) – (32), the following can be calculated:

G_{VD_EA} = 0.045, G_{EA_SH} = 7.33, Z_{EA_SH} = 11.29E+4 Ω and C9 = 1.17E-8 F is selected. A standard value of C9 = 0.01 µF is selected.

To determine the values of R11 and C8 a number of intermediate variables should be calculated. Using expressions (33) – (39), the following is calculated: G_{BST_FC} = 4.41, $G_{BST\_FC\_LOG}$ = 12.9, G_{VD_LOG} = -44.2, $G_{EA\_FC\_LOG}$ = 31.13, G_{EA_FC} = 36.7. R11 = 5.08E+5 and C8 = 1.117E-7 F. Standard values of R11 = 510 k and C8 = 0.1µF are selected.

PFC Controller Application Tips

FAN4810 start-up takes place when C15 is charged to 13V through R13 and R14. PFC switching action now boosts the voltage on C5 to 400V via boost inductor L1. Through auxiliary winding of boost inductor L1, the circuit receives a regulated 15V from a full wave rectifier that consists of D3, D4, C12, and C16. For proper circuit operation, high frequency bypass capacitors are required on Vcc and V_{REF}. Low ESR ceramic or film capacitors are highly recommended. Orderly PFC operation at start-up is guaranteed when D2 quick charges C5 to the peak AC line voltage before the boost switch Q1 turned on. This sequence ensures the boost inductor current is zero before the PFC action begins. The regulated voltage on C5 must always be greater than the peak value of the maxi-mum line voltage delivered to the supply.

The soft start circuit is comprised of components Q4, R16 and C20. The error amplifier's output voltage, V_{EAO}, is forced to follow the charging voltage of C20 by Q4. As C20 charges toward V_{REF}, Q4 is biased off. The PFC duty cycle is proportional to V_{EAO}, where zero V_{EAO} gives zero duty cycle.

Circuit Performance

Figure 11 is a complete schematic of this application circuit. Figures 12 and 13 show the efficiency and THD performance. Figure 14 shows input current waveforms. Figures 15-17 show start-up waveforms.

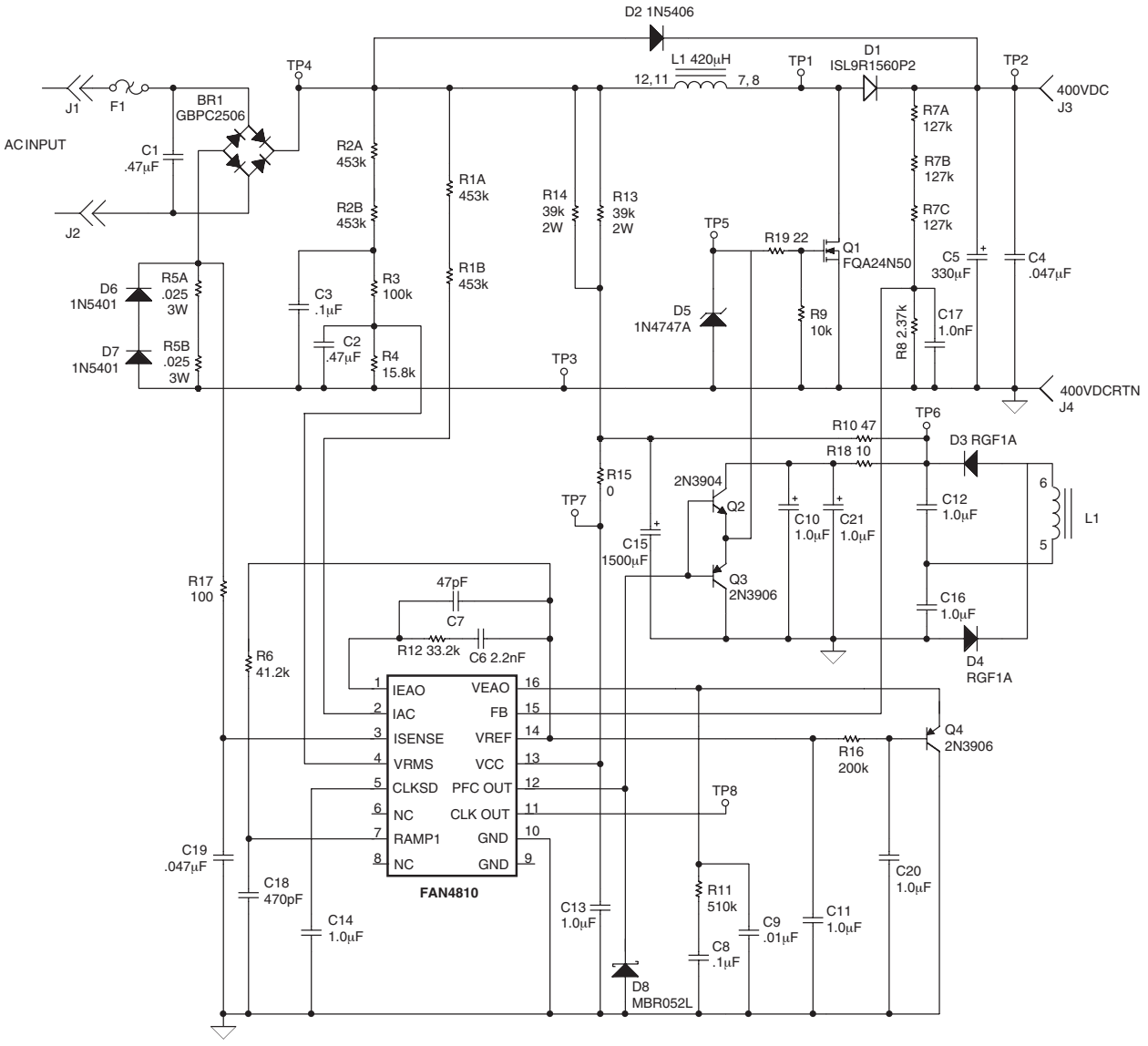

Figure 11. Schematic of 500W Power-Factor-Corrected Boost Converter

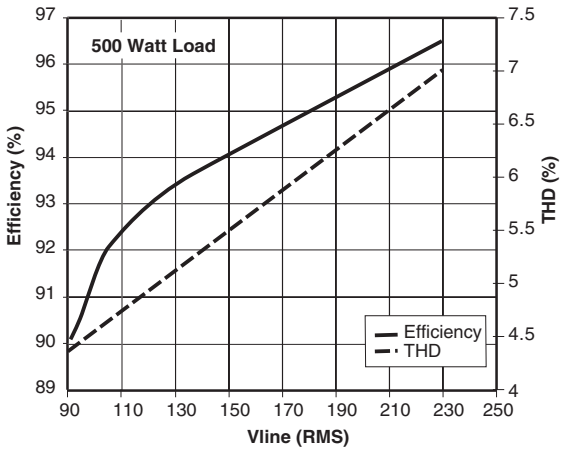

Figure 12. Efficiency and THD Performance vs. Input Line Voltage

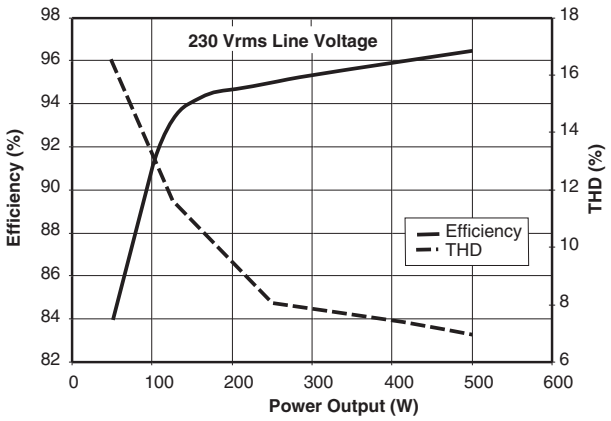

Figure 13. Efficiency and THD Performance vs. Output Power

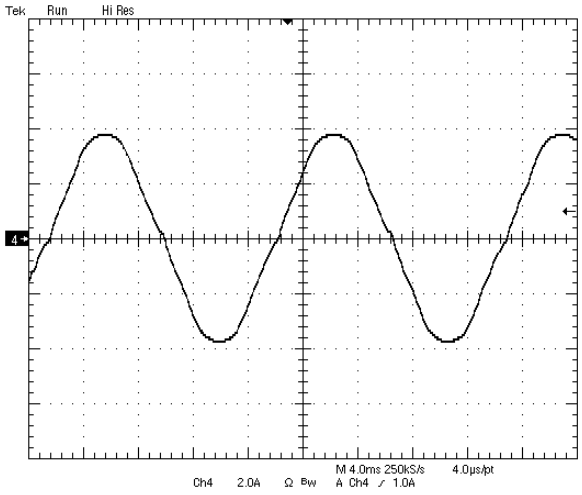

Figure 14. Input Current Waveform

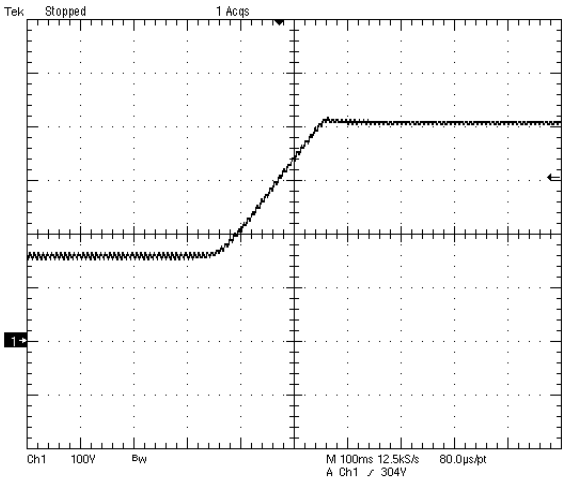

Figure 15. Turn-ON, Vo=405.3V, Io=0.5A

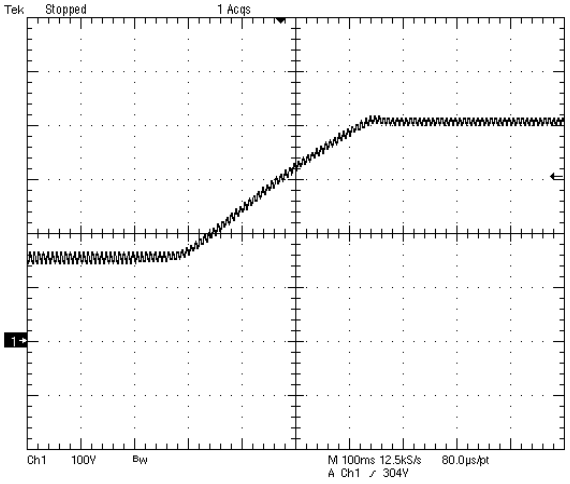

Figure 16. Turn-ON, Vo=405.3V, Po=500W

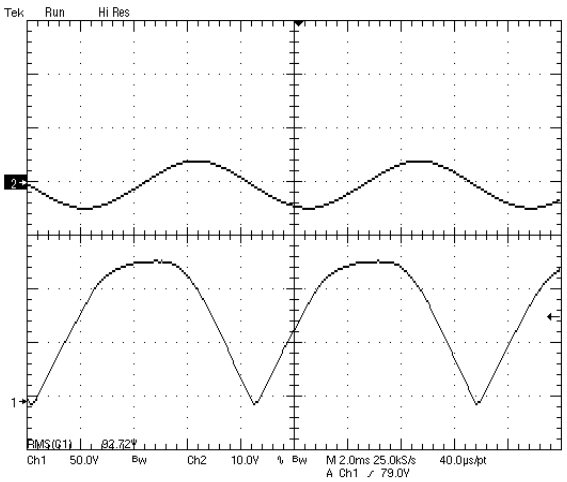

Figure 17. Input Voltage and Output Voltage Ripple Waveform

Table 1: Recommended Components

MOSFETs

Power Level	Voltage rating	P/Ns
75_100W	500,600V	FQP6N50,FQP9N50, FQA13N50, FQA16N50,FDH15N50
100_400W	500,600V	FQA16N50, FQA24N50, FQA19N60, FQA28N50
>400W	500,600V	FDH44N50 ,FQL40N50, FQA28N50 , FDH27N50, FQA19N60,FDH15N50 ,

IGBTs

Power Level	P/Ns for frequency < 75 kHz
75_100W	FGH20N6S2D,HGTG7N60A4D
100_400W	FGH30N6S2D,HGTG12N60A4D
>400W	FGH40N6S2D, HGTG20N60A4D, FGH50N6S2D, HGTG30N60A4D, FGK60N6S2D

Boost Diodes

Power Level	P/Ns
75_100W	ISL9R460P32 ISL9R860P2,
100_400W	ISL9R860P2,ISL9R1560P2,
>400W	ISL9R1560P2,ISL9R3060P2

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