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Guidelines for Pb-Free Soldering of Fairchild Components Based on JEDEC® J-STD 20D / IEC EN 61760-1:2006

Introduction

The basic concepts behind the Pb-free SMT reflow process are the same as the old industry standard Sn63Pb37 solder used for decades in the electronics industry. The proper characterization of the equipment, with consideration given to the board component loading, as well as the selection of the appropriate materials and printing process, result in a reliable, high-yield, low-rework assembly run. Similarly, proper characterization of the Pb-free wave-solder process results in consistent wetting of the terminals and through-holes with no damage to surface mounted components on the same board. This application note presents Fairchild's recommendation for a starting point for SMT and wave solder profiles; however, it is critical to recognize that a soldering profile that works for one board and material set likely differs from other production runs if the material or board design is different.

Solder Profile Basics

The placement of the thermocouples is critical for an accurate solder profile. Industry experts, such as Jabil Circuit1, recommend a review of the leaded components on the board to establish the hot spots, such as the package body, and cold spots, such as the terminal (where it sits on the land pattern). For array packages, such as WLCSP and BGA, it is a little more challenging, but very important; especially with large array packages. The top of the body is selected and, for the terminals, the recommendation is to drill a hole in the middle of the center ball and one of the perimeter balls to insert the thermocouples. Generally, selection of the largest components is desired for the thermocouples as they are slowest to reflow due to their thermal mass. The smallest packages and edges of the printed circuit board (PCB) should also be considered, as these heat quickly and could be overstressed if exposed to extended heating. Fairchild strongly suggests that customers review recommendations in JEDEC® JEP140 for thermocouple use.

Package Peak Temperature

JEDEC® J-STD 020D recommends that the target peak package temperature for Moisture Sensitivity Level (MSL) assessment be selected based on package volume and thickness. J-STD 020D is "…not meant to specify board assembly profiles;"[2] however, to prevent component damage, actual SMT profiles should not exceed the parameters J-STD 020D Table 5-2, reproduced below:

Table 1. J-STD 020D Table 5-2

Thickness (mm)	Volume (mm3)		
	<350	350-2000	>2000
<1.6	260c	260c	260c
1.6-2.5	260c	250c	245c
>2.5	245c	245c	245c

Note:

1. All Fairchild packages are rated for Pb-free solder using JEDEC® J-STD 020D MSL classification specification solder profile and are backward compatible with conventional Sn63Pb37 solder. Packages receiving an MSL rating greater than one may need to be baked before assembly, depending on storage conditions *(see product packaging for recommendations / requirements)*.

The Reflow Process[3]

Refer to Figure 1 for an illustration of a typical Pb-free Surface Mount (SMT) reflow profile.

In the reflow process, each of the process zones is critical for good performance.

The preheat zone's purpose is to evaporate any solvents in the solder paste or in the construction of the board. A ramp rate of three degrees centigrade per second (3°C/s) is the maximum recommendation to avoid splattering, bridging of solder fillets, slump, or solder-ball creation. Careful control of the ramp rate also helps avoid thermal shock stress of the components and the PCB.

In the soak zone, flux components are activated and the reduction of oxides on both terminals and board pads begins. The soak is important where there is a wide mix of component sizes (and mass) as they are all brought up in temperature in preparation for soldering.

The third process area is the reflow zone, in which the solder spheres in the solder begin to melt together, forming the solid mass needed to provide the strength in the bond between the component and the board.

The final step is the cool-down ramp rate. At this point, the board and components are brought back to room temperature at a controlled rate so no solder intermetallics that can weaken the bond form. The cool-down ramp rate affects the grain structure in the solder joint, which affects board-level reliability; in particular, drop test performance, where finer structure results in better results. Faster cool-down ramp rates result in finer grain structures.

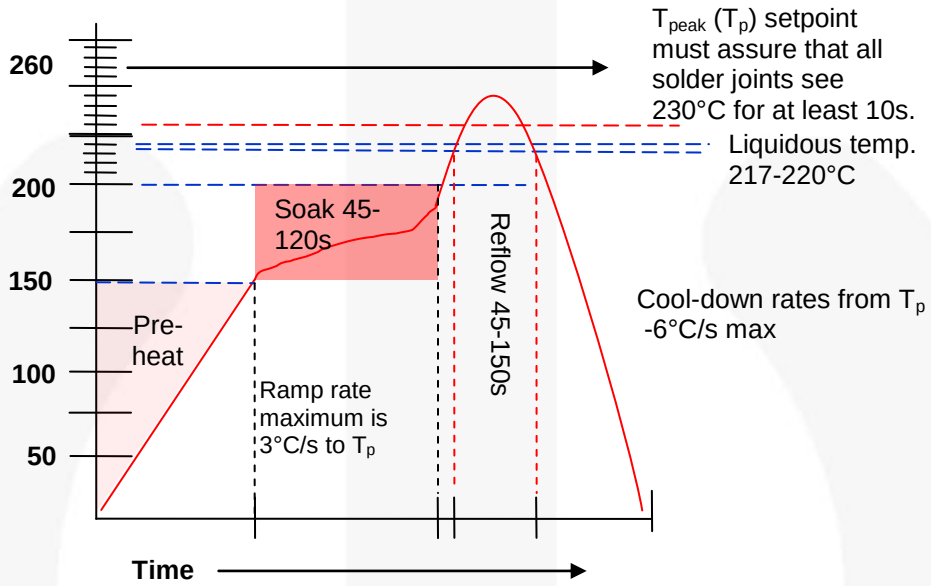

Figure 1. Pb-free Surface Mount (SMT) Reflow Process

Solder Reflow Profile Examples

Examples of Pb-free solder reflow profiles for various Fairchild Semiconductor SMT packages, showing that there is no single universal solder profile that can be used for all packages and boards.

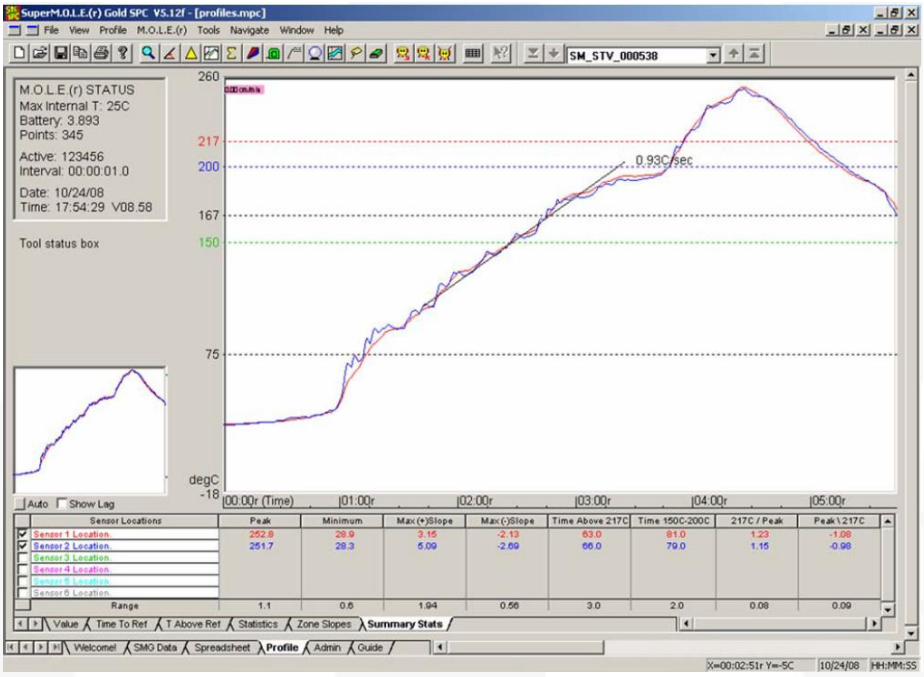

Figure 2. Fairchild-Derived Reflow Profile for WLCSP Using SAC305 Solder Paste

Note:

2. The time above 217°C is 63-66 seconds, depending on which thermocouple is viewed.

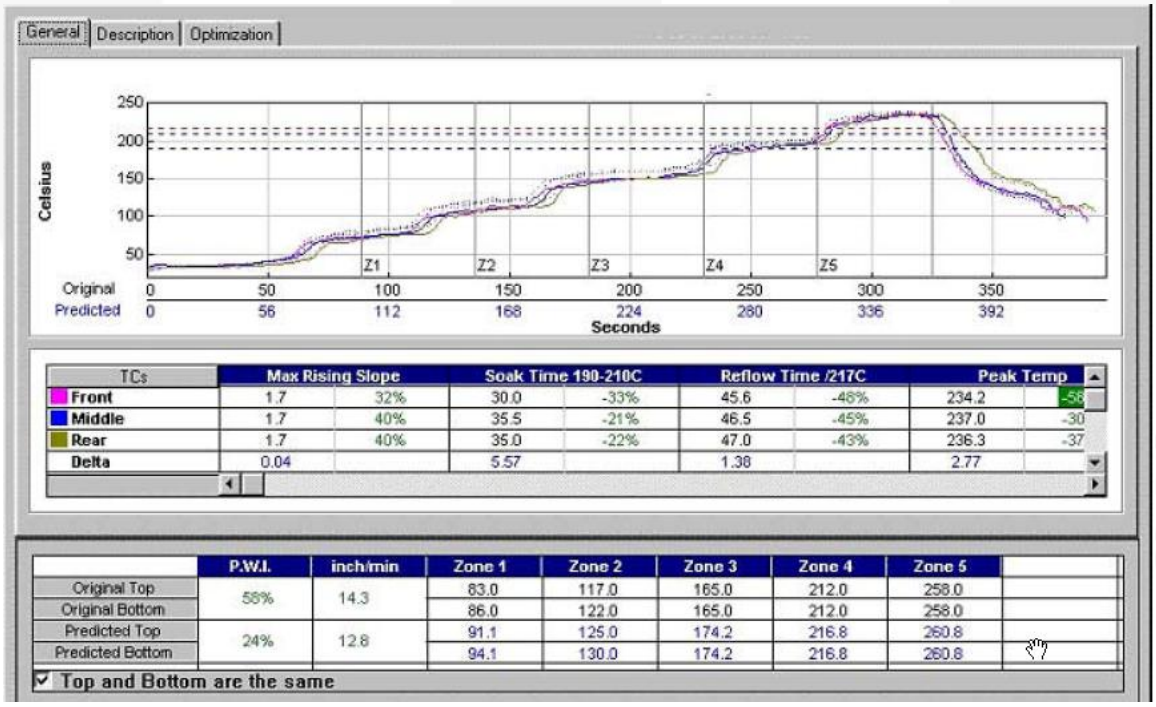

Figure 3. Fairchild-Derived Profile for 8x8 Multi-DAP QFN (MLP) Using SAC305 Solder Paste

Note:

3. The time above 217°C for this much-larger package is only 45-47 seconds. The difference is the PCB has a low density array of this package type, so thermal load is lower than the example in Figure 2 above.

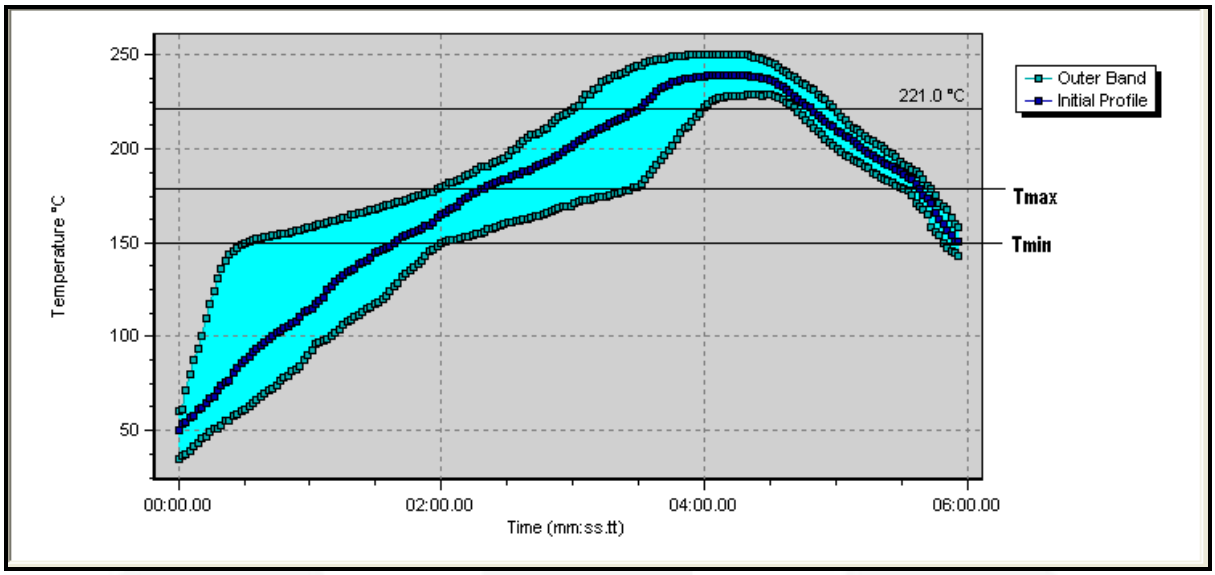

Figure 4. Fairchild-Derived Profile for .35 mm Pitch UDQFN Using SAC305 Solder Paste

Note:

4. The tiny UDQFN was assembled on a high-density board that featured a mix of packages and included a large number of 0603- and 0204-sized passive components as well as a 144ld TQFP package. The reflow time is around 60-70 seconds.

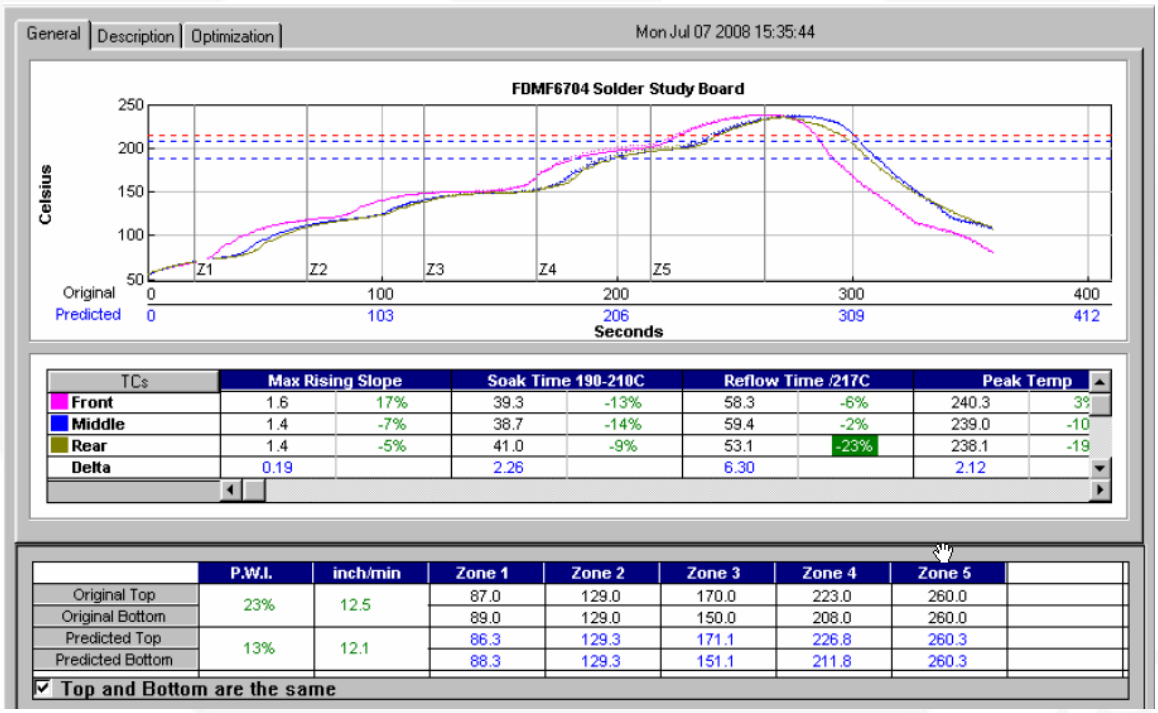

Figure 5. Fairchild-Derived Profile for 6x6 Multi-DAP QFN (MLP) Using SAC 305 Solder Paste.

Note:

5. The difference in this profile compared to the one for the 8 x 8 version of the same package technology in Figure 3. The reflow time in Figure 5 is 53-59 seconds compared to 45-47 seconds for the bigger package in Figure 3.

Solder Profile for Pb-Free Dual-Wave Soldering Process

To achieve good results with lead-free wave solder process, the condition of the solder must be considered, with analysis recommended every 5000 boards. The process should be carefully optimized as lead-free solders are slower to wet compared to traditional SnPb solder. Contact time, conveyor speed, and width are critical parameters for lead-free.

For ramp temperatures, the delta should be no more than 200°C/s with preheat heating rate of between 1 and 4°C/s, with 2°C/s typical. The target of the final preheat stage should be to bring the board to within 125°C of the soldering temperature. The maximum time across both waves should be limited to 10 seconds. The cool-down ramp should be 5°C/s maximum. 260°C is the maximum temperature and should not be exceeded.

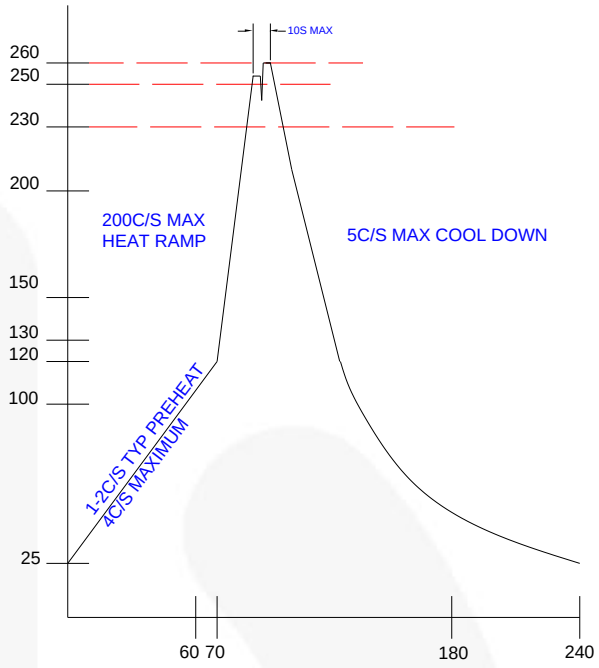

Figure 6. Lead-Free Dual-Wave Process
(refer to EN 61760-1:2006)

References

[1] "Lead-Free Reflow Profile Study" presented at IPC-JEDEC® 4th International Conference on Lead-free Electronic Components and Assemblies. Nabel Ghalib & Guyen Chu, Jabil Circuit, Inc. and Girish S. Wable, State University of New York, Binghamton.

[2] JEDEC® J-STD20D, Note 2, Table 5-2, Classification Reflow Profiles, page 7.

[3] David Scheiner, Kester Solder, "Solder Materials," SMT Magazine, July, 1998.

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