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AN-5078

Board Assembly Guideline for Fairchild High-Voltage Power88 Package

Summary

Power Quad Flat No-Lead (PQFN) packages are widely used package for low-voltage applications. Because of its small configuration and low profile, it offers a space-saving alternative to typical leaded packages. Fairchild has developed a PQFN package, Power88, for high-voltage applications. The new package size has an advantage over the industrial standard high-voltage SMD component, the D2PAK package, because of its size, while still meeting the clearance and creepage distance requirements for high-voltage applications. The Power88 package is paired with the Fairchild SuperFET® II super-junction MOSFET, which gives extremely fast switching and highly efficient devices.

This board assembly application note is created to guide user on maximizing the benefits of the Power88 product.

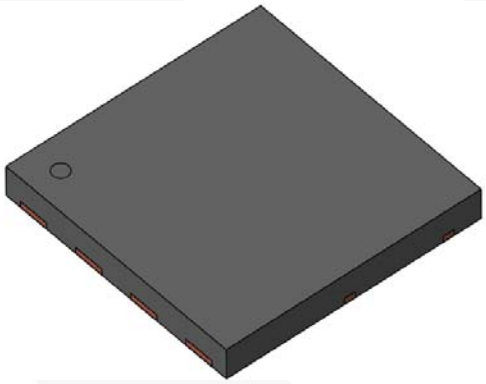

Figure 1. Power88 Package, Top View

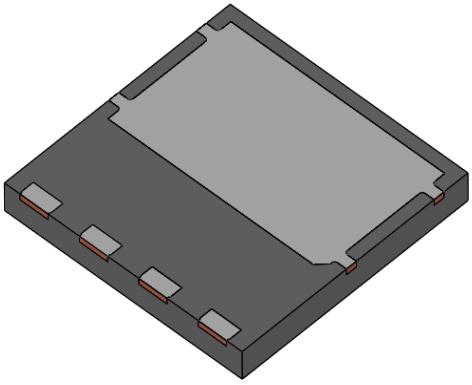

Figure 2. Power88 Package, Bottom View

Board Attributes and Design Guide

Land Pattern Design

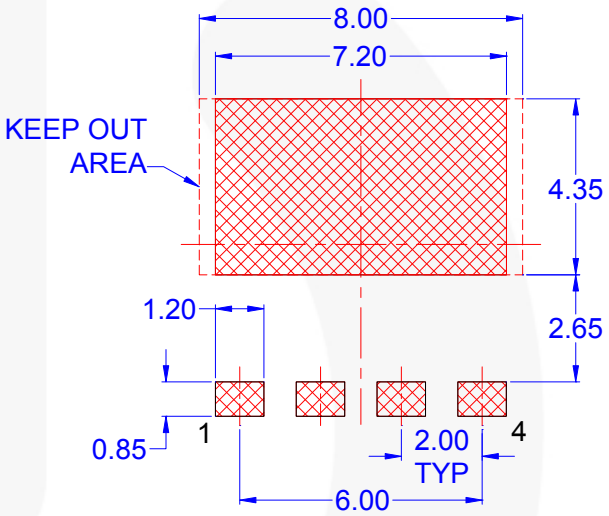

Figure 3. Recommended Land Pattern for Power88 (Dimensions are in millimeters)

The source and gate pads are larger than the package lead to allow toe filleting of the solder. This is also wider than the leads, providing enough allowance for variation in board fabrication and component placement during assembly. This tolerance can typically vary up to 0.10 mm, combined. The land pad for the exposed thermal pads of the package is equal to the size of this exposed pad. This connection between the board and the component allows the strong surface tension of the molten solder to pull the component to align itself with the land pad. With this, even highly offset component placement lets the component self-align with the board pads.

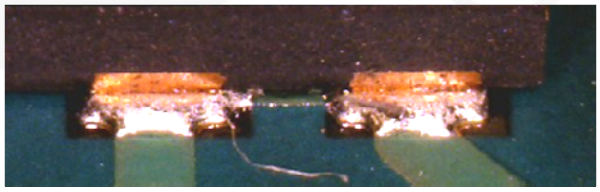

Figure 4. Solder Fillet at Toe of Component Lead

Solder Masking and Trace Routing

The board pads are either Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD), as shown in Figure 5.

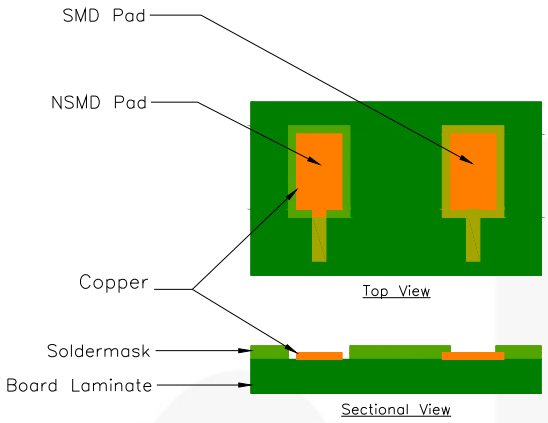

Figure 5. NSMD vs. SMD Land Pad

In NSMD, the copper pad is etched to define the land pattern. The overall pattern registration is dependent on the copper artwork. The SMD pad is defined by a photo-image able solder mask process. Because of the smaller area covered by the NSMD pads, this allows more area for routing traces around the component. This is not like the SMD pads where pads are much larger than the defined pads for soldering. SMD pads allow more metal for dissipating heat during application. The overlap on the copper pad also helps prevent bridging of the paste between the leads and the exposed pad by blocking solder from flowing outside the solderable pads during the reflow process. The solder masks anchors itself on the copper to improve copper adhesion to the board.

In the Power88, it is not recommended to route traces in between the leads and the thermal pad. In high-voltage applications, high potential between the terminals can create arcing between the narrow spaces between metals.

Board Surface Finish

The pad surface finishes commonly used are electroless nickel immersion gold (NiAu), organic solder ability preservative (OSP), and hot-air surface leveling (HASL). A finish becoming popular is immersion silver (Ag). NiAu is preferable in some applications and fine-pitch packages because of its excellent surface solder ability and flatness. OSP is excellent for fine pitch packages and BGA due to its very low cost and excellent flatness. The thickness should depend on the resistance of the underlying copper pad from tarnishing and retention of the solder ability of the surface. HASL is the most readily available surface finish. It has a superior barrel fill and solder ability characteristics. Immersion (Ag) is a lead-free alternative and has an excellent flatness, but special handling may be required.

There is no recommended surface finish for the Power88; however, reliability tests performed on this package used OSP and NiAu surface finishes. Both finishes the package passed the qualification requirements.

Via-in-Pad

Via-in-pad design is recommended to improve thermal dissipation performance of the mounted device. The vias provide thermal conduction path from the component side to the bottom and internal layers of the board. This allows faster heat dissipation from the package. The more vias are on the pad, the better the thermal dissipation. Vias also serve as escape path for volatile components of solder fluxes during reflow; which helps minimize formation of solder voids between the exposed thermal pad of the component and the board pad. Other factors that can affect the thermal performance of the package include:

- Board thickness
- Overall board size
- Number and thickness of the copper layers connected to the vias
- Proximity to other heat-dissipating parts on the board

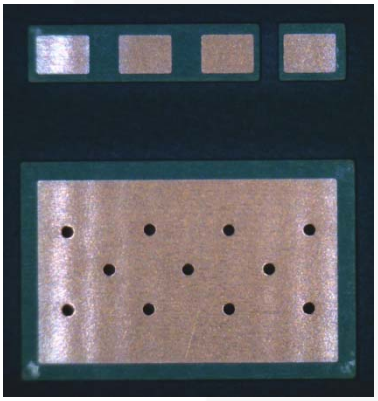

Figure 6. Sample Board Land Pad with Via Holes on Pad

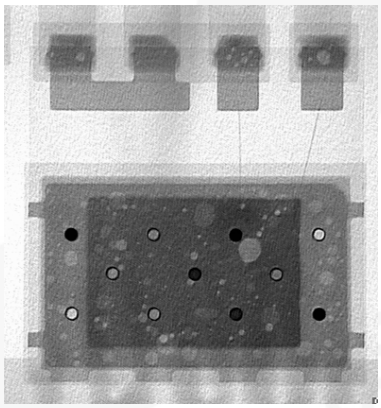

Figure 7. X-RAY of Power88 on Land Pad with Vias

Board Assembly Considerations by Solder Paste Printing and Reflow Process

Solder Paste

Solder pastes normally used in board assembly have particles sizes of either Type 3 or Type 4 and their flux materials are classified as rosin-based, low-activity, and halide-free (ROL0) or the no-clean solder paste (typically a ROL0 or ROM0). Typical metal loading of the paste ranges from 88% to 90% solder alloy in the paste; approximately 50% solder paste by volume. The most common solder alloys for board assembly are the eutectic SnPb solder (63Sn37Pb) and the SAC305 (95.5Sn3.0Ag0.5Cu) for the lead-free assembly.

Fairchild recommends solder pastes with a no-clean flux be used in the board assembly of the PQFN packages. Due to the low standoff heights of the solder joints; it is difficult to clean the trapped flux residues under the package.

Stencil Aperture and Thickness

The recommended stencil aperture designs for the PQFN packages are shown in Figure 8.

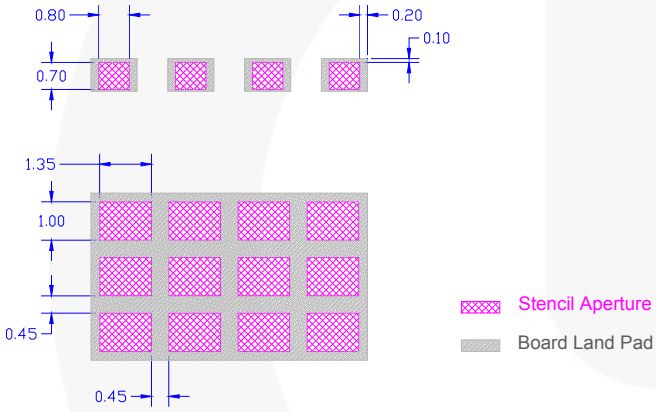

Figure 8. Stencil Aperture Design for Solder Paste Printing on Board for Power88 (in mm)

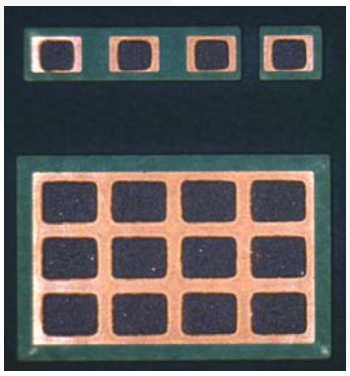

Figure 9. Sample Solder Paste Test Print on SMD Land Pads

The aperture for leads and exposed die pad are relatively smaller than the board pads. The apertures for the exposed pad are about 40 to 70% of the land pad size. The apertures on the leads are smaller than the pads to balance the thickness of the resulting solder joint from the exposed die pad. Recommended stencil thickness is 0.125 mm.

The relatively small solder paste print coverage for the exposed pad of the PQFN package is based on a study conducted on several pastes from different vendors and different solder paste print coverage for the exposed pad. It was found that each paste reacts differently to reflow. One paste outgases much more than the other pastes. Large print coverage for this kind of solder paste on the board pad can create several defects in the assembly. Among the defects observed are shown below.

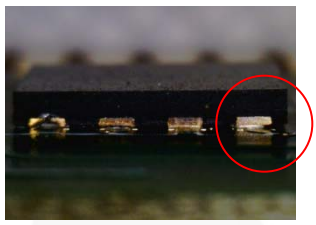

Figure 10. Tilted Component, Insufficient Wetting on Pin 4

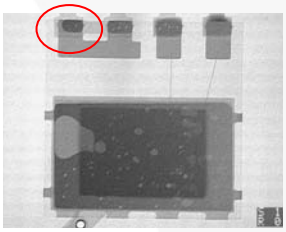

Figure 11. X-RAY of Tilted Component, Insufficient Solder on Pin 4

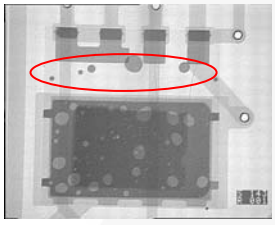

Figure 12. X-Ray of Solder Balls Under Package

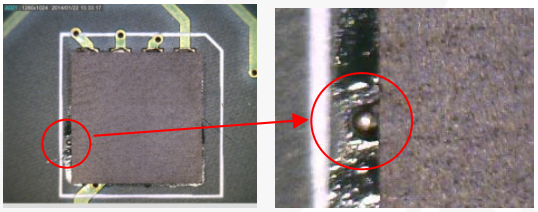

Figure 13. Solder Beading at Package Periphery

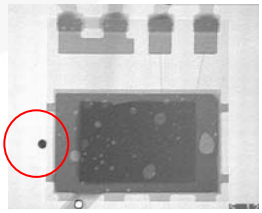

Figure 14. X-RAY of Solder Bead

Investigation into the cause of these defects revealed that the out gassing of the flux during reflow pushes the pastes or the molten solder outwards from the pad. As a result, the solder that goes outside the pad creates solder beads in the periphery or under the package. At times, this may add or pull out solder from the adjacent leads, creating an imbalance in the solder volume in between leads leading to a tilted package or solder bridging.

For other pastes evaluated, a print coverage of up to 85% does not show such defects. It is possible to use larger print coverage; it may be advisable to characterize the paste properly and the stencil design.

In the above recommended aperture, the aspect and area ratios were calculated and found to be above the typical minimum acceptable value for a laser-cut stencil. The formulae for area and aspect ratios are:

$$\text{Aspect Ratio} = \frac{\text{Width of Aperture}}{\text{Thickness of Stencil Foil}} \qquad \text{Area Ratio} = \frac{\text{Area of Pad}}{\text{Area of Aperture Wall}}$$

Generally, the aspect ratio should be >1.5 and the area ratio >0.66 for a laser-cut stencil. However, depending on the package type, lead size, and pitch; the aspect and area ratio may change in certain cases.

Tapering or trapezoidal opening of stencil holes is recommended because this improves the solder paste released during paste printing. Electro-polishing a laser cut stencil is also recommended for better solder paste release. Use of electroformed stencil is recommended because of its excellent release performance and its long useful life, but it may not be necessary for this type of package. The drawback for the electroformed stencil is its cost, which is significantly more expensive than the laser-cut stencil.

Component Placement

Depending on the placement accuracy of the pick-and-place machine, the PQFN packages can tolerate up to a certain amount of placement offset to have an acceptable solder joint. Simulations revealed that the PQFN package can allow placement offset up to 50% of its land pad width. This is about 0.50 mm offset. In this situation, the package can re-align itself with the board land pad during solder reflow.

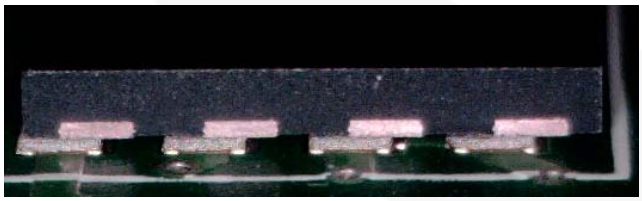

Figure 15. Package Placement Offset, Before Reflow Along the Length of the Leads

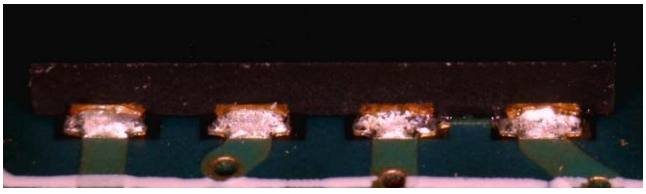

Figure 16. Package Placement Offset, After Reflow

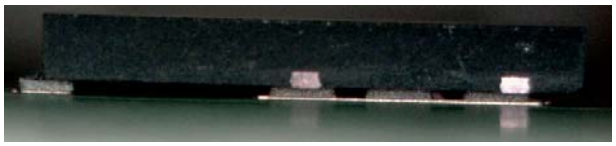

Figure 17. Package Placement Offset, After Reflow Along the Length of the Leads

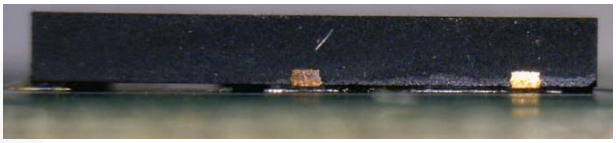

Figure 18. Package Placement Offset, After Reflow

Placement height or pressure should be taken into consideration during component placement on the board. Compressing the printed paste between the component and the board results in paste being spread out on the land pad area. This is especially true on the exposed area where large paste volume is deposited. The compressed paste narrows down the paths for solder paste to outgas during reflow, which can lead to defects like beading. It is recommended that the placement height be controlled. Some component mounters have the ability to control the height or the amount of bonding force during component placement. This should be characterized. The height should be sufficient to allow enough adhesion of the component to the paste, not to allow it to fall off during transport to the reflow oven.

Reflow Process and Component Moisture Sensitivity

The temperature profile to use during reflow of the PQFN package should be based on the recommended temperature profile of the solder paste vendor. Do not to expose the package to temperatures higher than 260°C. This package is tested and qualified to perform reliably up to three reflow passes at the maximum reflow peak temperature of 260°C.

Thermocouple locations should be taken into consideration when creating the reflow profile for the board. Due to variation in the component sizes, number of components on each area of the board, and board design; there is variation in the thermal masses on the board. This results in a wide temperature gradient across the board. It is important that thermocouples be placed on areas where temperature-sensitive components are placed to monitor the temperature to which the components are exposed and on areas where high thermal masses exists. This ensures the components on these areas are exposed to the right reflow temperatures.

Fairchild's application note AN-7528 provides guidelines on the different reflow methodologies for surface-mount devices. Critical conditions that affect the components on the board and the appropriate temperature profile for each reflow technology are presented.

The PQFN package is tested to meet moisture sensitivity level 1 at 260°C peak reflow temperature per IPC/JEDEC J-STD-020. Therefore, baking this component prior to assembly is not necessary.

Board Assembly Considerations by Wave Soldering

Wave Soldering Process

A typical wave-soldering process is illustrated in Figure 19. Adhesive is applied on the board and the package is mounted. The adhesive is then cured by subjecting the assembly to a high temperature environment (according to the adhesive specification). The board is flipped so that the mounted package is at the bottom side of the board as it goes through wave soldering. Flux is applied to the bottom side of the board where the package is mounted and wave soldered according to the set profile.

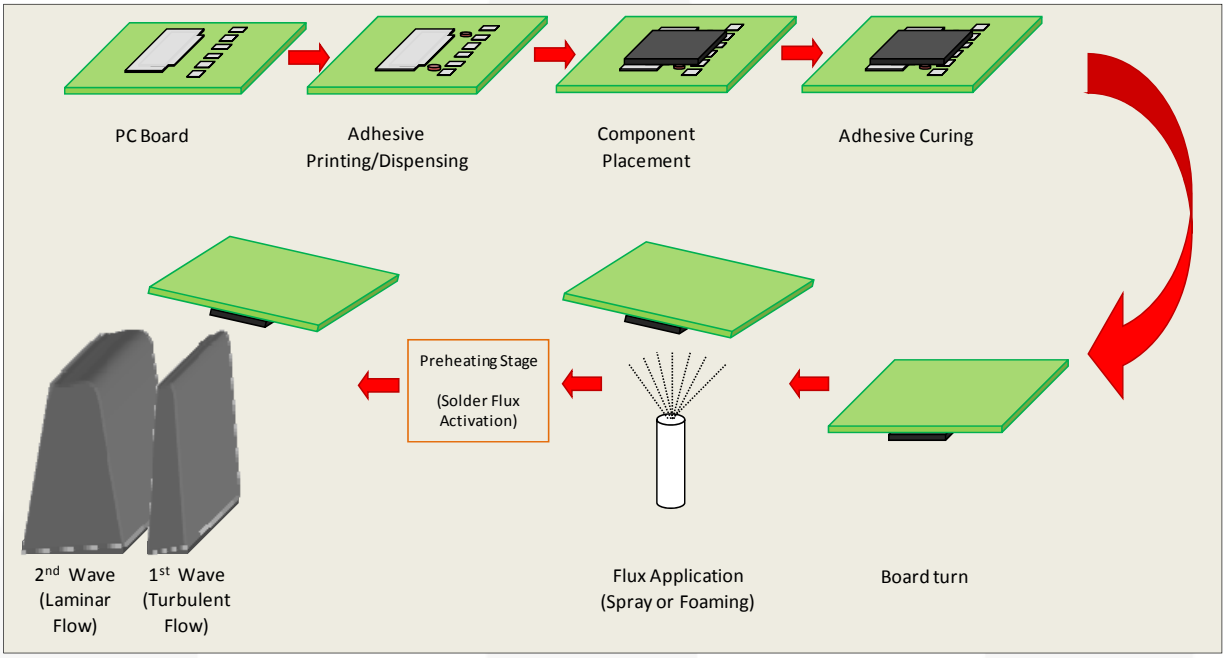

Figure 19. Wave Soldering Process Flow

To achieve a good wave-soldering process for PQFN packages, the following factors must be identified and studied carefully:

- PCB Mask Configuration
- PCB Solderable Surface Finish
- PCB Land Pad Design
- Adhesive and Adhesive Layout
- Solder Flux
- Wave Solder Profile
- Board Mask Configuration

The pad configuration of the board can be solder mask defined (SMD) or non-solder mask defined (NSMD). For wave soldering, any PCB mask configuration can be used. SMD pad, however, have an added advantage; the mask on top of the land can serve as an added spacer between the board pad and component, allowing more room for flux and solder to flow during processing.

Board Surface Finish

Hot Air Surface Leveling (HASL) and Organic Solder ability Preservatives (OSP) are common board surface finishes used in the industry today. These types are compatible with wave soldering the Power88 using the recommended land pad design shown in Figure 20.

In various land pattern options evaluated, the wetting mechanism using OSP surface finish differs from HASL. Solder filling is more readily observed in HASL than in OSP. This may be explained by the coalescence of molten solder and the molten HASL metallization. However, it is not uncommon for HASL to have inconsistent solder coating thickness that affects the leveling in board mounting PQFNs. The OSP may have poorer wetting than HASL, but is known to consistently produce thin coatings. To achieve good wetting for OSP metal, a good flux is necessary and it should be applied to where the solder needs to flow. For packages with large exposed thermal pads, like the Power88, land pads that extend outside the package allow solder to spread throughout the bottom surface of the package. The recommended land pad design proved compatible for both types of surface finishes using a no-clean flux in testing.

Board Land Pad Design

The recommended land pad design for wave soldering the Power88 is show in Figure 20.

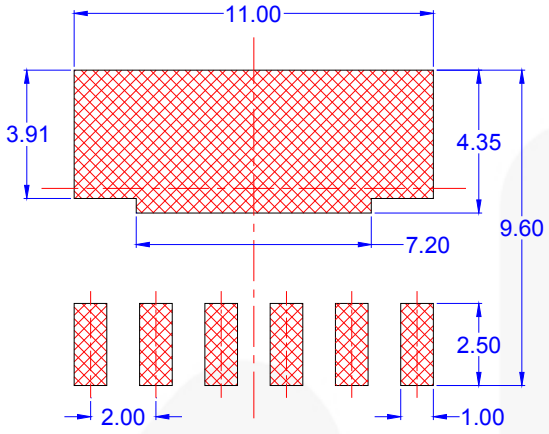

Figure 20. Land Pattern Design for Power88 Wave Soldering (in mm)

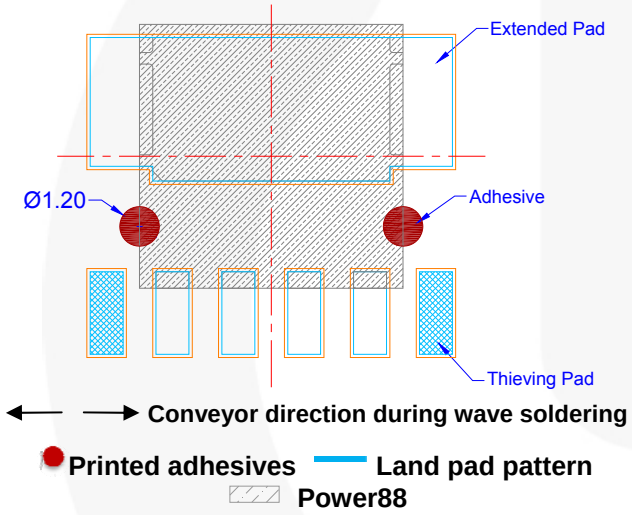

Figure 21. Overlaid Power88 on the Board Land Pad and Printed Adhesive

In wave soldering PQFNs, the land pad dimensions should be larger than the nominal package footprint dimensions. This allows a path for the molten solder to flow through the land pad at the bottom of the package. The recommended design for the Power88 has significantly larger land pad for the drain, which extends at the sides because it has a larger surface to be soldered at the bottom of the package.

Thieving pads are added at the two corner pins for the Power88 to wick excess solder from the active pads to prevent solder bridging.

Component orientation with respect to the direction of the equipment conveyor is critical to get a good soldering result. As illustrated in Figure 21, the lead land pads layout is aligned with the movement of the conveyor. This component orientation with respect to conveyor movement prevents solder bridging, solder skipping, or shadowing.

Adhesive

In wave soldering PQFNs, the adhesive must be chosen to ensure it holds the component through the entire wave soldering process flow. It must be tacky enough after print that the component doesn't move or fall off during transport from component placement to cure. It must have good adhesion strength after cure to prevent it from falling off during the wave soldering process, from flux spray and preheating up to wave soldering. The wet adhesive must maintain its consistency in continuous printing or dispensing process.

Adhesive print for Power88 is shown in Figure 21. Printing, instead of dispensing, the adhesive achieves better planarity and consistent volume. The amount of printed adhesive should be applied sufficiently. Too little adhesive may not hold the component during placement and wave soldering. Too much adhesive may spread up to the land pads during placement, causing solder non-wetting to the component leads and board pads. Adhesive must be cured according to the conditions recommended by the supplier. The adhesive must be fully cured before wave soldering. Recommended stencil thickness for adhesive printing is 6 mils.

Solder Flux

Flux selection is important in wave soldering. Solder flux with low solid content is preferred. Because of its low viscosity, it can wick up solderable pads under the component, flowing into the narrow space between the component and the board by capillary action and facilitating solder wetting during wave soldering. This flux can be applied by spray or foaming. Flux with high solid content is more tolerant of different wave soldering conditions due to its ability to hold the active components of the flux longer and facilitate solder wetting.

No clean-type solder flux is recommended. With the absence of standoff of the PQFN package and narrow spaces between the component and the board, it is difficult to remove the trap solder residues in these areas during board cleaning, so flux with low corrosive content is preferred.

Wave Solder Profile

A standard wave soldering machine usually consists of the fluxing zone, preheating zone, soldering zone, and cleaning zone (cleaning depends on the type of flux). Preheat temperatures and the preheating time should be set according to the flux specification. Too high temperature and too long preheat time may break down the flux activation systems, which causes shorts/icicles. Too low preheat temperature may cause skips or unwanted residues left on the PCB.

Dual-wave soldering is becoming more common in the industry. A typical dual wave soldering profile is shown in Figure 22. The first wave has turbulent wave crest that ensures wetting of all the land pads and allows the molten solder to find its way to all joints on the PCB. The second wave, which is laminar, drains the excess solder from the board, removing the solder bridges. Solder bath temperature

must consider the maximum temperature specified for the package (260°C). Wave soldering profile (preheat ramp rate, speed, peak temperature) depends on the wave soldering equipment and materials used.

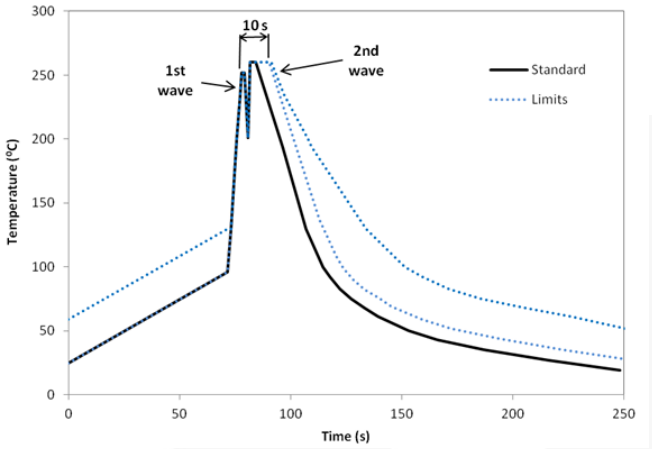

Figure 22. Typical Dual Wave Solder Profile

Inspection of Board-Mounted Power88 Components

Inspection of the mounted component should use 10-20X magnification and transmission or laminograph X-ray.

A well-reflowed solder joint shows evidence of wetting and adherence wherein the solder merges to the soldered surface, forming a contact angle of ≤ 90°. The solder joints should normally have a smooth appearance. On certain occasions; matte, dull, or grainy solder joint may appear. This can be due to the solder alloy used, the component termination, board pad surface finish, or the soldering process. IPC-A-610 provides the inspection methodology and acceptance criteria for this package.

In the wave-soldering process, the assembly is prone to solder bridging, skips, icicles, and other solder joint defects. Set controls in inspecting the solder joints so the leads and drain are not exposed for this type of package. Controls can be accomplished visually and through X-ray inspection.

Figure 23 and Figure 24 show the top and pin-side view of a Power88 that has already been wave soldered on a board. The solder coverage at the drain and flat pin areas of a soldered unit can't be inspected visually because it's not exposed. The appropriate control for this is through X-ray inspection of the solder coverage between the land pad and the solderable surfaces at the bottom of the component. Figure 25 is a typical X-ray image of the wave soldered Power88. X-ray inspection is reliable for detecting solder bridging and solder skips.

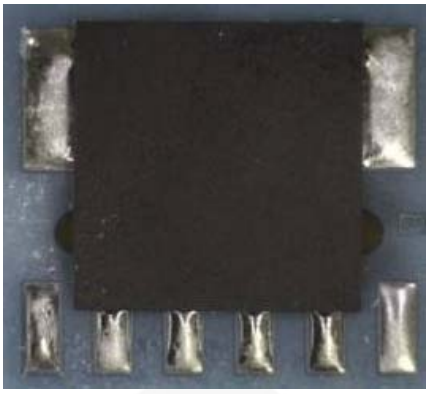

Figure 23. Wave Soldered Power88 (Top View)

Figure 24. Wave Soldered Power88 Gate and Source Leads (Side View)

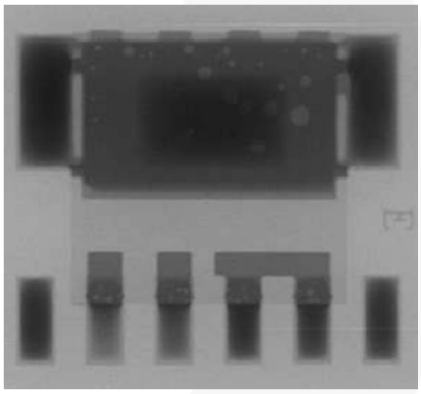

Figure 25. X-ray of Wave-Soldered Power88

Destructive inspection, such as cross-sectioning shown in Figure 26, may be performed for sample monitoring during development stage. With this, it can be verified whether there's a significant tilt of the mounted package due to adhesive print or wave soldering process.

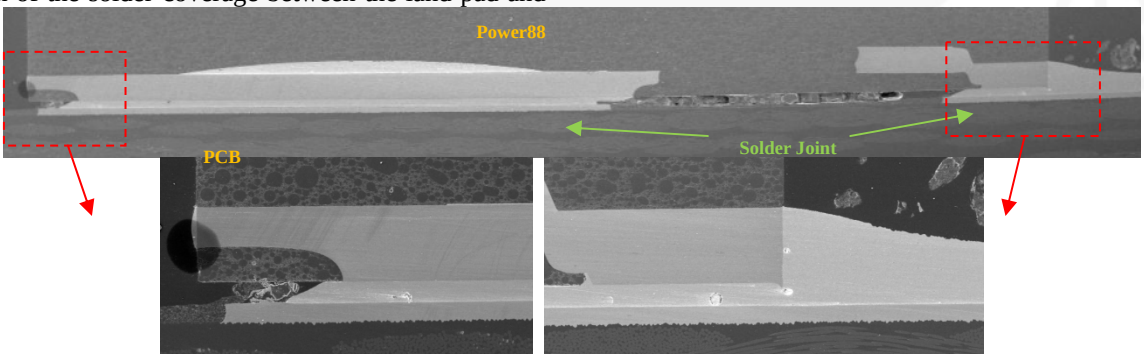

Figure 26. Cross-Section of the Wave Soldered Power88

Table 1. General Rework Guideline PQFN Packages

Step	Tools / Equipment	Guideline / Procedure
Baking	Oven	Baking the board assembly may be necessary, depending on the moisture sensitivity of the board and the surrounding components. The purpose is to eliminate absorbed moisture on these parts and prevent the damaging effects when subjected to sudden ramp of temperature during component removal.
Component Removal	Rework Station Heat Gun	Secure the board on the rework station. Preheat the whole board to minimize warpage of the board when high temperature is applied on the component to be removed. Apply heat into the component using a heat gun. Once the solder joint has melted, remove the component immediately using a vacuum nozzle. Note that applying too much heat on the board can affect the surrounding components! Complete this process quickly! It is also important not to expose the PQFN package to too much heat, which can damage the component.
Land Preparation	Solder Wick Soldering Iron Continuous Vacuum De-soldering System De-soldering Tip	After the component is removed, remove excess solder left on the lands using a continuous vacuum de-soldering system and soldering tip. Soldering iron and solder wicking material can also be used.
Component Installation	Mini Stencil Solder Paste Dispenser Low Magnification Microscope Pick and Place Machine Reflow Oven	After preparing the lands, install a new component into the board. The old component should not be used. Installation of the new component should follow these steps: 1. Solder paste printing / dispensing – Use a mini stencil with the same aperture size and thickness as the one used in the whole-board assembly. Alternatively, a solder paste dispensing system can also be used to put paste on the lands. 2. Inspection – verify sufficient paste is printed on the board. 3. Component placement – on the board manually or the work station. 4. Reflow – reflow the board using the standard reflow profile established for the whole-board assembly.
Inspection	X-Ray Machine Low Magnification Microscope	Inspect the component after reflow using an X-ray machine to check solder joint anomalies, such as solder bridging, beading, and voids.

Table 2. Board-Level Test on PQFN Packages

The PQFN packages are tested to simulate field conditions. The results below are from the environmental and mechanical stress tests performed on these packages. Except for the temperature cycle test that followed the FSC-QAR-0006 standard, all tests performed used daisy chained components and board.

Test	Conditions	Reference Standard	Result
Temperature Cycle Test	-40 °C to +125°C 15 minute dwell time per hot and cold zones 1.60 mm thick, 2-layer board 1500 temperature cycles	FSC-QAR-0006	Passed
Temperature Cycle Test	-40 °C to +125°C 10 minute dwell time ≤20°C / minimum ramp rate 2.35 mm thick 8-layer board 1000 cycles	IPC9701	Passed
Drop Test	Half sine pulse; 1500 G for 0.5ms 105 mm support span 1 mm thick 8 layer board 100 drops	JESD22-B111	Passed
Bending Cycle Test	110 mm support span 75 mm load span 2 mm deflection, sinusoidal 1 mm/s 1 mm thick, 8-layer board 200,000 cycles	JESD22-B113	Passed

References

[1] FSC-QAR-0024, Guideline on the Methodology of Board Level Characterization.
[2] IPC2221, IPC Standard, Generic Standard on Printed Board Design.
[3] Board-Level Evaluation of Power Qual Flat No-Lead (PQFN) Packages, Fairchild Semiconductor Power Seminar 2008-2009 white paper.
[4] ANSI/J-STD-004, IPC and EIA Joint Standard, Requirements for Soldering Fluxes.
[5] IPC7525, IPC Standard, Stencil Design Guidelines.
[6] IPC/EIA J-STD-001 and EIA Joint Standard, Requirements for Soldered Electrical and Electronic Assemblies.
[7] IPC-A-610, IPC standard, Acceptability of Electronic Assemblies.
[8] IPC-7093, Design and Assembly Process Implementation for Bottom Termination Components.
[9] IPC7351, IPC standard, Generic Requirements for Surface Mount Design and Land Pattern Standard.
[10] AN-7528 — Fairchild Application Note, Guidelines for Soldering Surface Mount Components to PC Boards.
[11] IPC/JEDEC J-STD-020, IPC. and JEDEC Joint Standard; Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.
[12] FSC-QAR-0006, Fairchild (internal) General Reliability Requirements.
[13] IPC9701, IPC Standard, Performance Test Methods, and Qualification Requirements for Surface-Mount Solder Attachments.
[14] JESD22-B111, JEDEC Standard, Board Level Drop Test Method of Components for Handheld Electronic Devices.
[15] JESD22-B113, JEDEC Standard, Board Level Cyclic Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Devices.
[16] JESD22-B103, JEDEC Standard, Vibration, Variable Frequency.
[17] IPC/JEDEC J-STD-033, IPC, and JEDEC Joint Standard, Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices.

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