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# AN-5076

## Design a High Power Factor Flyback Converter Using FL7733A for an LED Driver with Ultra-Wide Output Voltage

### Introduction

Due to continuous improvement of high-brightness LED's efficacy, as increasing number of lighting lamps are designed using LED as the replacement for incandescent, fluorescent, plate, down light, etc. LED drivers need highly precise output current regulation because LED brightness and color is dependent on LED current level. At the same time, high Power Factor (PF) and low Total Harmonics Distortion (THD) have become key design requirements for LED driver. In applications where precise output current regulation is required, the conventional control method uses current sensing in the secondary side, which results in additional sensing loss.

Primary-Side Regulation (PSR) for LED drivers can be a solution for achieving international regulations (such as Energy Star) for Solid-State Lighting (SSL) products. PSR controls the output current precisely with the information in the primary side of the power supply only, removing output current sensing loss and eliminating secondary feedback circuitry. This makes it feasible to fit the driver circuit

inside small-form factor retrofit lamps and meet international regulations without excessive cost increase for SSL application. Fairchild Semiconductor's Pulse Width Modulation (PWM) PSR controller, FL7733A, simplifies meeting SSL requirements while eliminating external components. FL7733A provides highly precise output current regulation versus change in the transformer's magnetizing inductance, input and output voltage information, and powerful protection functions for system reliability.

This application note presents practical design considerations for a single-stage flyback LED driver with ultra-wide output voltage ranges using the FL7733A. It includes the procedure for designing the transformer and selecting key components. The design procedure is verified through an experimental prototype converter. Figure 1 shows the typical application circuit of primary-side controlled flyback LED driver using the FL7733A.

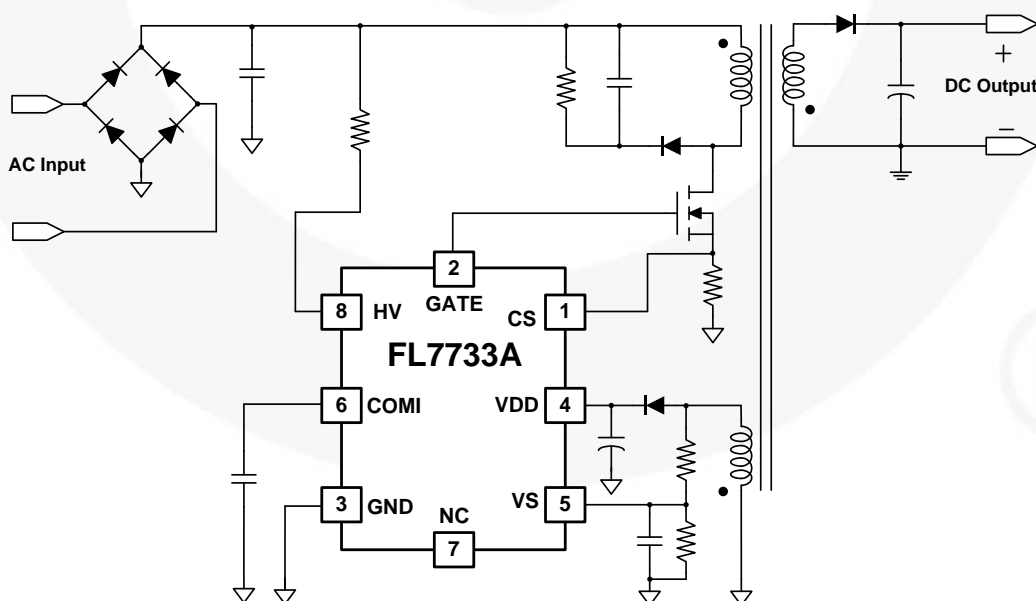


Figure 1. Typical Application Circuit

## Operation Principle of Primary-Side Regulation

Generally, Discontinuous Conduction Mode (DCM) operation is preferred for single-stage primary-side flyback converters because it allows better output regulation, higher PF, and lower THD. The operation principles of DCM flyback converter are as follows:

### Mode I

During the MOSFET turn-on time ( $t_{ON}$ ), input voltage ( $V_{IN}$ ) is applied across the transformer's primary-side inductance ( $L_m$ ). Then, drain current ( $I_{DS}$ ) of the MOSFET increases linearly from zero to the peak value ( $I_{DS,PK}$ ), as shown in Figure 3. During this time, the energy is drawn from the input and stored in the inductor.

### Mode II

When the MOSFET (Q) is turned off, the energy stored in the transformer forces the rectifier diode (D) to turn on.

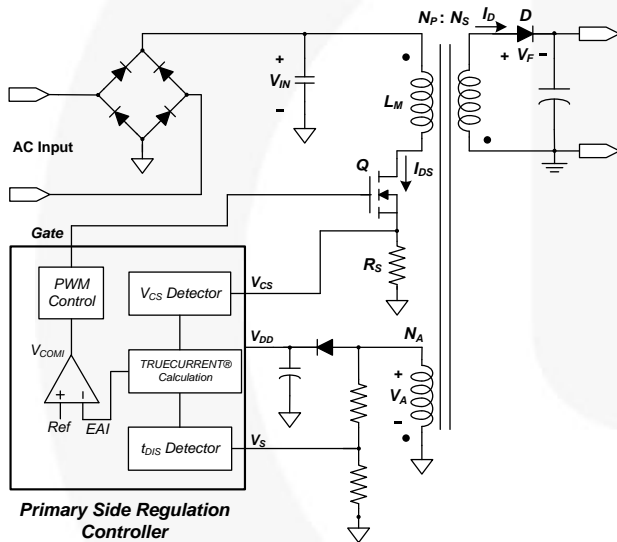


Figure 2. Primary-Side Regulated Flyback Converter

While the diode is conducting, output voltage ( $V_{OUT}$ ) and the diode forward-voltage drop ( $V_F$ ), is applied across the transformer's secondary-side inductance and diode current ( $I_D$ ) decreases linearly from the peak value ( $I_{DS,PK} \cdot N_P/N_S$ ) to zero. At the end of inductor current discharge time ( $t_{DIS}$ ), all energy stored in the transformer has been delivered to the output.

### Mode III

When the diode current reaches zero, the transformer auxiliary winding voltage begins to oscillate by the resonance between the primary-side inductance ( $L_m$ ) and the effective capacitor loaded across MOSFET (Q).

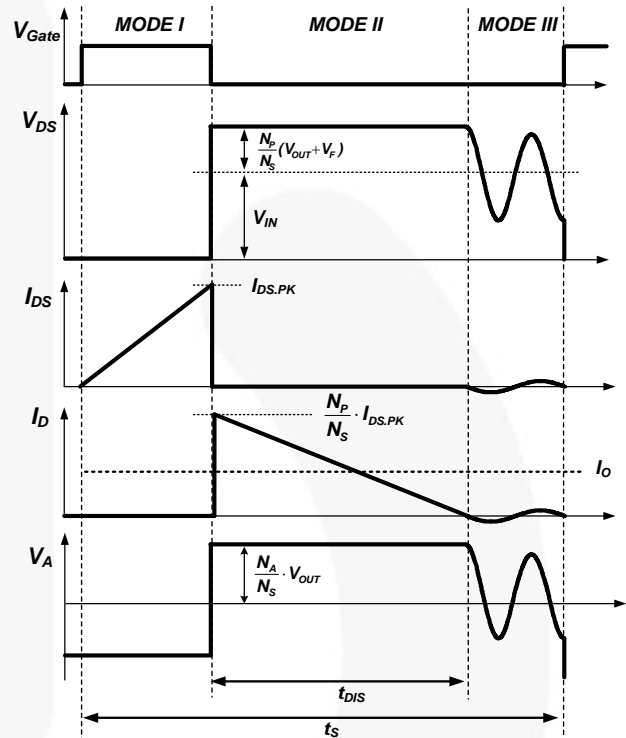


Figure 3. Key Waveforms of PSR Flyback Converter

The output current can be estimated using the peak drain current and inductor current discharge time because output current is the same as the average of the diode current in steady state. The peak value of the drain current is determined by the CS peak voltage detector and the inductor current discharge time ( $t_{DIS}$ ) is sensed by the  $t_{DIS}$  detector. With peak drain current, inductor current discharging time, and operating switching period information; the innovative TRUECURRENT<sup>®</sup> calculation block estimates output current as follows:

$$I_o = \frac{1}{2} \cdot \frac{t_{DIS}}{t_s} \cdot V_{CS} \cdot \frac{N_P}{N_S} \cdot \frac{1}{R_S} \quad (1)$$

$$\frac{t_{DIS}}{t_s} \cdot V_{CS} = 0.25 \quad (2)$$

$$I_o = 0.125 \cdot \frac{N_P}{N_S} \cdot \frac{1}{R_S} \quad (3)$$

## Design Procedure

A design procedure for a single-stage flyback LED driver, based on FL7733A, is presented in this section using the schematic of Figure 1 as the reference. An offline LED driver with 50 W (50 V / 1 A) output has been selected as a design example. The design specifications are:

- Input voltage range: 90 ~ 264 V<sub>AC</sub> and 50 ~ 60 Hz
- Nominal output voltage and current: 50 V / 1.0 A
- Operating output voltage: 7 V ~ 55 V
- Minimum efficiency: 88%
- Operating switching frequency: 65 kHz
- Maximum duty: 40%

### Step 1. Transformer Primary-Side Inductance Selection (L<sub>m</sub>)

FL7733A operates with constant turn-on and turn-off time, as shown Figure 4. When MOSFET turn-on time (t<sub>ON</sub>) and switching period (t<sub>s</sub>) are constant, I<sub>IN</sub> is proportional to V<sub>IN</sub> and it can achieve high power factor.

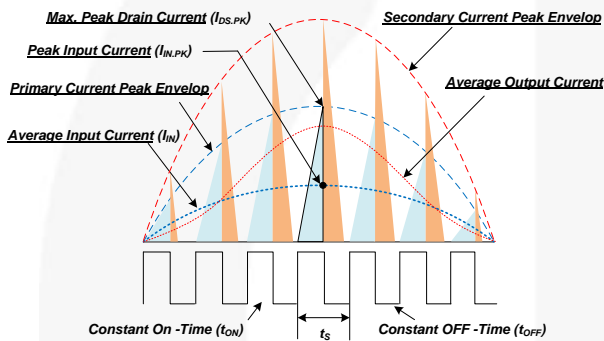


Figure 4. Theoretical Waveform

The single-stage flyback using FL7733A is assumed to operate in DCM due to constant t<sub>ON</sub> and t<sub>s</sub>. Input voltage is applied across the magnetizing inductance (L<sub>m</sub>) during t<sub>ON</sub>, charging the magnetic energy in L<sub>m</sub>. Therefore, the maximum peak switch current (I<sub>DS,PK</sub>) of the MOSFET occurs at peak point of line voltage, as shown Figure 4. The peak input current (I<sub>IN,PK</sub>) is also shown at the peak input voltage of one line cycle. Once the maximum t<sub>ON</sub> is decided, I<sub>DS,PK</sub> of MOSFET is obtained at the minimum line input voltage and full-load condition as:

$$I_{DS,PK} = \frac{t_{ON} \cdot V_{IN,PK}}{L_m} \quad (4)$$

where V<sub>IN,PK</sub> and t<sub>ON</sub> are the peak input voltage and the maximum turn-on time at the minimum line input voltage, respectively.

Using Equation (4), the peak input current is obtained by:

$$I_{IN,PK} = \frac{1}{2} \cdot (t_{ON}) \left( \frac{V_{IN,PK}}{L_m} \cdot t_{ON} \right) \cdot f_s \quad (5)$$

then, I<sub>IN,PK</sub> and V<sub>IN,PK</sub> can be expressed as:

$$I_{IN,PK} = \sqrt{2} \cdot I_{IN,rms} \quad (6)$$

$$V_{IN,PK} = \sqrt{2} \cdot V_{IN,rms} \quad (7)$$

where the I<sub>IN,rms</sub> and V<sub>IN,rms</sub> are rms line input current and voltage, respectively.

t<sub>ON</sub> is required to calculate the required L<sub>m</sub> value. With Equation (5) ~ (7), the turn-on time, t<sub>ON</sub>, is obtained as:

$$t_{ON}^2 = \frac{2L_m \cdot I_{IN,rms}}{V_{IN,rms} \cdot f_s} \quad (8)$$

The input power is given as:

$$P_{IN} = I_{IN,rms} \cdot V_{IN,rms} = \frac{P_o}{\eta} \quad (9)$$

With Equation (8) and (9), the L<sub>m</sub> value is obtained as:

$$L_m = \frac{\eta \cdot (V_{IN,rms})^2 \cdot f_s \cdot t_{ON}^2}{2P_o} \quad (10)$$

**(Design Example)** When the minimum input voltage is 90 V<sub>AC</sub>, the maximum t<sub>ON</sub> occurs at full-load condition. The maximum t<sub>ON</sub> at 65 kHz of the operating frequency can be decided by maximum duty, then the magnetizing inductance is obtained as:

$$L_m = \frac{0.88 \times 90^2 \times 65 \times 10^3 \times (6.2 \times 10^{-6})^2}{2 \times 50} = 175 \mu H$$

The drain peak current of MOSFET at nominal output power is calculated as:

$$I_{DS,PK} = \frac{6.2 \times 10^{-6} \times \sqrt{2} \times 90}{175 \times 10^{-6}} = 4.51 A$$

### Step 2. Sensing Resistor and n<sub>PS</sub> Selection

FL7733A adopts the TRUECURRENT<sup>®</sup> calculation method for constant output current (I<sub>o</sub>) regulation, as defined in Equation (1). The output current is proportional to turn ratio n<sub>ps</sub> between the primary and secondary windings of the transformer and inversely proportional to sensing resistor value (R<sub>s</sub>). The FL7733A implements cycle-by-cycle current limit by detecting V<sub>CS</sub> to protect the system from an LED short or overload. Therefore, the V<sub>CS</sub> level needs to handle the rated system power without triggering current-limit protection. It is typical to set the cycle-by-cycle limit level (typical: 0.85 V) at 15 ~ 20% higher than CS peak voltage (V<sub>CS,PK</sub>) at full-load condition. MOSFET peak current (I<sub>SW,PK</sub>) is converted into V<sub>CS,PK</sub> as:

$$V_{CS,PK} = I_{SW,PK} \cdot R_s \quad (11)$$

According to Equation (3), the primary-to-secondary turn ratio is determined by the sensing resistor and output current as:

$$n_{ps} = \frac{I_o \times R_s}{0.125} \quad (12)$$

**(Design Example)** Once V<sub>CS,PK</sub> is set as 0.85 V, the sensing resistor value and n<sub>ps</sub> are obtained as:

$$R_s = \frac{V_{CS,PK}}{I_{SW,PK}} = \frac{0.85}{4.51} = 0.188 \Omega$$

$$n_{ps} = \frac{1 \times 0.19}{0.125} = 1.52$$

### Step 3. $n_{AS}$ and $n_{AP}$ Selection

When  $V_{DD}$  voltage is 23 V, the FL7733A stops its switching operation due to Over-Voltage Protection (OVP). So,  $n_{AS}$  and  $n_{AP}$  can be determined as follows:

$$n_{AS} = \frac{V_{DD,OVP}}{V_{O,OVP}} = \frac{23}{V_{O,OVP}} \quad (13)$$

$$n_{AP} = \frac{n_{AS}}{n_{PS}} \quad (14)$$

where,  $n_{AS}$  is the auxiliary-to-secondary turns ratio and  $n_{AP}$  is the auxiliary to primary turns ratio of transformer.

**(Design Example)** Once output over-voltage level is set as 56 V,  $n_{AS}$  is obtained as:

$$n_{AS} = \frac{23}{56} = 0.41$$

$$n_{AP} = \frac{0.41}{1.52} = 0.27$$

### Step 4. Transformer Design

The number of primary turns is determined by Faraday's law.  $N_{p,min}$  is fixed by the peak value of the minimum line input voltage across the primary winding and the maximum on time. The minimum number of turns for the transformer primary side to avoid core saturation is given by:

$$N_{p,min} = \frac{V_{IN,min,pk} \cdot t_{ON}}{B_{sat} \cdot A_e} \quad (15)$$

where  $A_e$  is the cross-sectional area of the core in  $mm^2$  and  $B_{sat}$  is the saturation flux density in Tesla.

Since the saturation flux density decreases as temperature rises, the high-temperature characteristics must be considered if the transformer is used inside an enclosed case.

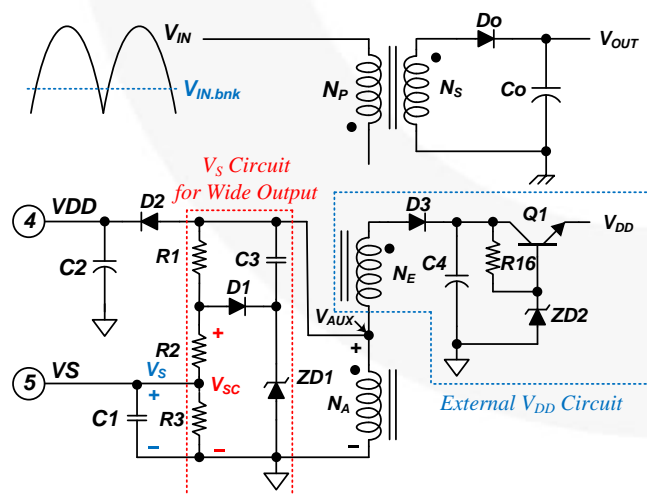


Figure 5. VS Circuit for Wide Output Voltage Range

Because FL7733A's  $V_{DD}$  operation range is 8.75 ~ 23 V, MOSFET switching will be shut down by triggering UVLO if output voltage is lower than  $V_{OUT-UVLO}$  ( $8.75 \times N_S / N_A$ ). Therefore,  $V_{DD}$  should be supplied properly without triggering UVLO across the wide output voltage range of 7 ~ 55 V.  $V_{DD}$  can be supplied by adding external winding  $N_E$  and  $V_{DD}$  circuits composed of a voltage regulator, as shown in Figure 5. The  $N_E$  should be designed so  $V_{DD}$  can be supplied without triggering UVLO at minimum output voltage ( $V_{min,OUT}$ ). The external winding,  $N_E$ , can be determined as:

$$N_E > \frac{(8.75 + V_{CE,Q1} + V_{FD3})}{(V_{F,Do} + V_{min,OUT})} \times N_S - N_A \quad (16)$$

where  $V_{CE,Q1}$  is Q1's collector-emitter saturation voltage, and  $V_{F,D3}$  is D3's forward voltage, and  $V_{F,Do}$  is Do's forward voltage at the minimum output voltage.

**(Design Example)** An PQ3220 core is selected for the transformer and the minimum turn number of the transformer primary winding to avoid core saturation is given by:

$$N_{p,min} = \frac{\sqrt{2} \cdot 90 \times 6.2 \times 10^{-6}}{0.22 \times 141 \times 10^{-6}} = 25.3$$

Once  $N_p$  is selected with a margin about 5% ~ 10% to avoid core saturation:

$$N_p = 25.3 \times 1.1 = 27.8$$

Once the turn number of the primary side ( $N_p$ ) is determined as 28, the turn number of the secondary side ( $N_s$ ) is obtained by:

$$N_s = 28 \div 1.52 = 18.4$$

Once the turn number of the secondary winding ( $N_s$ ) is determined as 19, the turn number of the auxiliary winding ( $N_A$ ) is obtained by:

$$N_A = 19 \times 0.41 = 7.79$$

Then  $N_A$  is determined to be 8.

If  $V_{CE,Q1}$  and  $V_{F,D3}$  are set as 0.5 V and 0.7 V, respectively, and assuming  $V_{F,Do}$  is 1 V at minimum output voltage 7 V; the external winding  $N_E$  can be obtained as:

$$N_E > \frac{(8.75 + 0.5 + 0.7)}{(1 + 7)} \times 19 - 8 = 15.6$$

Then  $N_E$  is determined to be 16.

## Step 5. $V_S$ Circuits for Wide Output Range

The first consideration for R1, R2, and R3 selection is that  $V_S$  should be 2.45 V at the end of diode current conduction time to operate at 65 kHz switching frequency at the rated power. The second consideration is  $V_S$  blanking, as explained below. The output voltage is detected by the auxiliary winding and a resistive divider connected to the VS pin, as shown in Figure 5. However, in a single-stage flyback converter without a DC link capacitor, auxiliary winding voltage cannot be clamped to reflected output voltage over the whole input line cycle due to the small  $L_m$  current, which induces  $V_S$  voltage sensing error, as shown in Figure 6. Frequency decreases rapidly at the zero-crossing point of line voltage, which can cause LED light flicker. To maintain constant frequency over the whole sinusoidal line voltage,  $V_S$  blanking disables  $V_S$  sampling when line voltage is below a particular level by sensing the auxiliary winding.

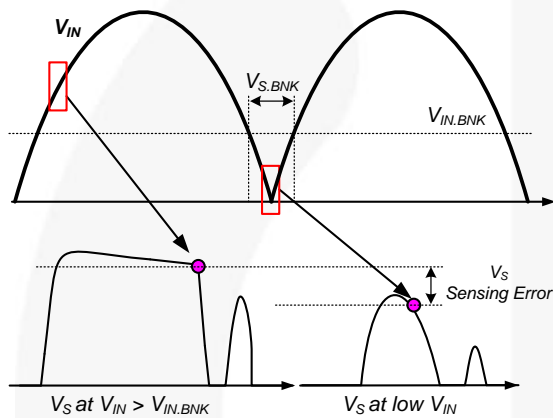


Figure 6.  $V_S$  Waveform

In wide output application, the  $V_S$  level in normal condition should be maintained between 0.6 and 3 V to avoid triggering SLP and  $V_S$  OVP. This is feasible using additional  $V_S$  circuits, as shown in Figure 5.

Considering the high switching frequency, up to 50% of rated output voltage and  $V_S$  blanking level for  $V_{IN,blk}$ , the Zener diode voltage ( $V_{ZD1}$ ), R1, R2, and R3 can be obtained as:

$$V_{ZD1} < (V_{DD,OVP} \times 0.5) - V_{F,D1} \quad (17)$$

where  $V_{F,D1}$  is forward voltage of D1 connected in series with Zener diode ZD1.

Considering Zener diode regulation range and its power rating, R1 can be selected to limit the Zener diode current  $I_{ZD1}$  to 10 mA:

$$R1 = \frac{(V_{DD,OVP} - V_{SC})}{10mA} \quad (18)$$

where  $V_{SC}$  is voltage clamped by D1 and ZD1.

$$R2 = n_{AP} \times \frac{V_{IN,blk}}{I_{VS,blk}} - R1 \quad (19)$$

where  $V_{IN,blk}$  is the line voltage level for  $V_S$  blanking and  $I_{VS,blk}$  is the current level for  $V_S$  blanking.

$$R3 \geq \frac{R2 \times 2.45}{V_{SC} - 2.45} \quad (20)$$

**(Design Example)** The voltage divider network is determined as:

$$V_{ZD1} < (23 \times 0.5) - 0.7 = 10.8$$

Then  $V_{ZD1}$  is determined to be 10 V and, assuming  $V_{F,D1}$  is 0.7 V, R1 can be obtained by:

$$R1 = \frac{23 - 10 + 0.7}{10 \times 10^{-3}} = 1.23 \text{ k}\Omega$$

R1 can be selected as 1.2 k $\Omega$ . Once  $V_{IN,blk}$  and  $I_{VS,blk}$  are 50 V and 90  $\mu$ A, respectively, R2 is obtained by:

$$R2 = \frac{8 \times 50}{28 \times 90 \times 10^{-6}} - 1.2 \text{ k}\Omega = 157.53 \text{ k}\Omega$$

Once R2 is determined to be 160 k $\Omega$ , R3 is obtained by:

$$R3 \geq \frac{160 \times 2.45}{10 + 0.7 - 2.45} = 47.51 \text{ k}\Omega$$

Then R3 can be selected as 51 k $\Omega$ .

After selecting R3, the  $V_S$  level should be checked to see if  $V_S$  voltage across R3 is over 0.6 V at the minimum output voltage 7 V as given by:

$$V_S = \frac{(N_A + N_E)}{N_S} \cdot (7V + V_{F,Do}) \cdot \left( \frac{R3}{R1 + R2 + R3} \right) > 0.6V$$

If  $V_S$  is less than 0.6 V, reduce the Zener diode voltage  $V_{ZD1}$  and increase R3 values through Equations (17) to (20).

A bypass capacitor, C1, of 5 ~ 10 pF closely between the VS and GND pins is recommended to bypass the switching noise. The value of the capacitor may affect constant-current regulation. If excessively high  $V_S$  capacitance is selected, discharge time,  $t_{DIS}$ , becomes longer and the output current is lower, compared to a small  $V_S$  capacitor.

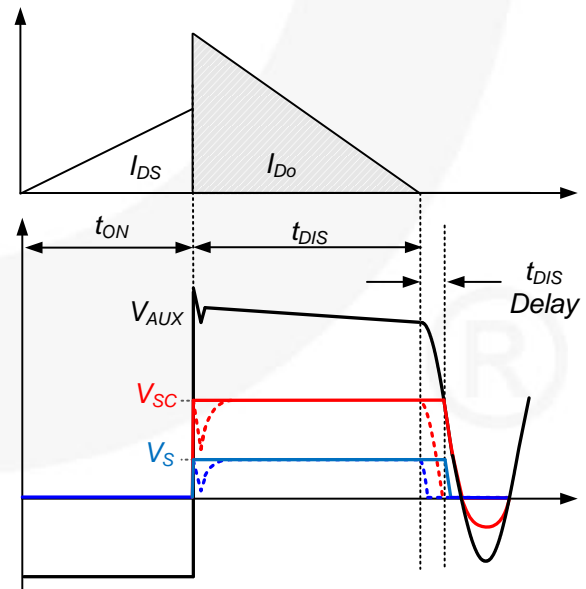


Figure 7.  $V_S$  Waveform for  $t_{DIS}$  Detection

An additional consideration in  $V_S$  circuits for wide output voltage range is  $t_{DIS}$  delay caused by the voltage difference between  $V_{AUX}$  and  $V_{SC}$  when  $V_{AUX}$  across auxiliary winding is clamped to  $V_{SC}$  as shown in Figure 7. This delay lasts until  $V_{AUX}$  is the same as  $V_{SC}$  and may affect constant output current regulation. It can be removed by putting a capacitor, C9, between the auxiliary winding and the cathode of Zener diode, ZD1. The  $V_{AUX}$  is divided with capacitor voltage  $V_{C3}$  and  $V_{ZD1}$  when the gate is turned off. Then  $V_{C3}$  is maintained to its voltage without discharging at the moment, but  $V_{ZD2}$  is decreased to  $V_{AUX} - V_{C3}$  when the diode current  $I_D$  reaches zero. Therefore,  $V_S$  can follow  $V_{AUX}$  as the dotted line shown in Figure 7. C3 should be selected to the proper value depending on resonant frequency determined by the resonance between magnetizing inductance  $L_m$  and MOSFET  $C_{OSS}$ . The 330 pF used in this application was selected by trial and error. Its value can be obtained as:

$$C_3 = \frac{300 \text{ kHz}}{f_r} \cdot 330 \text{ pF} \quad (21)$$

where  $f_r$  is the resonance frequency determined by the resonance between  $C_{OSS}$  and  $L_m$ .

## Step 6. Calculate the Voltage and Current of the Switching Devices

**Primary-Side MOSFET:** The voltage stress of the MOSFET is discussed in determining the transformer turns ratio. Assuming the drain voltage overshoot is considered as certain voltage  $V_{OS}$ , the maximum drain voltage is given as:

$$V_{DS(max)} = V_{IN,max.pk} + \frac{N_p}{N_s} (V_{O,OV} + V_{F,D0}) + V_{OS} \quad (22)$$

where  $V_{IN,max.pk}$  is the maximum line peak voltage and  $V_{OS}$  is the drain voltage overshoot. The rms current ( $I_{SW,rms}$ ) through the MOSFET is given as:

$$I_{DS,rms} \approx I_{pk} \cdot \sqrt{\frac{t_{ON} \cdot f_s}{6}} \quad (23)$$

**(Design Example)** Assuming that drain voltage overshoot is about 100 V, the maximum drain voltage across the MOSFET is calculated as:

$$V_{DS(max)} = 265 \times \sqrt{2} + \frac{28}{19} \times (56 + 1) + 100 = 559 \text{ V}$$

The rms current through the MOSFET is:

$$I_{DS,rms} \approx 4.51 \times \sqrt{\frac{6.2 \times 10^{-6} \times 65 \times 10^3}{6}} = 1.17 \text{ A}$$

**Secondary-Side Diode:** The maximum reverse voltage and rms current of the rectifier diode are obtained as:

$$V_D = V_O + \frac{N_s}{N_p} \cdot V_{in,max.pk} \quad (24)$$

$$I_{D,rms} \approx I_{SW,rms} \times \sqrt{\frac{V_{in,min.pk}}{2 \times V_{RO}}} \cdot \frac{N_p}{N_s} \quad (25)$$

**(Design Example)** Diode voltage and current are obtained as:

$$V_D = 56 + \frac{19}{28} \times 265 \times \sqrt{2} = 310 \text{ V}$$

$$I_{D,rms} \approx 0.357 \times \sqrt{\frac{127}{2 \times 74.1}} \cdot \frac{60}{20} = 0.991 \text{ A}$$

## Step 7. Design RCD Snubber in Primary Side

When the power MOSFET is turned off, there is a high-voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of the device. Therefore, it is necessary to use an additional network to clamp the voltage. The RCD snubber circuit and its waveform are shown in Figure 8. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode ( $D_{SN}$ ) once the MOSFET drain voltage exceeds the cathode voltage of the snubber diode. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle. The snubber capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable for these reasons.

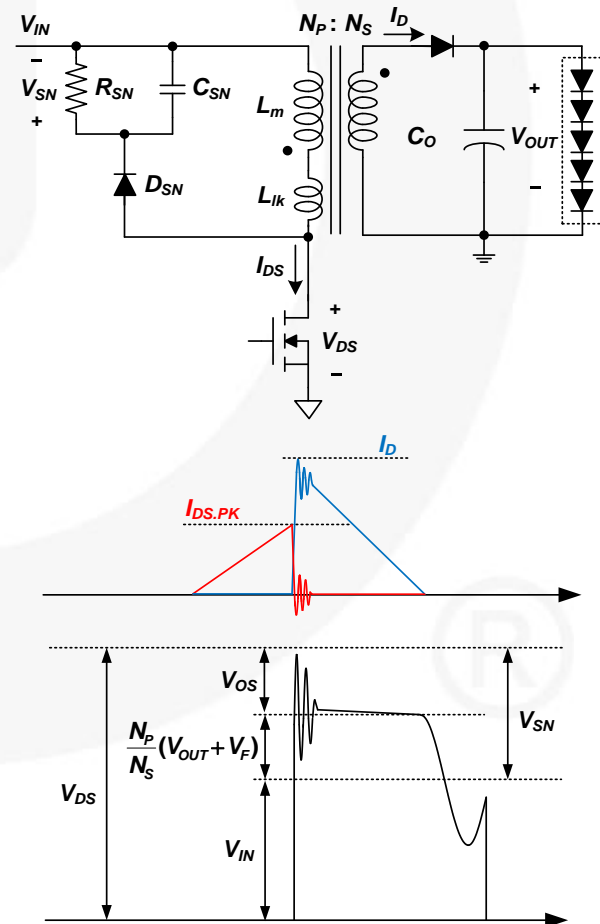


Figure 8. Snubber Circuit and Waveforms



Snubber capacitor voltage at full-load condition is given as:

$$V_{SN} = V_{RO} + V_{OS} \quad (26)$$

The power dissipated in the snubber network is obtained as:

$$P_{SN} = \frac{V_{SN}^2}{R_{SN}} = \frac{1}{2} L_{IK} \cdot I_{DS,PK}^2 \cdot \frac{V_{SN}}{V_{SN} - V_{RO}} \cdot f_S \quad (27)$$

where  $L_{IK}$  is leakage inductance,  $V_{SN}$  is snubber capacitor voltage at full load, and  $R_{SN}$  is the snubber resistor.

The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted. The snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_S} \quad (28)$$

In general, 5 ~ 20% ripple of the selected capacitor voltage is reasonable. In this snubber design, neither the lossy discharge of the inductor nor stray capacitance is considered.

**(Design Example)** Since the voltage overshoot of the drain voltage has been determined to be the same as the reflected output voltage, the snubber voltage is:

$$V_{SN} = V_{RO} + V_{OS} = 200 \text{ V}$$

The leakage inductance is measured as 3  $\mu\text{H}$ . Then the loss in snubber networking is given as:

$$P_{SN} = \frac{1}{2} \times 5 \times 10^{-6} \times 4.56^2 \times \frac{200}{200 - 84} \times 65 \times 10^3 = 3.48 \text{ W}$$

$$R_{SN} = \frac{200^2}{3.48} = 11.45 \text{ k}\Omega$$

To allow 15% ripple on the snubber voltage (200 V):

$$C_{SN} = \frac{200}{0.15 \times 200 \times 12 \cdot 10^3 \times 65 \cdot 10^3} = 8.9 \text{ nF}$$

## PCB Layout Guidance

PCB layout for a power converter is as important as circuit design because PCB layout with high parasitic inductance or resistance can lead to severe switching noise and cause system instability. PCB should be designed to minimize coupling of switching noise into control signals.

1. The signal ground and power ground should be separated and connected only at one position (GND pin) to avoid ground loop noise. The power ground path from the bridge diode to the sensing resistors should be short and wide.
2. Gate-driving current path (GATE –  $R_{GATE}$  – MOSFET –  $R_{CS}$  – GND) must be as short as possible.
3. Control pin components; such as  $C_{COM1}$ ,  $C_{VS}$ , and  $R_{VS2}$ ; should be close to the assigned pin and signal ground.
4. High-voltage traces related to the drain of the MOSFET and RCD snubber should be kept far way from control circuits to avoid unnecessary interference.
5. If a heat sink is used for the MOSFET, connect this heat sink to the power ground.
6. The auxiliary winding ground should be connected closer to the GND pin than the control pin components' ground.

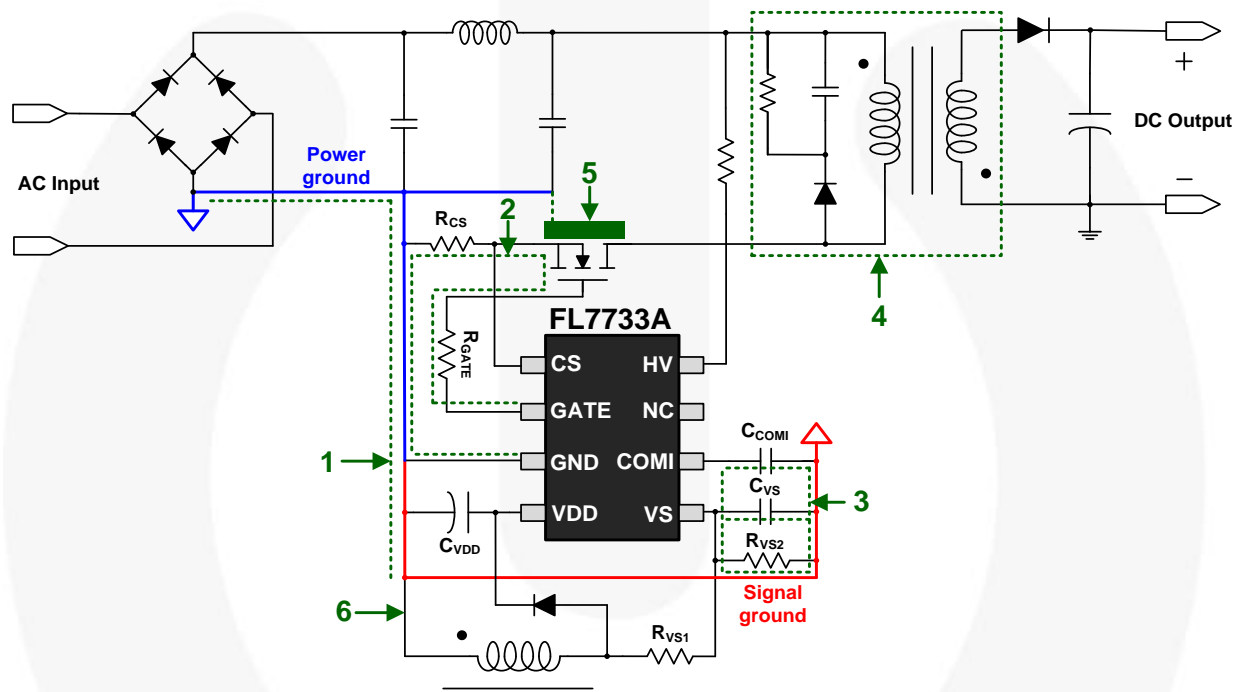


Figure 9. Layout Example

## Lab Note

Before modifying or soldering / de-soldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during the process. This

device is sensitive to electrostatic discharge (ESD). To improve yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

## Schematic of Design example

Figure 10 shows the schematic of the 50 W LED driver design example. A PQ3220 core is used for the transformer. Figure 11 shows the transformer information.

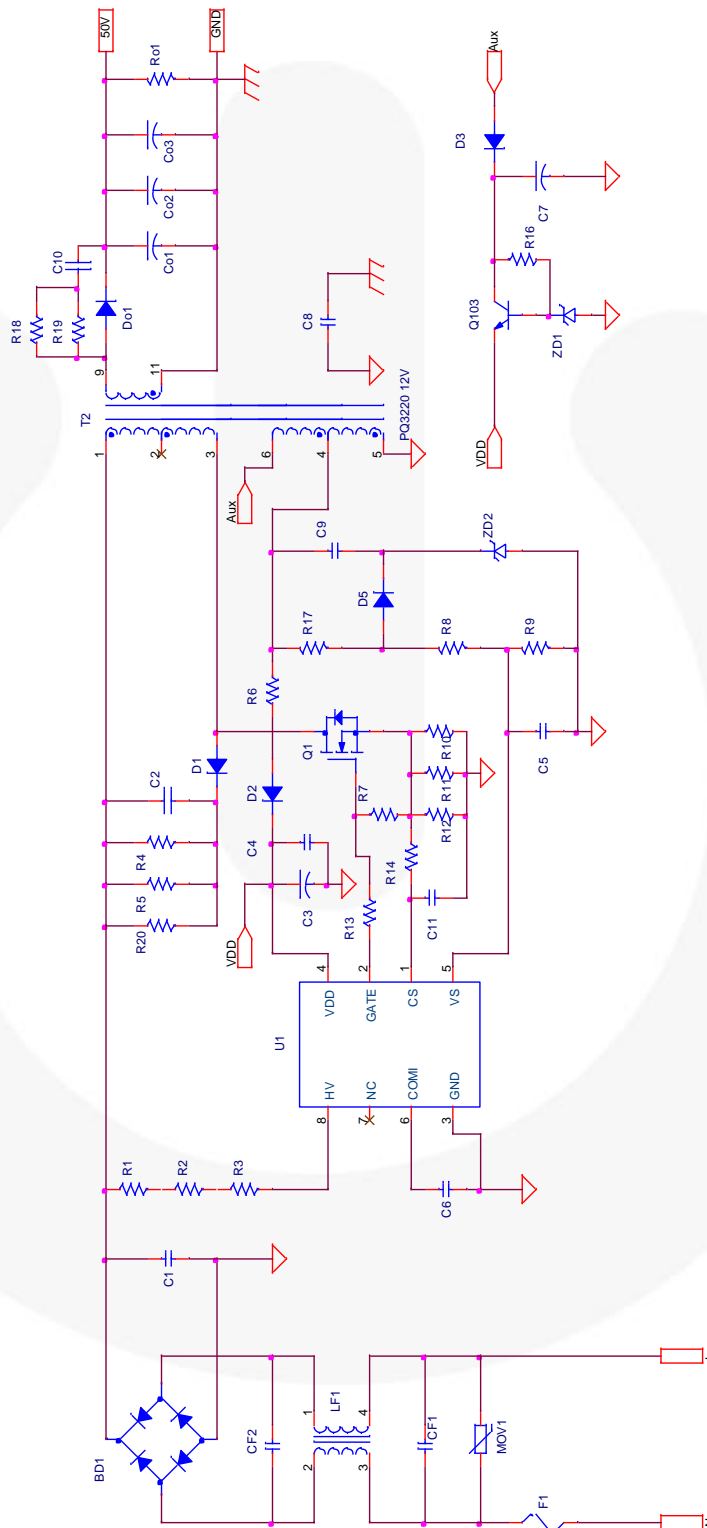


Figure 10. Schematic of the FL7733A 50 W Design Example

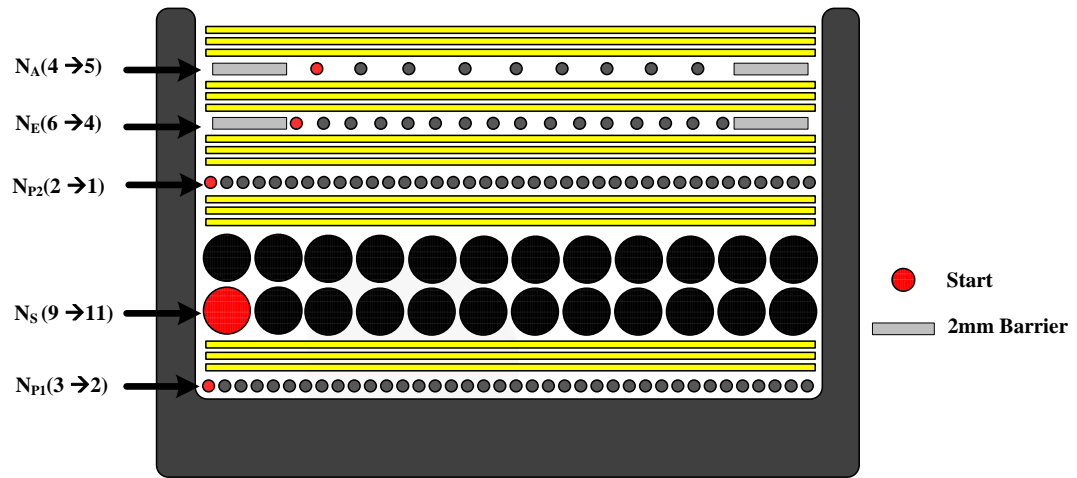


Figure 11. Transformer Winding Structure

Table 1. Winding Specifications

No	Winding	Pin(S → F)	Wire	Turns	Winding Method
1	NP1	3 → 2	0.45 $\phi$	17 Ts	Solenoid Winding
2	Insulation: Polyester Tape t = 0.025 mm, 3-Layer				
3	NS	9 → 11	0.7 $\phi$ (TIW)	19 Ts	Solenoid Winding
4	Insulation: Polyester Tape t = 0.025 mm, 3-Layer				
5	NP2	2 → 1	0.45 $\phi$	11 Ts	Solenoid Winding
6	Insulation : Polyester Tape t = 0.025 mm, 3-Layer				
7	NE	6 → 4	0.25 $\phi$	16 Ts	Solenoid Winding
8	Insulation: Polyester Tape t = 0.025 mm, 3-Layer				
9	NA	4 → 5	0.25 $\phi$	8 Ts	Solenoid Winding
10	Insulation: Polyester Tape t = 0.025 mm, 3-Layers				

Table 2. Electrical Characteristics

	Pin	Specifications	Remark
Inductance	1 – 3	170 $\mu$ H $\pm$ 10%	60 kHz, 1 V
Leakage	1 – 3	5 $\mu$ H	60 kHz, 1 V, Short All Output Pins

## Bill of Materials

Item No.	Part Reference	Part Number	Qty.	Description	Manufacturer
1	BD1	G3SBA60	1	4 A / 600 V, Bridge Diode	Vishay
2	CF1	MPX AC275V 474K	1	470 nF / 275 V <sub>AC</sub> , X-Capacitor	Carli
3	CF2	MPX AC275V 224K	1	220 nF / 275 V <sub>AC</sub> , X-Capacitor	Carli
4	Co1, Co2, Co3	KMG 470 μF / 63 V	3	470 μF / 63 V, Electrolytic Capacitor	Samyoung
5	C1	MPE 630 V 334K	1	330 nF / 630 V, MPE Film Capacitor	Sungho
6	C2	C1206C103KDRACTU	1	10 nF / 630 V, SMD Capacitor 1206	Kemet
7	C3	KMG 10 μF / 35 V	1	10 μF / 35 V, Electrolytic Capacitor	Samyoung
8	C4	C0805C104K5RACTU	1	100 nF / 50 V, SMD Capacitor 2012	Kemet
9	C5	C0805C519C3GACTU	1	5.1 pF / 25 V, SMD Capacitor 2012	Kemet
10	C6	C0805C205J3RACTU	1	2.2 μF / 25 V, SMD Capacitor 2012	Kemet
11	C7	KMG 1 μF / 50 V	1	1 μF / 50 V, Electrolytic Capacitor	Samyoung
12	C8	SCFz2E472M10BW	1	4.7 nF / 250 V, Y-Capacitor	Samwha
13	C9	C1206C331K5RACTU	1	330 pF / 630 V, SMD Capacitor 1206	Kemet
14	C10	C1206C471KDRACTU	1	470 pF / 630 V, SMD Capacitor 1206	Kemet
15	C11	C0805C101C3GACTU	1	100 pF / 25 V, SMD Capacitor 0805	Kemet
16	Do1	FFPF08H60S	1	600 V / 8 A, Hyper-Fast Rectifier	Fairchild Semiconductor
17	D1, D3	RS1M	2	1000 V / 1 A, Ultra-Fast Recovery Diode	Fairchild Semiconductor
18	D2	1N4003	1	200 V / 1 A, General-Purpose Rectifier	Fairchild Semiconductor
19	D5	LL4148	1	100 V / 0.2 A, Small Signal Diode	Fairchild Semiconductor
20	F1	250 V / 2 A	1	250 V / 2 A, Fuse	Bussmann
21	LF1	B82733F	1	40 mH Common Inductor	EPCOS
22	MOV1	SVC681D-10A	1	Metal Oxide Varistor	Samwha
23	Q1	FCPF400N80Z	1	800 V / 400 mΩ, N-Channel MOSFET	Fairchild Semiconductor
24	Q103	KSP42	1	High-Voltage NPN Transistor	Fairchild Semiconductor
25	Ro1	RC1206JR-0727KL	1	27 kΩ, SMD Resistor 1206	Yageo
26	R1, R7	RC1206JR-0710KL	2	10 kΩ, SMD Resistor 1206	Yageo
27	R2, R3	RC1206JR-0715KL	2	15 kΩ, SMD Resistor 1206	Yageo
28	R4, R5, R20	RC1206JR-07100KL	3	100 kΩ, SMD Resistor 1206	Yageo
29	R6, R15	RC1206JR-0710RL	2	10 Ω, SMD Resistor 1206	Yageo
30	R8	RC0805JR-07160KL	1	160 kΩ, SMD Resistor 0805	Yageo
31	R9	RC0805JR-0727KL	1	56 kΩ, SMD Resistor 0805	Yageo
32	R10	RC1206JR-070R2L	1	0.2 Ω, SMD Resistor 1206	Yageo
33	R11, R12	RC1206JR-073RL	2	3.0 Ω, SMD Resistor 1206	Yageo
34	R13	RC0805JR-0710RL	1	10 Ω, SMD Resistor 0805	Yageo
35	R14	RC0805JR-07510RL	1	510 Ω, SMD Resistor 0805	Yageo
36	R16	RC1206JR-0730kL	1	30 kΩ, SMD Resistor 1206	Yageo
37	R17	RC1206JR-071KL	1	1.0 kΩ, SMD Resistor 1206	Yageo
38	R18, R19	RC1206JR-07300RL	2	300 Ω, SMD Resistor 1206	Yageo
39	T2	PQ3220	1	PQ Core, 12Pin Transformer	TDK
40	U1	FL7733A	1	Main PSR Controller	Fairchild Semiconductor
41	ZD1	15 V	1	15 V Zener Diode	Fairchild Semiconductor
42	ZD2	10 V	1	10 V Zener Diode	Fairchild Semiconductor

## Experimental Result of Design Example

To show the validity of the design procedure presented in this application note, the converter described by the design example was built and tested.

Figure 12 shows the normal operation waveforms at minimum and maximum line voltage condition. Input current waveform is sinusoidal and high PF and low THD performance can be achieved by DCM control.

Figure 13 shows key waveforms at minimum input condition. The conduction time and drain peak current for the transformer inductance designed in STEP-1 are 6.2  $\mu$ s and 4.5 A, respectively.

Figure 14 shows the CC tolerance measured over the entire line and output voltage ranges. CC over universal line at rated output voltage is less than  $\pm 0.3\%$  and total CC regulation for whole line and ultra-wide output voltage range (7 V ~ 55 V) is  $\pm 1.76\%$ .

Figure 15 shows the PF and THD measured at rated load condition. PF can reach beyond 0.9 and THD can achieve less than 7% for universal line.

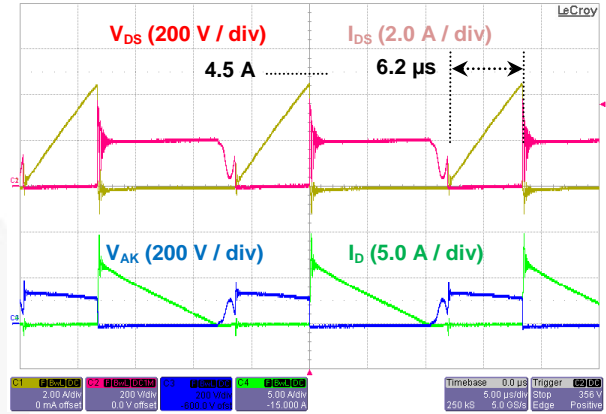


Figure 13. Operation Waveforms at Minimum Line Voltage Condition

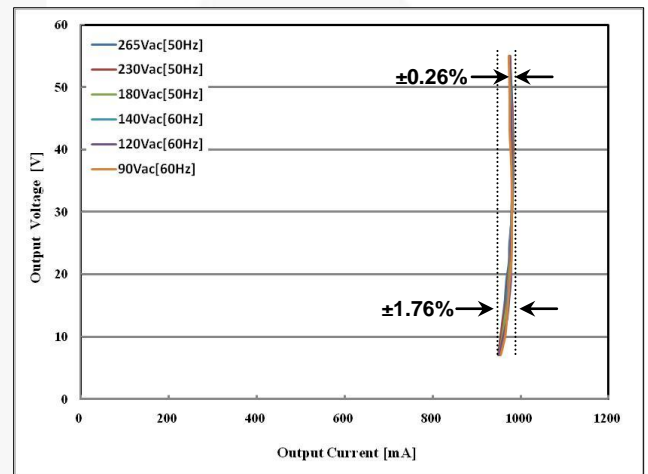


Figure 14. CC Tolerance

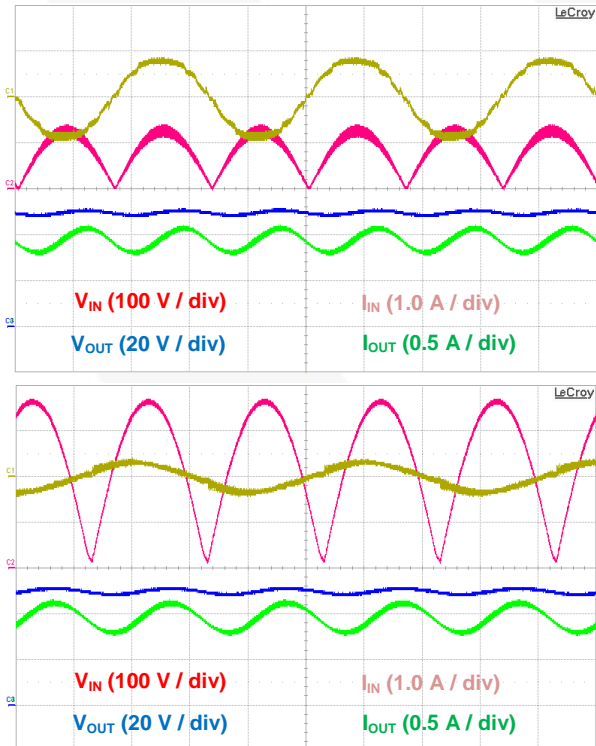


Figure 12. Input and Output Waveforms

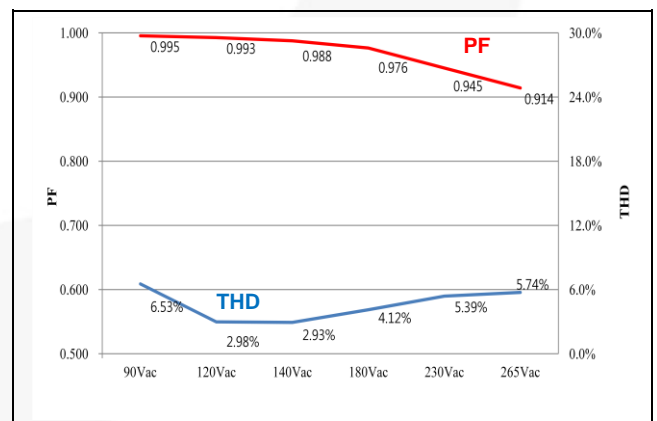


Figure 15. PF and THD

## Related Product Resources

[FL7733A — Primary-Side-Regulated LED Driver with Power Factor Correction](#)

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