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AN-5055

Fairchild Semiconductor
Application Note
October 2004
Revised October 2004

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Portability and Ultra Low Power TinyLogic®

Abstract

With the advent of Fairchild Semiconductor's ULP (Ultra Low Power) TinyLogic family, a new level of low power performance is possible for designs requiring optimal portability. The ULP family offers up to 50% less power consumption compared to other low voltage logic families. ULP provides significant power reduction through innovative design and process techniques and helps meet the portable market demand for extended battery charge duration and life cycle. Popular portable applications that can benefit from ULP include mobile phones, notebooks, PDAs, digital cameras, and all other battery-based systems.

The information in this application note will focus on the power savings available when using the ULP family. It will also offer insight to device performance, system analysis, and design comparison, however, emphasis will center on power dissipation with respect to the portable system.

The Power Calculations

In order to review and compare power dissipation in logic devices, an overview of the formulas required to calculate power consumption is presented below. After reviewing the elements of power, example calculations are used to illustrate power dissipation in the application.

The power consumed by a logic device is derived using the published datasheet specifications along with the external parameters. There are two basic elements of power that must be considered. They are static and dynamic, or DC and AC in nature. Summation of these elements yields total power consumed by the device. In addition, the package thermal resistance characteristic should be used in conjunction with the device power dissipation in order to assure the temperature of the device does not exceed the absolute maximum junction temperature.

The following information on power consumption is devoted to CMOS technology. CMOS is the technology of choice in today's low power applications. This is because during the quiescent or static condition, CMOS devices consume considerably less current than bipolar. CMOS input impedances are typically more than 10^{12} Ohms, minimizing input current consumption. For CMOS applications, static power is a very small portion of total power, however, during system operation switching requires charging and discharging of internal and external capacitance. This toggling of the device, i.e., introduction of a frequency component, constitutes dynamic power.

Quiescent Power

There are 3 basic formulas used in calculating the accumulated power dissipation of the device. First, quiescent or static power is determined by the fundamental DC power equation: P = I * E. This formula uses basic datasheet DC electrical parameters I_{DD} and V_{DD} as follows:

Equation 1: Quiescent or Static Power

$P = I * E$ or $P_{DQ} = I_{DD} * V_{DD}$

Where,

P_{DQ} = Quiescent Power Dissipation

I_{DD} = Device static current taken from the datasheet

V_{DD} = Voltage applied to the device power terminals

In many CMOS datasheets, I_{DD}, ΔI_{DD}, and V_{DD} are referred to as I_{CC}, ΔI_{CC}, I_{CCT}, I_{CCQ}, I_{DDQ}, and V_{CC}. I_{CCT} is a parameter relating the current taken when CMOS inputs are conditioned with TTL input levels. This additional current occurs when input stages are partially biased ON. I_{CCT} is not considered when rail amplitude signals are applied to inputs. CMOS inputs should be conditioned to a potential equal to one rail or the other - V_{DD} or Ground. This is the case with most low voltage CMOS technologies and includes ULP TinyLogic products.

Internal Dynamic Power

The next equation reflects internal dynamic power with respect to the internal gate capacitance (C_{PD}) inherent to all CMOS logic devices. All CMOS logic devices dissipate power when internal node capacitance is dynamically switched from one state to another. As these small internal nodes are charged and discharged power is consumed. the C_{PD} parameter listed on the datasheet is the sum of these internal node capacitances innate to a particular design.

The C_{PD} parameter for CMOS logic devices is typically published in the datasheet. For some logic functions C_{PD} is stated for the entire device. For others, it is listed for a single bit only. A JEDEC standard test methodology has been adopted that specifies the test setup for the various logic functions. The standard describes how C_{PD} should be tested for each function.

As mentioned earlier, the C_{PD} parameter is dependent on functionality of the device. For instance, a counter will switch more internal stages for a given single input signal, i.e., a clock signal, than will a simple gate function. Please refer to Appendix A for more information regarding JEDEC C_{PD} test methodology. Following are a few examples of how C_{PD} is tested per device functionality according to JEDEC test methodology:

Internal Dynamic Power (Continued)

Gates	Switch one input and bias the remaining inputs such that one output switches
Flip-Flops	Switch the clock pin while changing data such that the output(s) change
Counters	Switch the clock with other inputs biased such that the device counts

Equation 2 relates internal dynamic power dissipation with respect to the applied device switching frequency and associated C_{PD}. The functional C_{PD} difference is accounted for in Equation 2 per the JEDEC standard test methodology.

Equation 2: Internal Dynamic Power

$$P_{DINT} = (C_{PD} * V_S * F)\ V_{DD}$$

Where,

P_{DINT} = Internal Power Dissipation

C_{PD} = Internal Device Power Dissipation Capacitance

V_S = Internal Voltage Swing

F = Switching Frequency

V_{DD} = Voltage applied to the Device Power Rail

Please note, the quantity $C_{PD} * V_S * F$ is directly proportional to dynamic switching current (I_{DD}) in Equation 1. It can be seen from the formula that the C_{PD} figure inherent to the logic function has considerable influence on the internal dynamic power dissipation. The ULP family of functions capitalizes on this parameter and reduces C_{PD} to levels well below those of competing technologies through innovative design and process optimization.

External Dynamic Power

Equation 3 is an expression for dynamic power with respect to the external capacitive loading that must be charged and discharged under AC conditions. The formula is identical to Equation 2 except the capacitance is external to the device. C_{EXT} represents the total external capacitance the device must switch including board trace, other device inputs, and to a lesser extent, the package interlead parasitic.

Equation 3: External Dynamic Power

$$P_{DEXT} = (C_{EXT} * V_S * F)\ V_{DD}$$

Where,

P_{DEXT} = External Capacitive Load Power Dissipation

C_{EXT} = Aggregate External Capacitance Presented at the Device Output

V_S = The Output Voltage Swing Amplitude

F = The Output Switching Frequency

V_{DD} = The Voltage Applied to the Power Rails

The number of outputs switching is in aggregate and must be factored into the formula, i.e., if there are 8 outputs switching the right side of the equation must be multiplied by 8. For instance, for an 8-bit buffer device with all outputs switching, the equation would appear as $P_{DEXT} = ((C_{EXT} * V_S * F)\ V_{DD}) * 8$. This works only if all outputs are loaded equally and are switching at the same frequency. If outputs are not equally loaded and frequencies differ then the equation must be utilized separately for each output and then combined to arrive at the total power dissipation.

Finally, the results of each of the three equations can be combined to reveal the total power the device will dissipate in the application. With all 3 elements combined, Equation 4 is derived. In this equation, $V_S * V_{DD}$ is written as V_{DD}^2 because CMOS technology output voltage swings are from rail-to-rail. Similarly, internal and external capacitances can be combined.

Equation 4: Total Power Dissipation

$$\mathbf{P_{TOTAL}} = \mathbf{P_{QD}} + \mathbf{P_{INT}} + \mathbf{P_{EXT}}$$

$$= ((C_{PD} + C_{EXT}) * V_{DD}^2 * F)) + (I_{DD} * V_{DD})$$

Example Calculations

To demonstrate the power equations and the ULP power advantage, an example based on two identical TinyLogic functions is presented.

UHS NC7SZ125 Switching at 20MHz into 15pF Loading

Datasheet specifications:

V_{DD} = 3.3V; I_{DD} = 20uA; C_{PD} = 17pF

Using Equation 4:

P_{TOTAL} = $((C_{PD} + C_{EXT}) * V_{DD}^2 * F)) + (V_{DD} * I_{DD})$

= ((17pF + 15pF) * 10.89V * 20MHz)) + (3.3V * 20uA)

= (32pF * 10.89V * 20MHz) + 66uW

= 6.97mW + 66Uw

P_{TOTAL} = 7.036mW

ULP NC7SV125 Switching at 20MHz into 15pF Loading

Datasheet specifications:

V_{DD}: 3.3V; I_{DD}: 0.9uA; C_{PD}: 10pF

Using Equation 4:

P_{TOTAL} = $((C_{PD} + C_{EXT}) * V_{DD}^2 * F)) + (V_{DD} * I_{DD})$

= ((10pF + 15pF) * 10.89V * 20MHz)) + (3.3 * 0.9uA)

= (25pF * 10.89 * 20MHz) + 2.97uW

= 5.445mW + 2.97uW

P_{TOTAL} = 5.448mW

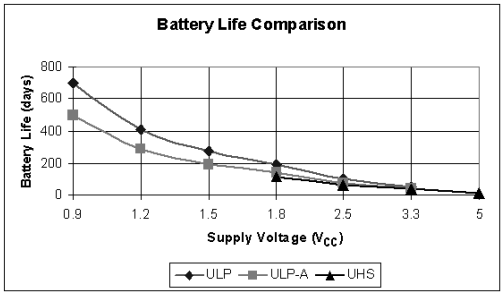
The example illustrates a 23% reduction in power based on an identical single-gate function in two families, UHS and ULP. The significant reduction in power is directly attributable to the smaller C_{PD} parameter and less standby current intrinsic to the ULP device.

Reducing Power in the Portable Application

As more functionality is packed into portable applications, the availability of lower power semiconductor technologies becomes increasingly important. ULP is the next level in a generation of low power, high-speed single-gate products. The graphic below is useful in making comparison to other single-gate logic families. Not only are lower battery terminal voltages possible, battery charge and life cycle can be extended with ULP.

A prevalent application can be used to illustrate how ULP TinyLogic lowers power in the portable design. The mobile phone may incorporate a number of single-gate functions into the design to perform logical operations. Commonly found solutions are the following:

1. Buffering weak or distorted signals
2. Dividing a clock signal by 2
3. Synchronizing data with a clock signal
4. Providing a gating function for scan-path testing
5. Convenient inversion of an enable signal



Power in a Cell Phone Application

Cell phones are comprised of four functional sections. Single-gates typically fit in the digital section along with DSP and ASIC functions. In standby mode, the digital section may consume as much as 10% of the overall power of a cell phone. A reduction in standby current can be key to improving efficiency in the phone design. The significantly reduced quiescent power of ULP directly addresses this concern.

Logic in the cell phone can consume as much as 33% of the digital section's power budget. By comparison, ULP consumes approximately 11% of the Digital Section's power. This is a reduction in power of 66%.

The cell phone application used in the analysis includes six single-gate devices. Devices and quantities found in the phone are 2-NC7S04, 2-NC7SZ04, and 2-NC7SZ08 for a total of six TinyLogic devices. In the application, these devices drive small capacitive loads consisting of short circuit traces typically 1 inch or less (~5pF) plus the capacitance of a single CMOS input equal to 5pF. The combination of these parameters yields a load of approximately 10pF. The frequency of operation of a cell phone is typically less than or equal to 10MHz in the digital section. These figures are used to analyze the digital power consumed and compare ULP to standard single-gate logic.

The following power analysis compares power dissipation using ULP to equivalent HS and UHS TinyLogic devices in a cell phone application. Functions found in the design:

HS/UHS	ULP Equivalent
NC7S04	NC7SP04
NC7SZ04	NC7SV04
NC7SZ08	NC7SV08

Parameters used for power analysis:

V_{CC}: 3.3V

Capacitive Load: 10pF

Frequency: 10MHz

Datasheet parameters used in the Power Calculations:

Device	C_{PD}	I_{DDQ} Maximum
NC7S04	6pF	10uA
NC7SZ04	20pF	20uA
NC7SZ08	20pF	20uA
NC7SP04	8pF	0.9uA
NC7SV04	10pF	0.9uA
NC7SV08	8pF	0.9uA

Equation 4, total power used by the TinyLogic HS/UHS devices in the cell phone:

$$P_{TOT} = ((C_{PD} + C_{EXT}) * V_{DD}^2 * F)) + (I_{CCQ} * V_{DD})$$

NC7S04

P_{TOT} = ((6pF + 10pF) * 10.89V * 10MHz)) + (10uA * 3.3V)

= 1.78mW * 2 = 3.56mW

NC7SZ04

P_{TOT} = ((20pF + 10pF) * 10.89V * 10MHz)) + (20uA * 3.3V)

= 3.33mW * 2 = 6.66mW

NC7SZ08

P_{TOT} = ((20pF + 10pF) * 10.89V * 10MHz)) + (20uA * 3.3V)

= 3.33mW * 2 = 6.66mW

Total HS/UHS TinyLogic Power

= 3.56mW + 6.66mW + 6.66mW

= 16.88mW

Power in a Cell Phone Application (Continued)

Total power used if replaced with identical function TinyLogic ULP devices:

NC7SP04

P_{TOT} = ((8pF + 10pF) * 10.89V * 10MHz)) + (0.9uA * 3.3V)

= 1.96mW * 2 = 3.92mW

NC7SV04

P_{TOT} = ((10pF + 10pF) * 10.89V * 10MHz)) + (0.9uA * 3.3V)

= 2.18mW * 2 = 4.36mW

NC7SV08

P_{TOT} = ((10pF + 10pF) * 10.89V * 10MHz)) + (0.9uA * 3.3V)

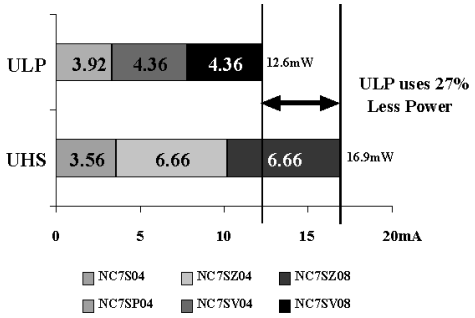
= 2.18mW * 2 = 4.36mW

Total ULP TinyLogic Power

= 3.92mW + 4.36mW + 4.36mW

= 12.64mW

The analysis indicates that under identical conditions, ULP TinyLogic dissipates over 27% less power in the application compared to HS and UHS TinyLogic technologies.



Total Power Consumption Comparison

Summary

Although the number of single-gate logic devices contained in the typical cell phone represents a small portion of the total power, the opportunity to reduce power at any stage is imperative to battery longevity. As greater functionality is packed into the handheld, power consumption problems continue to loom. Another issue is how to bundle more features into portable applications without increasing battery size and printed circuit board size. ULP TinyLogic provides a method of reducing battery current consumption. In addition, Fairchild's TinyLogic advanced small footprint packaging, MicroPak™, significantly reduces the necessary board space.

Please refer to our website for additional information regarding TinyLogic packaging options at http://www.fairchildsemi.com/products/logic/micropak/index.html.

Appendix A

C_{PD} Test Methodology

In an effort to reduce confusion about measuring Power Dissipation Capacitance, C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device function. This allows a device to be exercised in a consistent manner for the purpose of specifications comparison.

The following is a list of different types of logic functions along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements, the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation capacitance for the entire device or for just a certain stage of the device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device since the entire device is exercised during the measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages since only one input was switched during the test. Therefore, the overall power dissipation for the octal should be calculated for each of the eight stages individually. All output pins are unloaded or left to float.

The following list succinctly describes how each category of logic is to be tested for C_{PD}:

Gates, Buffers, and Line Drivers: Switch one input. Bias the remaining inputs such that one output switches.

Latches: Switch the Enable and D inputs such that the latch toggles.

Flip-Flops: Switch the clock pin while changing D or bias J and K such that the output(s) change each clock cycle. For devices with a common clock, exercise only one flip-flop.

Decoders: Switch one address pin, which changes tow outputs.

Multiplexers: Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.

Counters: Switch the clock pin with other inputs biased such that the device counts.

Shift Registers: Switch the clock pin with other inputs biased such that the device shifts.

Transceivers: Switch one data input. For bidirectional devices, enable only one direction.

Parity Generators: Switch one input.

Priority Encoders: Switch the lowest priority input.

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