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Live Insertion Using Low Voltage Differential Signaling

Abstract

Supporting live insertion or hot swapping is important in certain applications such as the ones used in telecommunications systems. These applications require maintenance, upgrades, and repairs to be conducted without shutting down the system or causing disruptions to traffic on the backplane. Inserting and removing cards on a backplane is a capability often required for maximizing system uptime. This paper will discuss how Low Voltage Differential Signaling (LVDS) technology supports live insertion for multi-drop applications and hardware considerations to minimize the effects inserted cards have on a backplane.

LVDS in Multi-Drop Configuration

Multi-drop configurations, which connect multiple receivers to a single driver, are possible with LVDS provided the transmission distance is short and stub lengths are kept as short as possible to preserve signal integrity. This configuration may be useful in data and clock distribution applications. A single termination resistor (matching the characteristic impedance) at the receiver inputs furthest away from the driver is all that is needed for achieving signal integrity.

Power-Off High Impedance Bus Pins

Fairchild's LVDS drivers and receivers incorporate high impedance bus pins, which limit the power-off input current (I_{OFF} and I_{IOFF}) to a maximum of ±20µA. This feature is useful in applications that employ more than one receiver, which are powered from local power supplies. If the power is turned off to a receiver card, inputs (I_{IOFF}) will be in high impedance and not load down the line. With the driver powered off and receiver on, driver outputs will be high impedance and LVDS receiver outputs will lock in a high state failsafe condition to avoid oscillation.

In point-to-point applications which is ideal for LVDS, with the driver powered down and receiver active, communication will cease and the receiver will go into a failsafe condition. With the driver active and receiver powered down, the high impedance bus pins will prevent any damage by limiting the current and not cause a latch-up condition on the receiver inputs.

To determine if a device supports power-off high impedance bus pins refer to the features list in the device datasheet and the receiver power-off input, I_{IOFF} and the driver power-off output current parameter, I_{OFF}.

Live Insertion Test Set-Up

To evaluate and demonstrate live insertion capability of LVDS, lab testing done in Fairchild's EnSigna Lab has shown zero errors while plugging in cards to an active bus. A system card which had Fairchild's FIN1111 clock driver connecting to two load cards each having Fairchild's FIN1018 LVDS receivers on a backplane with a differential pair was used. The R+/R– of one load card was monitored, which had the termination resistor and the second load card was inserted. LVDS will not work without the terminating resistor, which is placed on the card rather than the backplane for optimum signal integrity. Figure 1 illustrates the multi-drop configuration used for the live insertion performance plot.

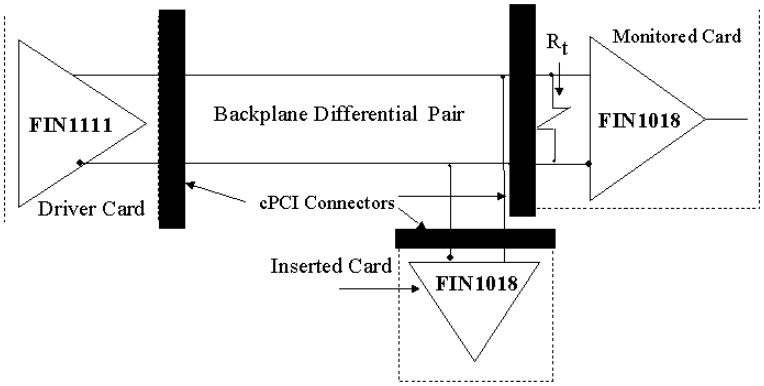

FIGURE 1. Multi-Drop Configuration for Live Insertion Testing

Live Insertion Test Set-Up (Continued)

Screen capture of following channels included:

CH1: R+ Input of monitored card

CH2: R– Input of monitored card

CH3: TTL output of the monitored card

CH4: R+ of the inserted card

F3 : Math waveform (CH1 - CH2), Vdiff

FIGURE 2. Live Insertion Performance Plot

The results shown in Figure 2 illustrate effective isolation during a live insertion event. The highlighted portion of the differential (Vdiff) signal shows a distortion at the point the card is inserted. The disturbance is minimal resulting in noise margin of ~350mV from the zero crossing pint of the differential signal. Channel 3 is the TTL output of the monitored card which is not impacted by the insertion of a second card and data is asserted once the inserted card gets powered up.

Hardware Considerations

Upon insertion of a card into a live backplane, assuming the occurrence of abnormalities on the signals is common on both signals, data should not be impacted. This is due to the fact that the deferential lines equally load the active line once asserted and any glitch seen as a common-mode modulation will be ignored by LVDS receivers.

Pin staggering within the card connector should be adopted as well for proper biasing of the devices and establish the highest level of isolation during live insertion. Asserting the ground, data and V_{CC} pins in the following sequence should be implemented with the power pin being the shortest pin and the data pins being the next shorter pins:

Space for diagram?

1. Ground Pin: Discharge path for any built up charge on the card.
2. I/O Data Pins: With no power the pins are high impedance, minimizing loading in the live bus.
3. V_{CC} Pins: Last pin to assert for highest level of isolation.

Summary

In multi-drop applications, maintaining operation during the removal and insertion of cards is a requirement to minimize system downtime. LVDS devices that support power-off high impedance features should be considered for the system design. This feature will insure error free operation of the bus even when one or more receiver cards are not powered. The performance plot in Figure 2 illustrates no data disruptions or errors on the bus during a live insertion of a card. Along with the power-off high impedance feature of LVDS drivers and receivers, pin staggering on the edge connector of the card should be adopted for the highest level of isolation during live insertion events.

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