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LVDS Receiver Failsafe Biasing Networks

Abstract

Failsafe biasing of an LVDS data line receiver establishes a know state under certain fault conditions. Typically these devices are designed with integrated failsafe biasing resistors. This paper will discuss how to add additional external failsafe biasing resistor networks to increase noise immunity in a system and improve the reliability of failsafe operation within a specific application. An application example will be discussed and calculations for resistor values will also be provided.

External "Assist" Failsafe Resistors

Certain applications (especially noisy environments) may warrant the need for additional failsafe protection. Adding external failsafe resistors may be justified to create a larger noise margin beyond what is provided by the receiver. Selecting external failsafe resistors can be done to protect against differential noise and have minimal impact on the signal integrity of the LVDS signal. Additional failsafe current will tend to "unbalance" the symmetry of the LVDS signal which should not be an issue at low data rates, however could be aggravated at higher data rates.

What Resistor Values Should Be Used?

For Fairchild LVDS receivers designed with an internal failsafe bias, they typically will have an internal bias voltage of ≅ 20 to 35mV (Figure 1). In a cable application where the receiver will not always be driven by the transmitter and there is a potential for the presence of more than 20mV of differential noise on the receiver inputs, additional failsafe resistors should be considered. The resistor values should be specified to overcome the differential noise and have minimal impact on the driver current. Figure 1 illustrates a typical differential input voltage verses the logic output state of the receiver.

The amount of differential noise anticipated should be measured and resistor values chosen to overcome this noise. The VFSB is the offset voltage is generated across the R^t resistor and the external resistor values should be enough to overcome the differential noise. Making VFSB too large will counter with the driver loop current impacting the signal integrity of the signal. Note using shielded cable can reduce differential noise.

Once the amount of differential noise at the receiver input has been determined (under worse case conditions), the following formulas are provided to assist the designer in calculating the resistor values.

$V_{FSB} = R_{pu} / (R_{pu} + R_t + R_{pd}) * V_{CC}$

$I_{FSB} = V_{CC} / (R_{pu} + R_t + R_{pd})$
$(I_{FSB} < 0.1 * I_{LOOP})$

$V_{CM} = (R_{up} + R_t/2) / (R_{pu} + R_t + R_{pd}) * V_{CC}$
(Ideal $V_{CM} \cong 1.2V$)

$R_t = (R_t * (R_{pu} + R_{pd})) / (R_{pu} + R_t + R_{pd})$
(match R_t to Z_{ODIFF})

The external failsafe "Assist" resistors may change the termination resistance, thus adjust the R_t value to match within 10% of the characteristic impedance of the transmission line.

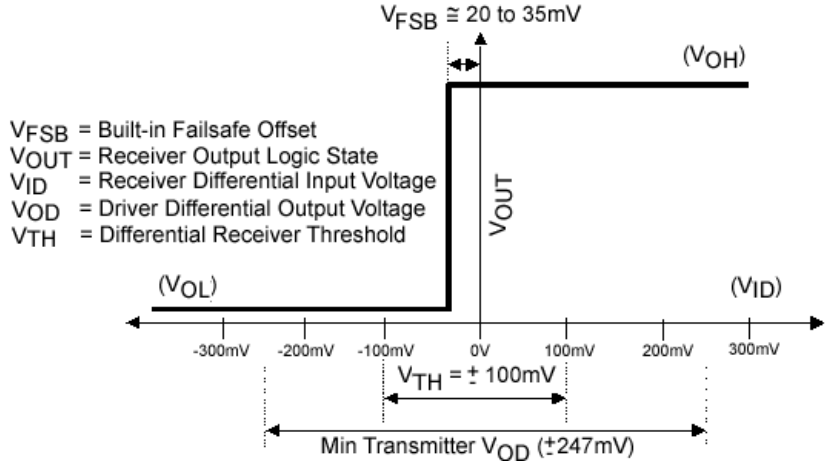


FIGURE 1. Differential Input Voltage verses Receiver Output Voltage

What Resistor Values Should Be Used? (Continued)

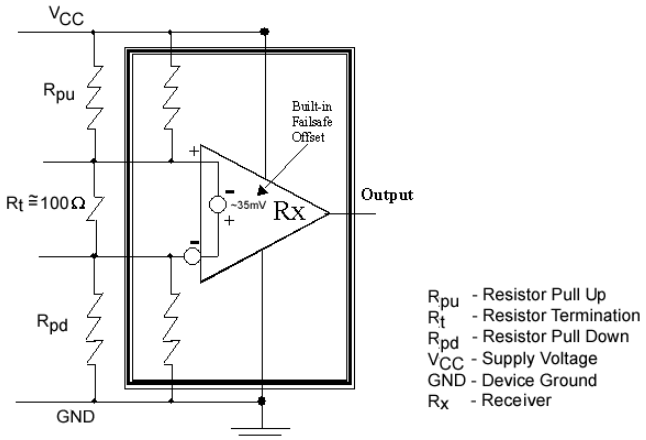


FIGURE 2. Simplified Schematic of Internal Failsafe Circuitry with External "Assist" Failsafe Resistors

Point-to-Point Application Example

System problems can impact proper "Failsafe" operation with LVDS receivers in an application involving communication between equipment racks within the same cabinet typically found in telecom equipment. Potentially receiver outputs will not assert "failsafe" (Logic High) under specific failsafe conditions within a system environment due to the presence of system noise or other circuitry (such as ESD protection diodes) which could impede the effectiveness of the integrated failsafe feature.

Failsafe circuitry internal to the receiver is designed to source/sink a small amount of current, providing failsafe protection for floating receiver inputs, shorted inputs and terminated inputs. However, an application environment and certain conditions potentially create differential noise that causes the receiver to oscillate and not maintain a known failsafe state. External failsafe resistors may be needed to increase or improve noise margins to insure reliable failsafe operation under all fault conditions. Refer to Figure 3 as an example of an external failsafe bias resistor network.

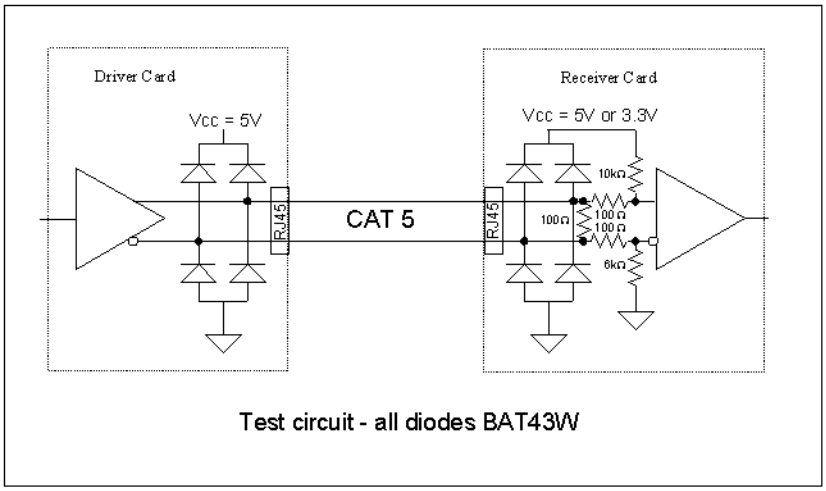


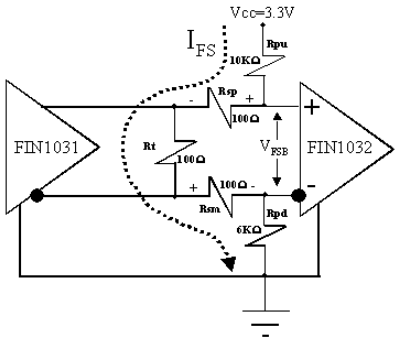
FIGURE 3. Point-to-Point Circuit Application with External Failsafe Resistors and ESD Protection Diodes

Worse Case Failsafe Conditions

1. Reviewing the circuit in Figure 1, with the driver card powered down (V_{CC} = 0V), the ESD protection diode network on the driver card is forward biased. This results in a clamping action of the diodes providing an alternate current path reducing the offset voltage created across the termination. The diodes forward bias causing an approximate worst case clamping of the line at ≅ 0.3V with respect to ground.
2. Series resistors R_{sp} and R_{sm} work to counter the effects of the clamping action of the diodes providing additional failsafe bias voltage enabling the receiver to assert a logic high on the output.
3. The suggested resistor network should provide reliable failsafe operation and improved differential noise immunity during a failsafe event.
4. The additional resistor network has been confirmed to have no impact on the signal integrity in our lab setup.

For certain cable point-to-point applications where data rates are in the low MHz range, additional failsafe protection may be needed to improve noise margins and increase the reliability of failsafe operation. The following section discusses and illustrates resistor networks that could be considered for additional failsafe bias resistors yielding increased noise margins.

Suggested Failsafe Resistor Values for FIN1032



R_{pu}	Resistor Pull Up
R_{sp}	Resistor Series Plus
R_t	Resistor Termination
R_{sm}	Resistor Series Minus
R_{pd}	Resistor Pull Down
I_{FS}	Failsafe Bias Current
V_{FSB}	Failsafe Bias Voltage
V_{CM}	Common Mode Voltage

FIN1032 F/S Bias Voltage and Current Calculations

With R_{sp} & R_{sm} Resistors

$I_{FS} \cong 3.3V/16.3K\Omega = 0.202mA$

$V_{CM} \cong 0.2mA*6.15K\Omega \cong 1.23V$

$V_{FSB} \cong I_{FS}*300\Omega \cong 60mV$

Without R_{sp} & R_{sm} Resistors

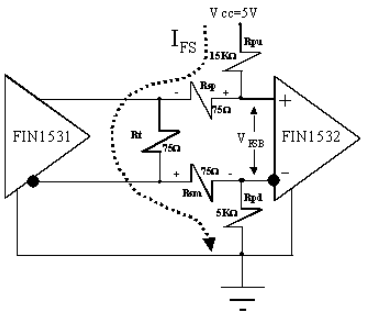
$I_{FS} \cong 3.3V/16.2K\Omega = 0.205mA$

$V_{CM} \cong 0.205mA*6.05K\Omega \cong 1.24V$

$V_{FSB} \cong I_{FS}*100\Omega \cong 21mV$

Note: An additional failsafe bias voltage of ≅40mV can be attained with the series resistors.

Suggested Failsafe Resistor Values for FIN1532



R_{pu}	Resistor Pull Up
R_{sp}	Resistor Series Plus
R_t	Resistor Termination
R_{sm}	Resistor Series Minus
R_{pd}	Resistor Pull Down
I_{FS}	Failsafe Bias Current
V_{FSB}	Failsafe Bias Voltage
V_{CM}	Common Mode Voltage

FIN1532 F/S Bias Voltage and Current Calculations

With R_{sp} & R_{sm} Resistors

$I_{FS} \cong 5V/20.25K\Omega = 0.25mA$

$V_{CM} \cong 0.25mA*5.125K\Omega \cong 1.26V$

$V_{FSB} \cong I_{FS}*250\Omega \cong 62mV$

Without R_{sp} & R_{sm} Resistors

$I_{FS} \cong 5V/20.1K\Omega = 0.249mA$

$V_{CM} \cong 0.249mA*5.050K\Omega \cong 1.26V$

$V_{FSB} \cong I_{FS}*100\Omega \cong 25mV$

Note: An additional failsafe bias voltage of ≅40mV can be attained with the series resistors.

Summary and Conclusions

LVDS translators are supplied with internal failsafe bias protection. Depending on the system noise environment, it may be necessary to implement an external FS bias resistor network to insure reliable failsafe operation. Other circuitry in a system such as ESD protection networks may impede or counter the effectiveness of the integrated receiver failsafe bias circuit. This paper provided an example of a system that had ESD diode networks employed on the driver and receiver cards. The specific application environment and failsafe requirements will ultimately dictate the optimum failsafe solution.

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