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AN-5029

Fairchild Semiconductor
Application Note
August 2002
Revised August 2002

Interfacing Between PECL and LVDS Differential Technologies

Introduction

Over the past several years, growth in the demand for high-speed data transmission has spawned dramatic changes and innovations in high-speed ICs. Achieving these increased levels of high performance, lower power and improved noise immunity involves optimizing the interface between ICs. Often times a more cost effective solution requires interfacing between ICs with different I/O voltage levels and technology requirements. System designers must familiarize themselves with the different I/O circuit configurations to understand the requirements for proper biasing and effective termination necessary to maintain good signal integrity between differing technologies. This application note will describe an approach to interfacing Positive Emitter Coupled Logic (PECL) with Low Voltage Differential Signaling (LVDS) technologies.

What is PECL?

Emitter Coupled Logic (ECL) is an ultra-high speed digital logic technology and is based on a differential amplifier. Small signal swings prevent saturation during switching and increase operating frequency performance. The input and output voltage levels are referenced directly to V_{CC}/V_{CCA} pins which are normally zero volts or ground potential operating with a negative V_{EE} and negative termination V_{TT} supplies. With PECL operation the V_{CC}/V_{CCA} pins are offset to the positive +5V nominal potential, V_{TT} is offset by +5V from −2V to +3V and the V_{EE} pin becomes 0V or ground potential. Refer to the schematic representation of the PECL operation and the associated voltage levels in Figure 1.

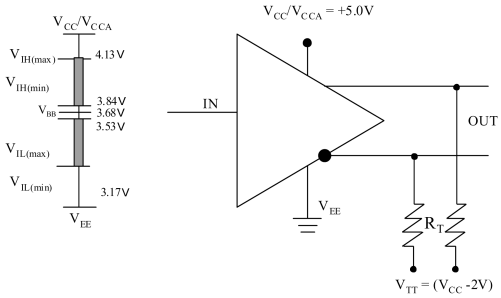


FIGURE 1. ECL Device Configured for PECL Operation

What is LVDS?

LVDS technology is defined by the ANSI/TIA/EIA-644 industry standard. LVDS is targeted for general purpose high speed applications requiring very low noise and minimal power consumption. Using a constant current source driver allows power consumption to be relatively independent of frequency resulting in greater performance. LVDS drivers have a very low differential swing of typically 350 mV, which is centered on an offset voltage of 1.2V above circuit common (ground). With lower signal swings, higher data rates can be achieved as it takes less time to transition between logic states. Noise concerns are reduced with differential signaling techniques as noise is coupled onto both conductors with equal magnitude and phase and is rejected by the receiver, which senses the difference between the two signals.

TABLE 1. Signal Voltage Comparisons

DC Parameter	5V PECL	LVPECL	LVDS
Power Supply, V_{CC}	+5.0V	3.3V	3.3V
Output HIGH, V_{OH}	4.0V	2.4V	1.4V
Output LOW, V_{OL}	3.3V	1.7V	1.0V
Differential Output, V_{OD}	595 to 960 mV	595 to 930 mV	247 to 454 mV
Common Mode Voltage, V_{OS}	3.65V	2.1V	1.2V

5V PECL to 5V LVDS Interface

For a PECL driver, each emitter follower output is properly terminated with a 50Ω resistor to a termination voltage of $V_{TT} = V_{CC} - 2V$. Although this termination technique will consume significantly less power, an additional supply for the termination voltage may be undesirable for the system. The LVDS receiver should have a sufficiently wide common mode range to respond to the output signals from the PECL driver. Figure 2 shows how the interface can be configured using a split resistor termination with a V_{TT} of (V_{CC} – 2V). This configuration consists of a +5V PECL device driving a 5V LVDS receiver. The configuration is possible providing the receiver has a wide common mode range that accommodates the worst case PECL output levels and compliance to all device datasheet specifications is met. To ensure proper operation of the PECL device within the system the tolerances of the V_{TT} and V_{CC} supplies should be considered. Refer to waveforms in Figure 3, illustrating the PECL to LVDS interface operation. Although the configuration conserves power and keeps component count low, an additional power supply is required.

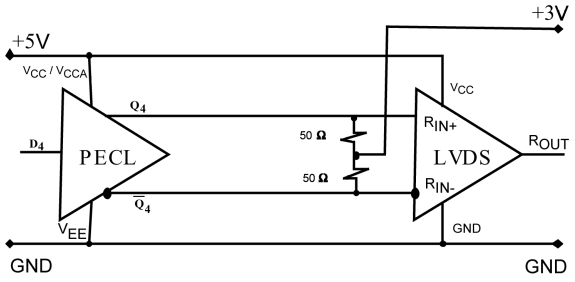


FIGURE 2. PECL to 5V LVDS Interface

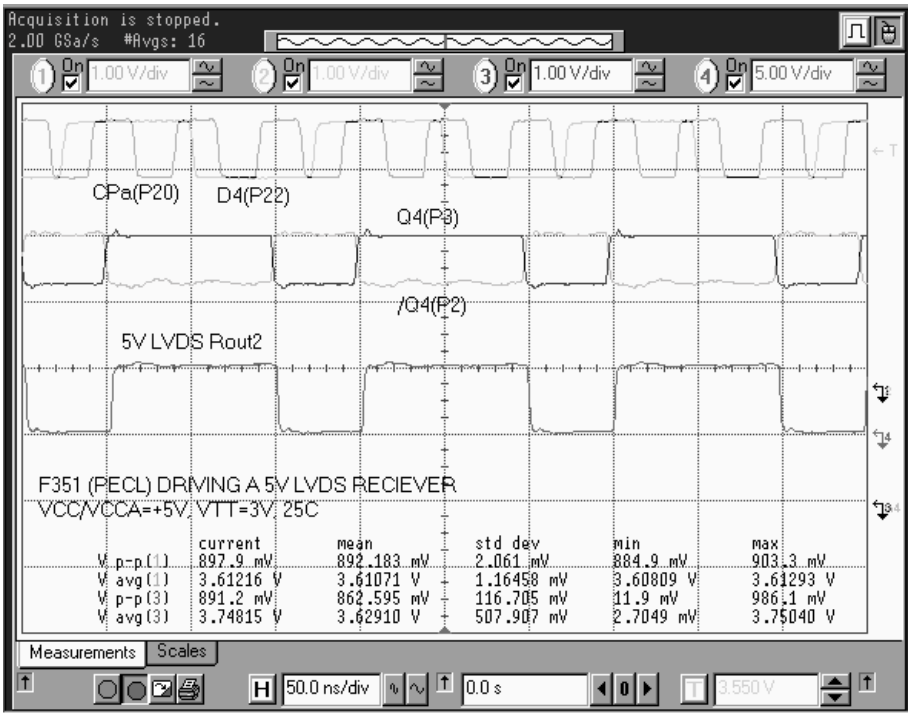


FIGURE 3. PECL to 5V LVDS Interface

LVPECL to 3V LVDS Interface

A similar bench set up was evaluated using an LVPECL driver with a 1-meter CAT5 Unshielded Twisted Pair (UTP) cable as a 100Ω characteristic impedance transmission media driving a Fairchild FIN1018 LVDS receiver. Although power consumption is significantly less, the parallel termination scheme requires an extra V_{TT} power supply for the impedance matching load resistor. Depending on the system this extra power supply requirement may prohibit use of this technique. As the number of PECL devices incorporated in the design increases the more attractive the V_{TT} termination scheme becomes. Typically, trade-offs between the performance requirements and system costs will dictate which approach the designer will use. The parallel termination technique using an extra V_{TT} power supply is shown in Figure 4. Refer to the Figure 5 for waveforms of the LVPECL to LVDS interconnect. This configuration conserves power and keeps component count low, however requires an additional supply voltage.

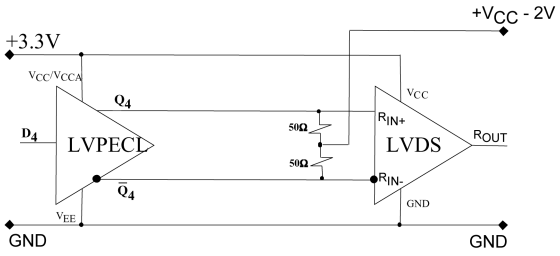
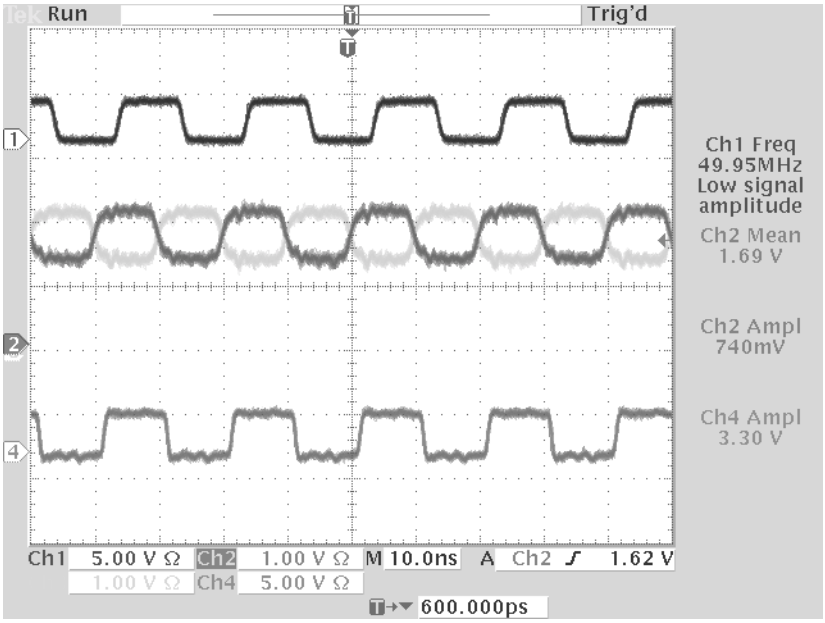


FIGURE 4. LVPECL to 3V LVDS Interface



Note: Channel 1: LVTTL Input

Channel 2 and 3: Single Ended LVPECL Outputs

Channel 4: LVTTL Output from LVDS Receiver

FIGURE 5. LVPECL to 3V LVDS Interface

Thevenin Equivalent Termination Scheme

As previously mentioned, since an LVPECL output is designed to drive a 50Ω load connected to a V_{TT} of (V_{CC} – 2V), using a termination supply voltage may not be available in the system application. An alternative approach involves using a Thevenin equivalent parallel combination of resistors which is equal to the transmission line impedance and shifts the PECL driver signals to be in the common mode input range of the LVDS receiver using a single supply voltage. This technique will consume more termination power, however the absence of an additional power supply will more than compensate for the extra power consumption. This extra power is consumed entirely in the external resistor network and will not change the current being sourced by the device, hence will not alter the reliability of the IC.

To explore this approach we will use an LVPECL driver interfacing to a 3V LVDS receiver. A parallel Thevenin termination network as shown in Figure 6 will provide a resistor divider network to generate the proper DC levels for the LVDS receiver. The resistor network ensures the LVPECL outputs are terminated for a 50Ω load to (V_{CC} - 2V) and will attenuate the LVEPCL output signals to within the input range of the LVDS receiver. While this technique increases the component count and dissipates more termination power, the additional V_{TT} supply is not required.

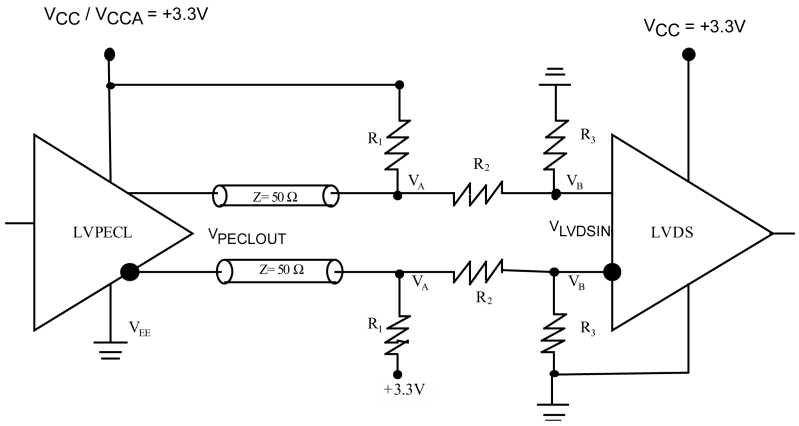


FIGURE 6. LVPECL to LVDS Interface Using a Thevenin Equivalent Termination Scheme

Thevenin Equivalent Termination Scheme (Continued)

The characteristic line impedance is approximately 50Ω for each of the single ended lines, therefore the parallel combination of R_1 || (R_2 + R_3) must provide the correct R_T of 50Ω. To illustrate the attenuation resistor network the following equations will be used in the example:

Equation 1: $V_A = R_1/(R_1 + R_2 + R_3) = 2/V_{CC}$

Equation 2: $V_B = R_3/(R_1 + R_2 + R_3) = V_{IL}/V_{CC}$

Equation 3: $V_{LVDSIN} = R_3/(R_2 + R_3) * V_{PECLOUT}$

Example:

Assume the following differential voltage levels

V_{LVDSIN} = 350 mV (typical)

$V_{PECLOUT}$ = 700 mV (typical)

V_{CC} = 3.3V

Using Equation 3:

Ratio of V_{LVDSIN}/ $V_{PECLOUT}$ is 350 mV/700 mV = $R_3/(R_2 + R_3)$, since it's a 1:2 relationship then $R_2 = R_3$

R_1 || (R_2 + R_3) = 50Ω and since $R_2 = R_3$, replacing R_3 with R_2 this equation becomes R_1 || (2*R_2) = 50Ω

$V_A = R_1/(R_1 + R_2 + R_3) = 2/V_{CC}$

$= R_1/(R_1 + R_2 + R_3) = 2/3.3V$ $\quad V_{CC} = 3.3V$

$= R_1/(R_1 + 2R_2) = 0.61V$ $\quad R_3 = R_2$

Solve for R_1:

$R_1 = 0.61R_1 + 1.22R_2$

$(1 - 0.61)R_1 = 1.22R_2$

$$R_1 = \frac{1.22R_2}{0.39}$$

$R_1 = 3.13R_2$ $\quad (R_2 \sim 3$ times larger than $R_1)$

Solve for R_2:

$$R_1 \,||\, (2R_2) = \frac{R_1 * 2R_2}{R_1 + 2R_2} = 50\Omega$$

$2R_1R_2 = 50R_1 + 100R_2$

$2(3.13R_2)R_2 = 50(3.13R_2) + 100R_2$ $\quad R_1 = 3.13R_2$, replace R_1 with $3.13R_2$

$R_2 = 41\Omega$

Resistor values are $R_1 = 128\Omega$; $R_2 = 41\Omega$; $R_3 = 41\Omega$

The results of these calculations are non-standard resistor values, adjust and select the resistor values for the specific application maintaining proper matching of the line impedance and termination of the LVPECL outputs.

Interfacing LVDS to LVPECL

If an application requires interfacing from LVDS to LVPECL, direct interface is possible provided the LVPECL line receiver has the proper differential common mode input range. Refer to the individual LVPECL device datasheets for the specifications and performance requirements. This solution would simply require a single termination resistor, typically 100Ω, for matching the transmission line impedance without any additional attenuation resistor network. Refer to Figure 7. For interfacing LVDS to PECL, direct interface is possible providing the PECL receiver has extended common mode range inputs to process the LVDS signals when supplied with 5V ± 5% supply voltage.

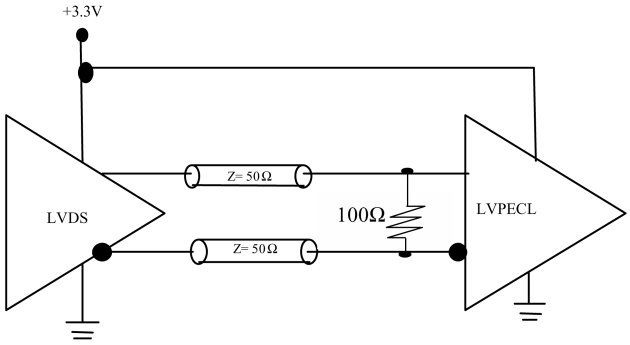


FIGURE 7. LVDS to LVPECL Interface

Summary

Interfacing between multiple differential technologies presents some challenges to system designers who must evaluate options for a cost-effective solution. Existing system requirements, signal integrity demands and costs will dictate which approach is preferred to minimize risk and optimize the reliability of the system. Although the single resistor termination to V_{TT} conserves power, the interface requires an additional termination voltage which may be impractical. An alternative approach to an additional power supply is to use a resistor divider network to develop a Thevenin voltage, termination voltage and provide impedance matching termination for the transmission line to minimize reflections. The Thevenin equivalent of the two resistors for each single ended transmission line needs to be equal to the characteristic impedance of the line. Although this scheme will consume more power, this extra power is consumed entirely in the external resistor network and will not change the current being sourced by the device, hence will not alter the reliability of the IC. The approaches illustrated in this application note provide guidelines for understanding the requirements. Compliance to all individual IC maximum ratings should be met to ensure proper system performance.

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