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AN-4185

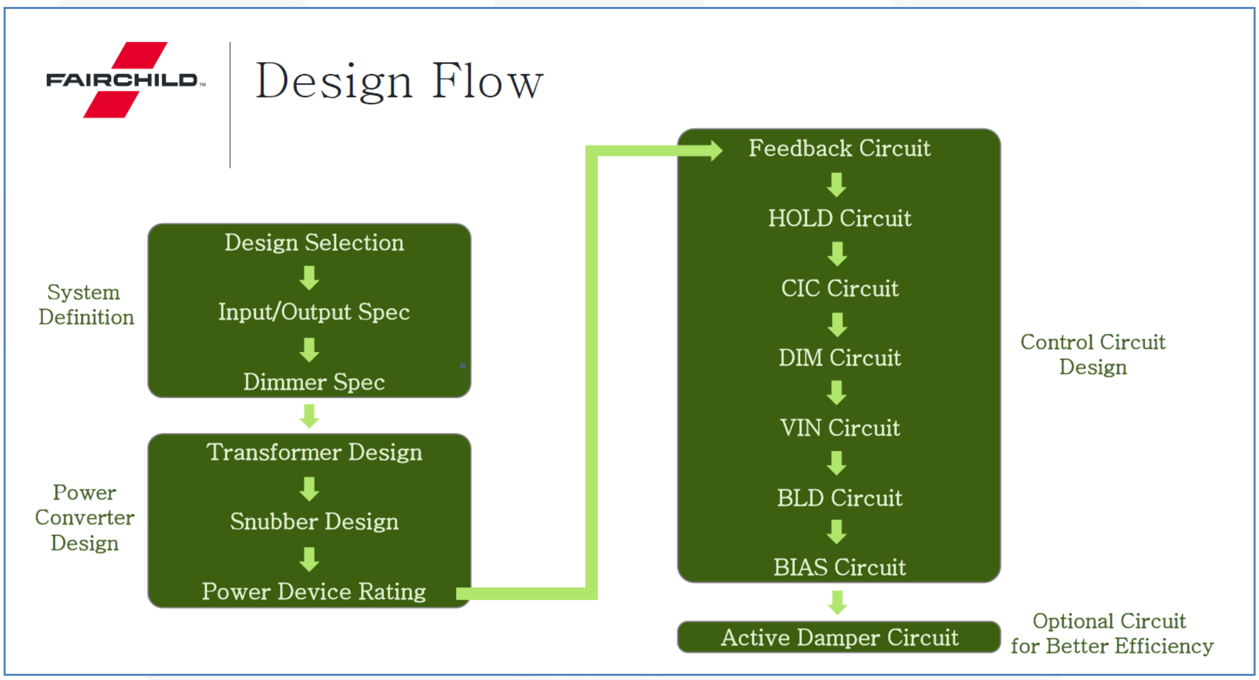
FL7734 Design Tool Flow

Overview

This application note provides a step-by-step guide for using the FL7734 Design Tool. It should be used in conjunction with the FL7734 product information.

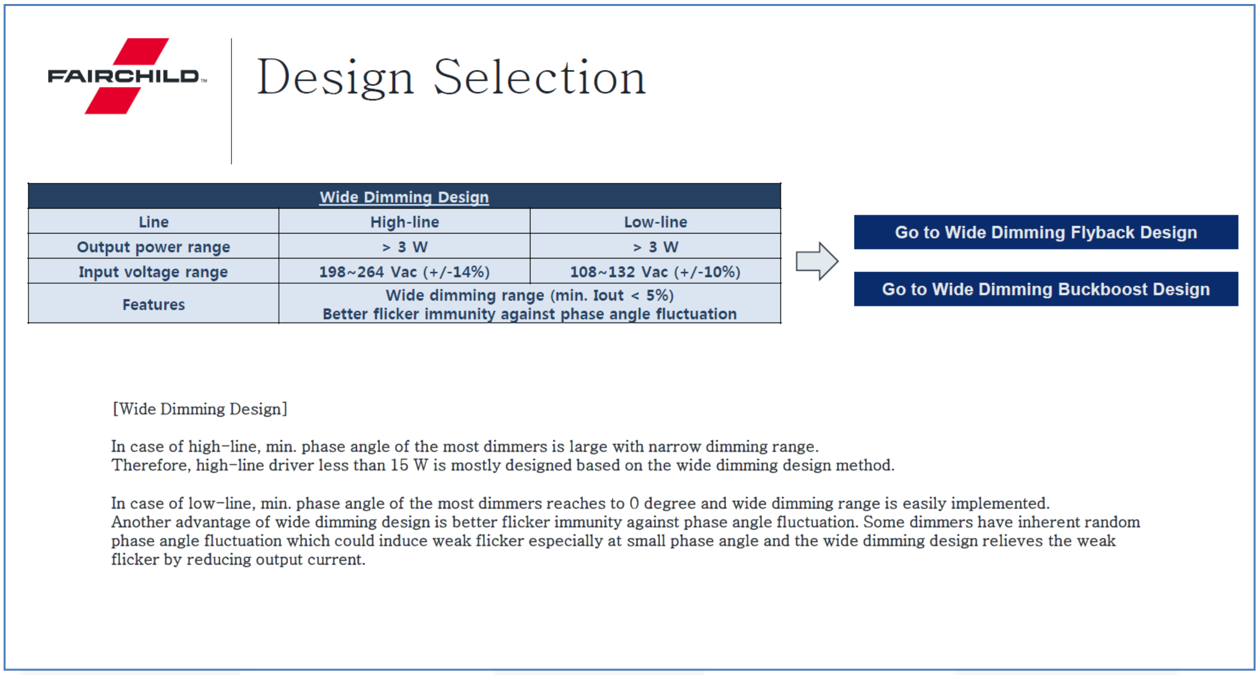
Design Flow

The FL7734 design starts with system definition. Then design parameters will be calculated through the power converter design and control circuit design. In order to increase efficiency, an active damper circuit design can be completed according to user's preference.



Design Selection

User can select 4 different designs based on target specification.



Design Selection

Wide Dimming Design		
Line	High-line	Low-line
Output power range	> 3 W	> 3 W
Input voltage range	198~264 Vac (+/-14%)	108~132 Vac (+/-10%)
Features	Wide dimming range (min. Iout < 5%) Better flicker immunity against phase angle fluctuation	

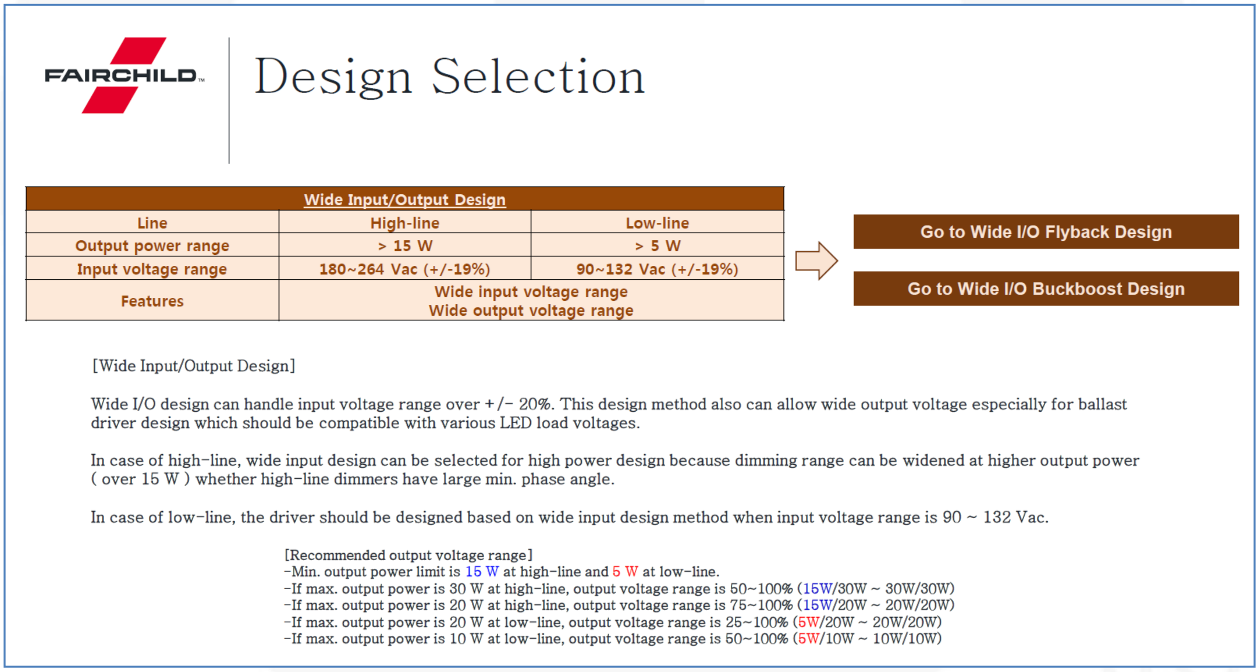
Go to Wide Dimming Flyback Design

Go to Wide Dimming Buckboost Design

[Wide Dimming Design]

In case of high-line, min. phase angle of the most dimmers is large with narrow dimming range. Therefore, high-line driver less than 15 W is mostly designed based on the wide dimming design method.

In case of low-line, min. phase angle of the most dimmers reaches to 0 degree and wide dimming range is easily implemented. Another advantage of wide dimming design is better flicker immunity against phase angle fluctuation. Some dimmers have inherent random phase angle fluctuation which could induce weak flicker especially at small phase angle and the wide dimming design relieves the weak flicker by reducing output current.



Design Selection

Wide Input/Output Design		
Line	High-line	Low-line
Output power range	> 15 W	> 5 W
Input voltage range	180~264 Vac (+/-19%)	90~132 Vac (+/-19%)
Features	Wide input voltage range Wide output voltage range	

Go to Wide I/O Flyback Design

Go to Wide I/O Buckboost Design

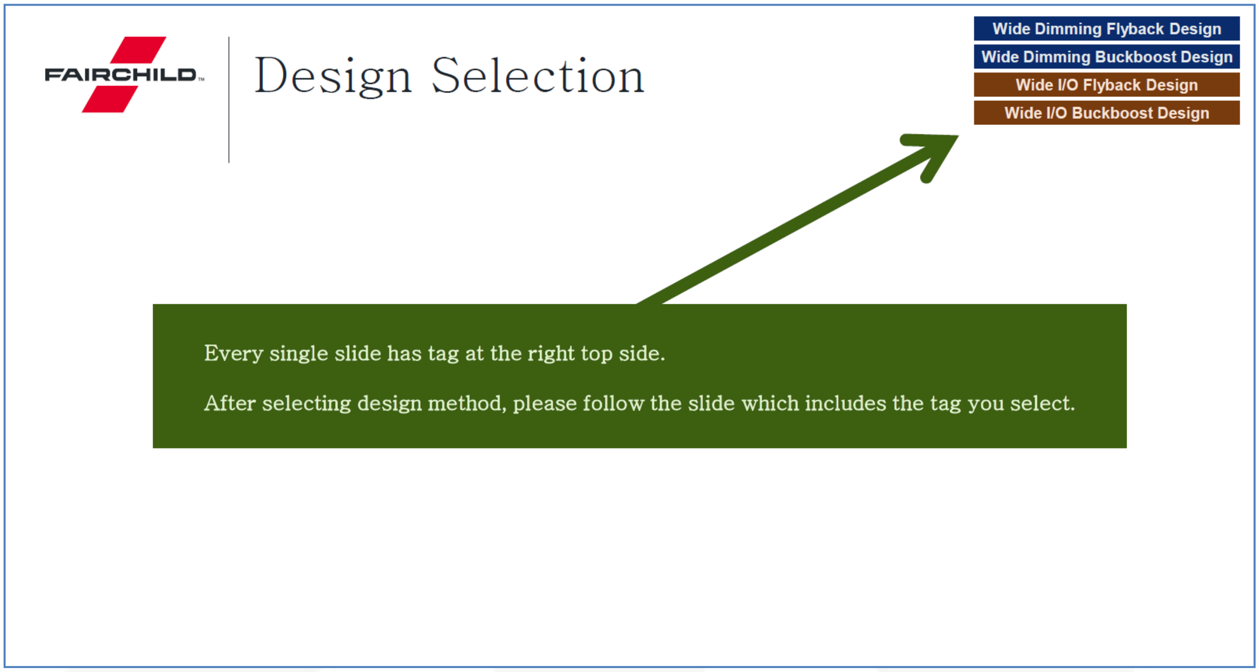
[Wide Input/Output Design]

Wide I/O design can handle input voltage range over +/- 20%. This design method also can allow wide output voltage especially for ballast driver design which should be compatible with various LED load voltages.

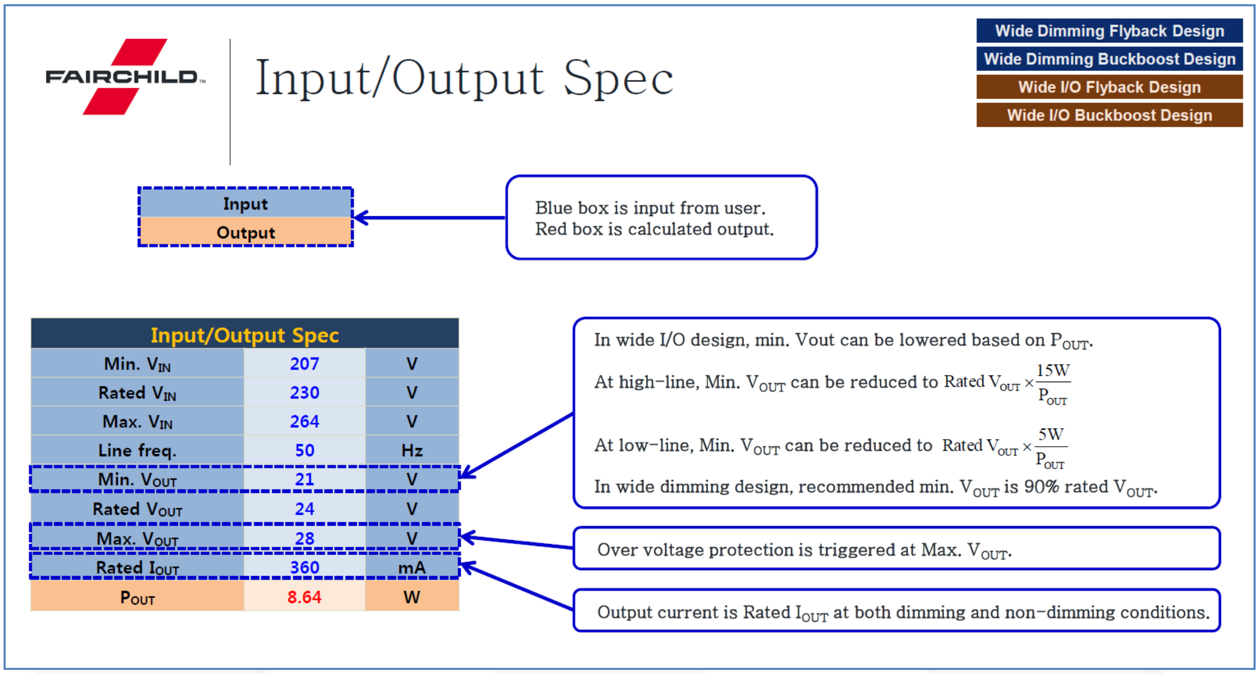
In case of high-line, wide input design can be selected for high power design because dimming range can be widened at higher output power (over 15 W) whether high-line dimmers have large min. phase angle.

In case of low-line, the driver should be designed based on wide input design method when input voltage range is 90 ~ 132 Vac.

[Recommended output voltage range]
-Min. output power limit is 15 W at high-line and 5 W at low-line.
-If max. output power is 30 W at high-line, output voltage range is 50~100% (15W/30W ~ 30W/30W)
-If max. output power is 20 W at high-line, output voltage range is 75~100% (15W/20W ~ 20W/20W)
-If max. output power is 20 W at low-line, output voltage range is 25~100% (5W/20W ~ 20W/20W)
-If max. output power is 10 W at low-line, output voltage range is 50~100% (5W/10W ~ 10W/10W)

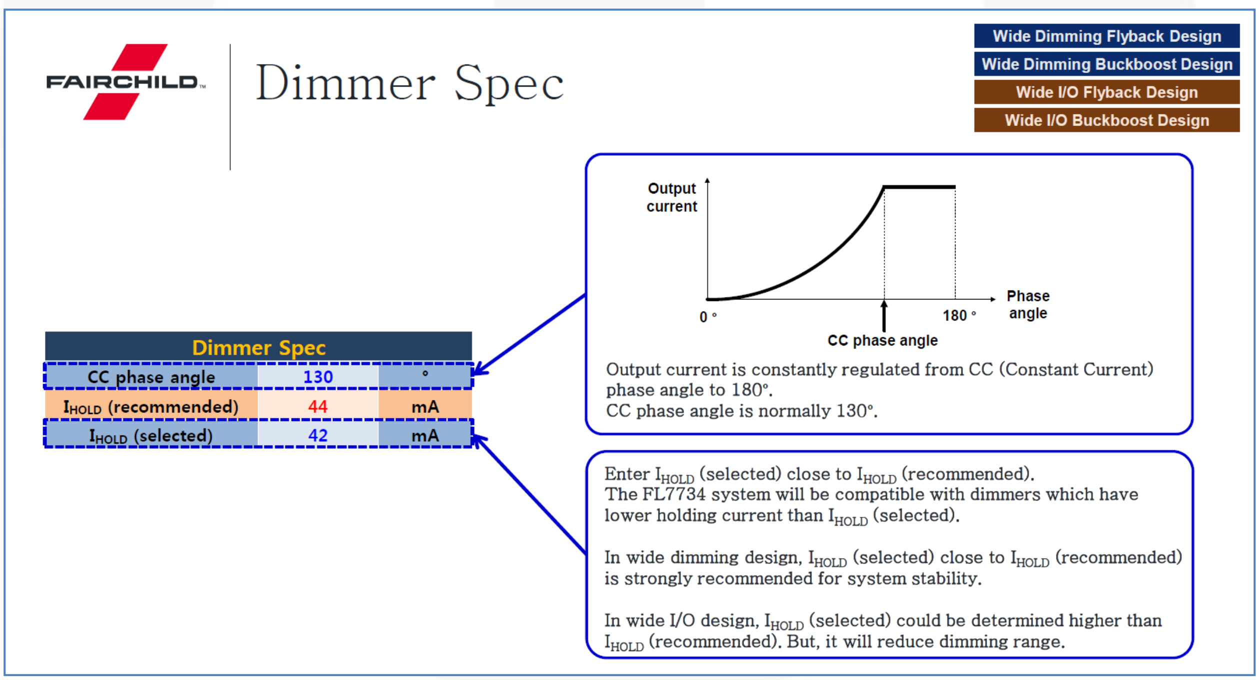

Design Selection
Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design
Every single slide has tag at the right top side.
After selecting design method, please follow the slide which includes the tag you select.

Step 1 – Input / Output Specs



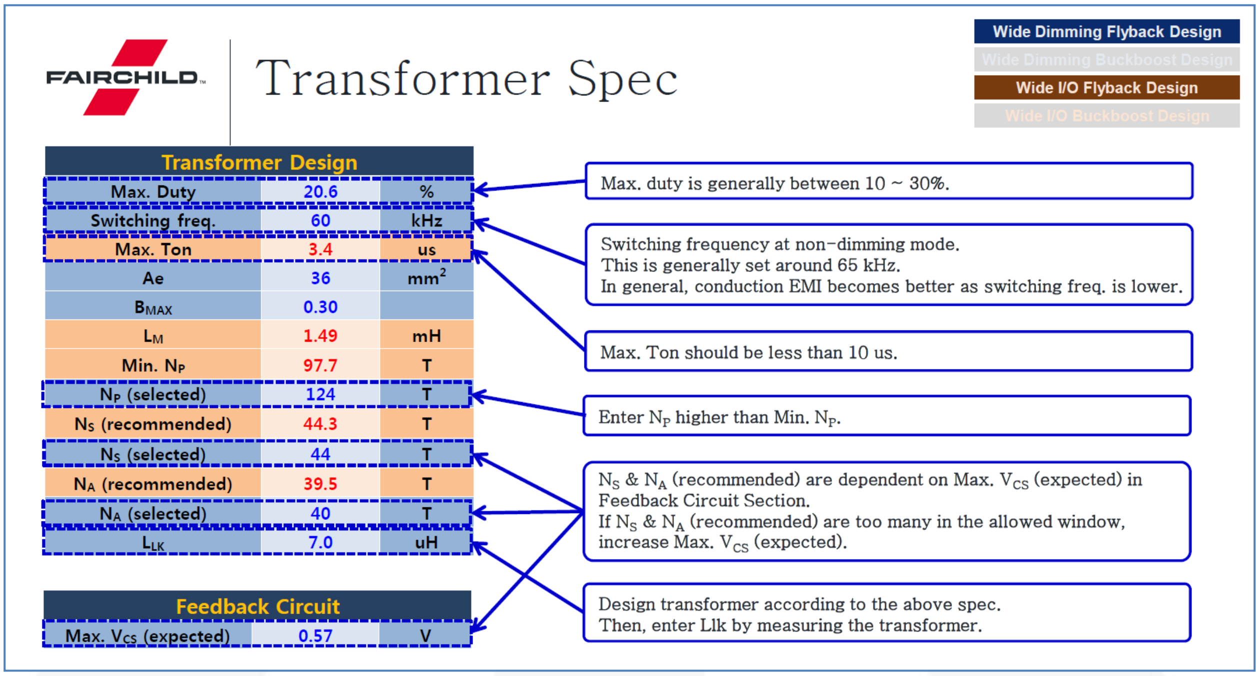
Input/Output Spec		
Min. V_{IN}	207	V
Rated V_{IN}	230	V
Max. V_{IN}	264	V
Line freq.	50	Hz
Min. V_{OUT}	21	V
Rated V_{OUT}	24	V
Max. V_{OUT}	28	V
Rated I_{OUT}	360	mA
P_{OUT}	8.64	W

Step 2 – Dimmer Specs



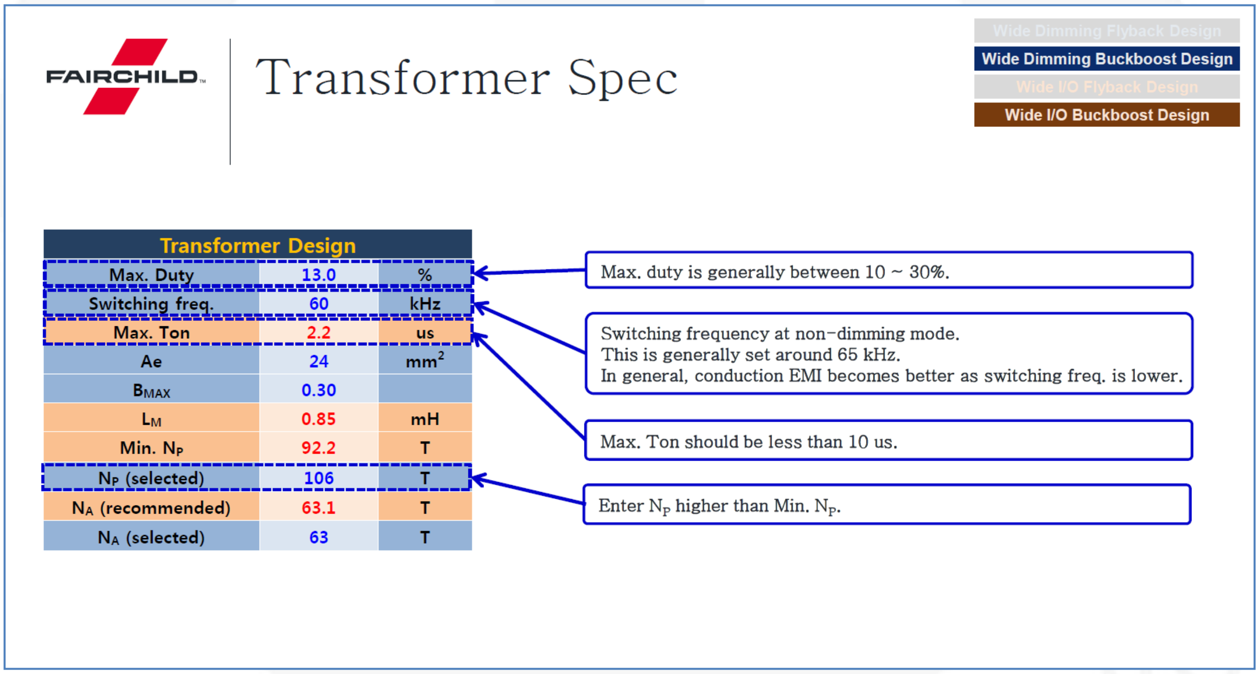
Dimmer Spec		
CC phase angle	130	°
I_{HOLD} (recommended)	44	mA
I_{HOLD} (selected)	42	mA

Step 3 –Transformer Specs



Transformer Design		
Max. Duty	20.6	%
Switching freq.	60	kHz
Max. Ton	3.4	us
Ae	36	mm^2
B_{MAX}	0.30	
L_M	1.49	mH
Min. N_P	97.7	T
N_P (selected)	124	T
N_S (recommended)	44.3	T
N_S (selected)	44	T
N_A (recommended)	39.5	T
N_A (selected)	40	T
L_{LK}	7.0	uH

Feedback Circuit		
Max. V_{CS} (expected)	0.57	V



Transformer Design		
Max. Duty	13.0	%
Switching freq.	60	kHz
Max. Ton	2.2	us
Ae	24	mm^2
B_{MAX}	0.30	
L_M	0.85	mH
Min. N_P	92.2	T
N_P (selected)	106	T
N_A (recommended)	63.1	T
N_A (selected)	63	T

Step 4 – Snubber Specs

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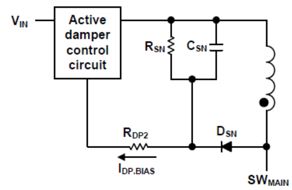
Snubber Spec

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

Snubber Design		
V_{SN}	150	V
ΔV_{SN}	10	V
R_{SN} (w/o active damper)	117	kohm
R_{SN} (w/ active damper)	193	kohm
C_{SN}	2	nF

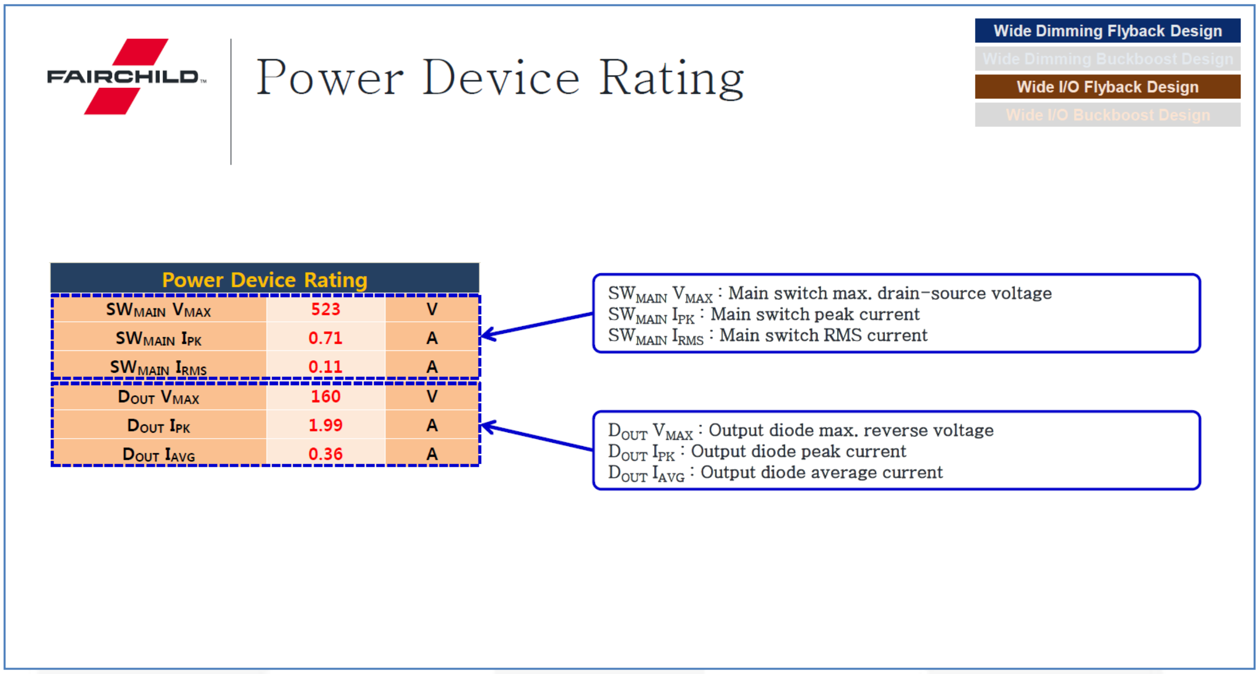
V_{SN} is generally set as 2 ~ 2.5 times n_{PS} x V_{OUT}.

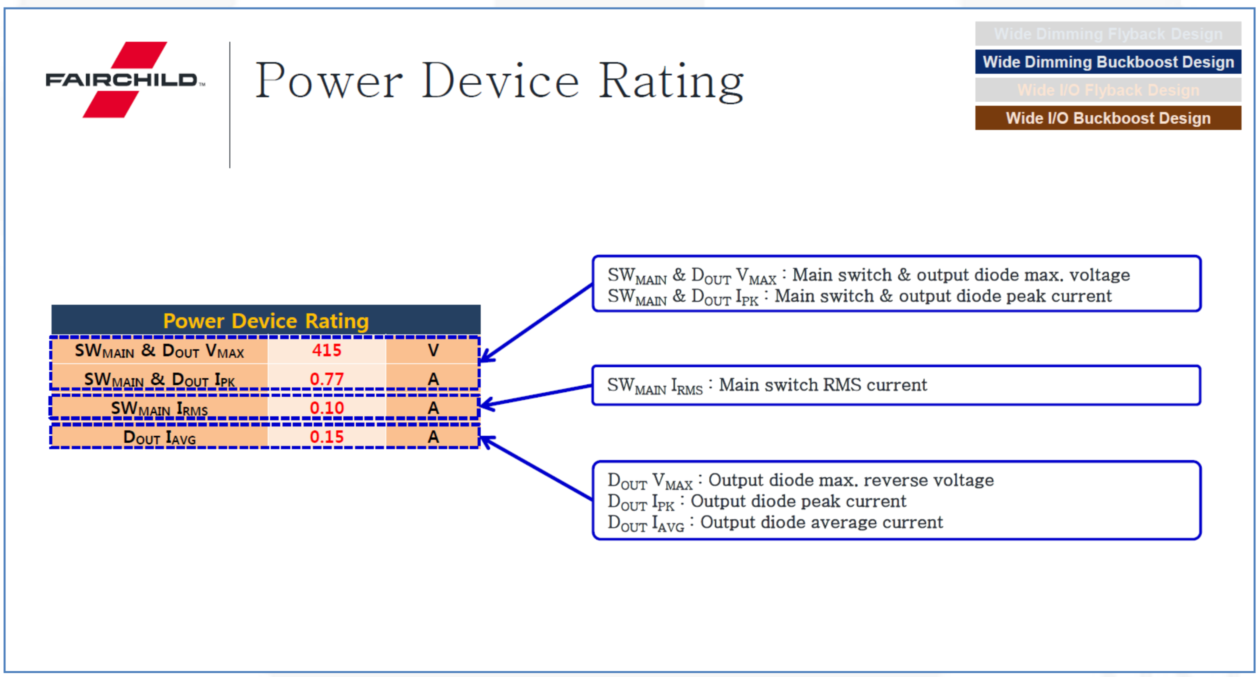
ΔV_{SN} is generally set as 5% ripple of V_{SN}.



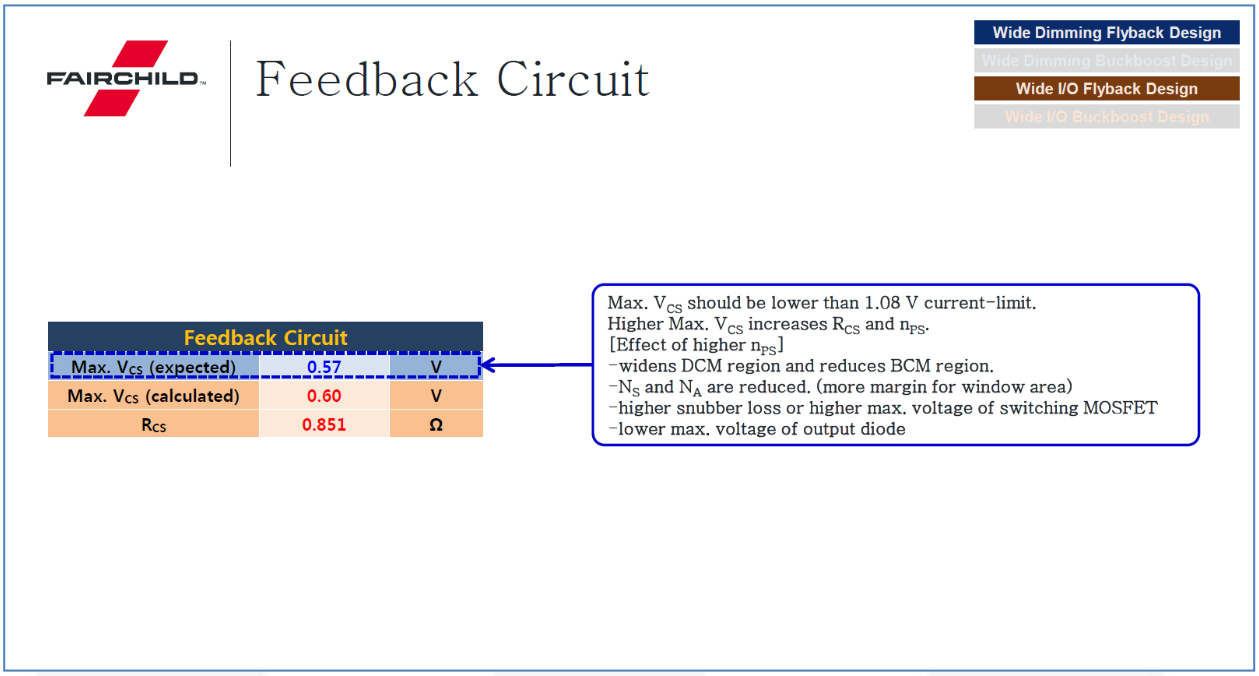
If active damper is not used, select R_{SN} (w/o active damper)
If active damper is used, select R_{SN} (w/ active damper)
Because R_{DP2} path provides biasing current for active damper, snubber voltage is determined by both R_{SN} and R_{DP2} path.

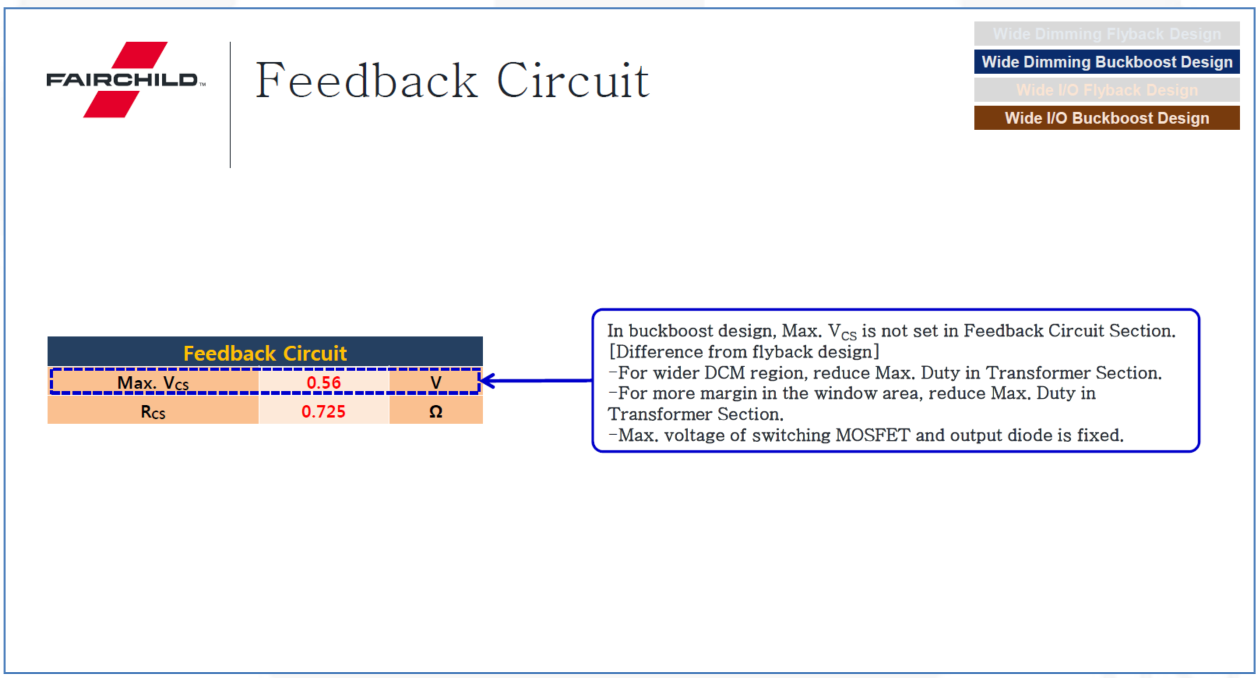
Step 5 – Power Device Rating





Step 6 – Feedback Circuits

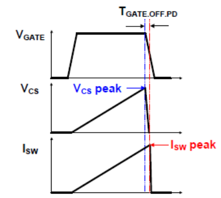




Feedback Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

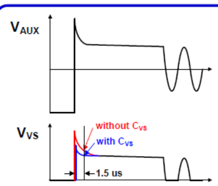
Feedback Circuit		
$T_{GATE.OFF.PD}$	90	ns
R_{COMP}	159	Ω
C_{FB}	1.0	uF
R_{VS1}	302	kΩ
R_{VS2}	38	kΩ
C_{VS}	10	pF



$T_{GATE.OFF.PD}$ is the time from V_{CS} peak to I_{SW} (Switch current) peak. I_{SW} should be measured at the node between transformer and MOSFET drain.

R_{COMP} compensates CC tolerance by line voltage change. (Line CC tolerance is caused by $T_{GATE.OFF.PD}$.)

C_{FB} is typically 1 ~ 2.2 uF. Larger C_{FB} makes slower feedback loop.



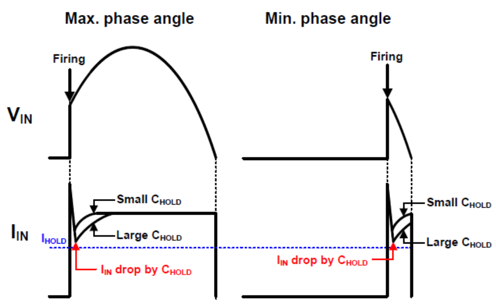
C_{VS} relieves voltage spike at gate-off. Increase C_{VS} until VS voltage at 1.5 us after gate-off is flat.

Step 7 – HOLD Circuits

HOLD Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

HOLD Circuit		
R_{HOLD}	18	kΩ
C_{HOLD}	1.0	nF



In general, C_{HOLD} is 1 ~ 5 nF.

Large C_{HOLD} has pros and cons.
Pros : can remove LED shimmer if there is.
Cons : input current at firing drops which can cause TRIAC mis-firing with flicker.

How to select C_{HOLD}.
1. Select the worst dimmer which has the highest holding current in user's dimmer list.
2. Increase C_{HOLD} until input current drop at firing is not lower than TRIAC holding current.
(The test condition should be max. and min. phase angle, in which input current drop is the lowest.)

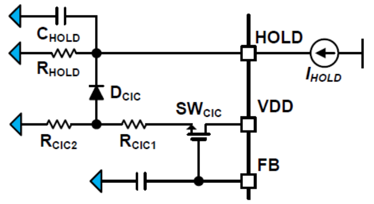
Step 8 – CIC Circuit

CIC Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

CIC Circuit		
R_{TCIC} (recommended)	333	kΩ
R_{TCIC} (selected)	330	kΩ
C_{TCIC}	33	nF
SW_{CIC}	2N7002	
D_{CIC}	1N4148WS	
R_{CIC1}	11.4	kΩ
R_{CIC2}	8.6	kΩ

Yield and temperature tolerance
R_{TCIC} should be less than +/− 1%.
C_{TCIC} should be less than +/− 5%.

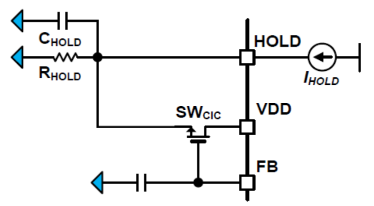


FB voltage can control HOLD voltage by HOLD pull-up circuit (SW_{CIC}, D_{CIC}, R_{CIC1} and R_{CIC2}).
When FB voltage is increased, HOLD voltage is pulled up and input current level is increased with more power delivery.

CIC Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

CIC Circuit	
SW_{CIC}	2N7002

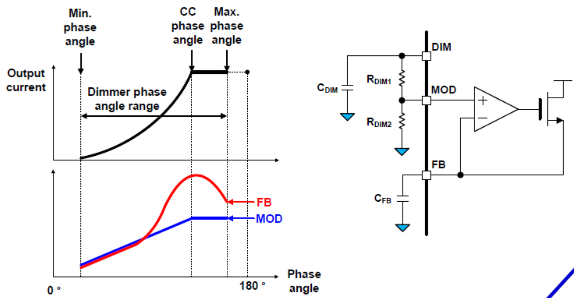


In wide I/O design, FB voltage controls HOLD voltage simply by SW_{CIC}.

Step 9 – DIM Circuit

DIM Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design



DIM Circuit		
R_{DIM1}	24	kΩ
R_{DIM2}	90	kΩ
C_{DIM}	438	nF

[Yield and temperature tolerance]

–R_{DIM1} and R_{DIM2} tolerance should be less than +/− 1%.

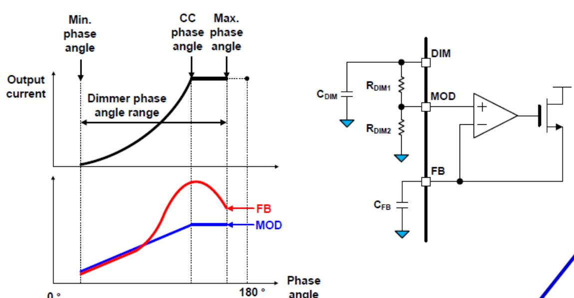
[$\frac{R_{DIM2}}{R_{DIM1}+R_{DIM2}}$ (=r_{DIM}) selection]

*Max. r_{DIM} limit
–FB should not be clamped by MOD voltage at max. phase angle.
(If MOD clamps FB voltage at max. phase angle,
output current will be higher than the rated output current.)
–Therefore, check if FB is clamped by MOD voltage at max. phase angle condition.
–If FB is pulled up by MOD voltage, reduce r_{DIM}. (In order to reduce r_{DIM}, increase R_{DIM1} and decrease R_{DIM2}. Keep R_{DIM1} + R_{DIM2} same as design tool.)

*Min. r_{DIM} limit
–If output current oscillation with periodic visible flicker is occurred, increase r_{DIM}.

DIM Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design



DIM Circuit		
R_{DIM1}	24	kΩ
R_{DIM2}	90	kΩ
C_{DIM}	438	nF

[Yield and temperature tolerance]

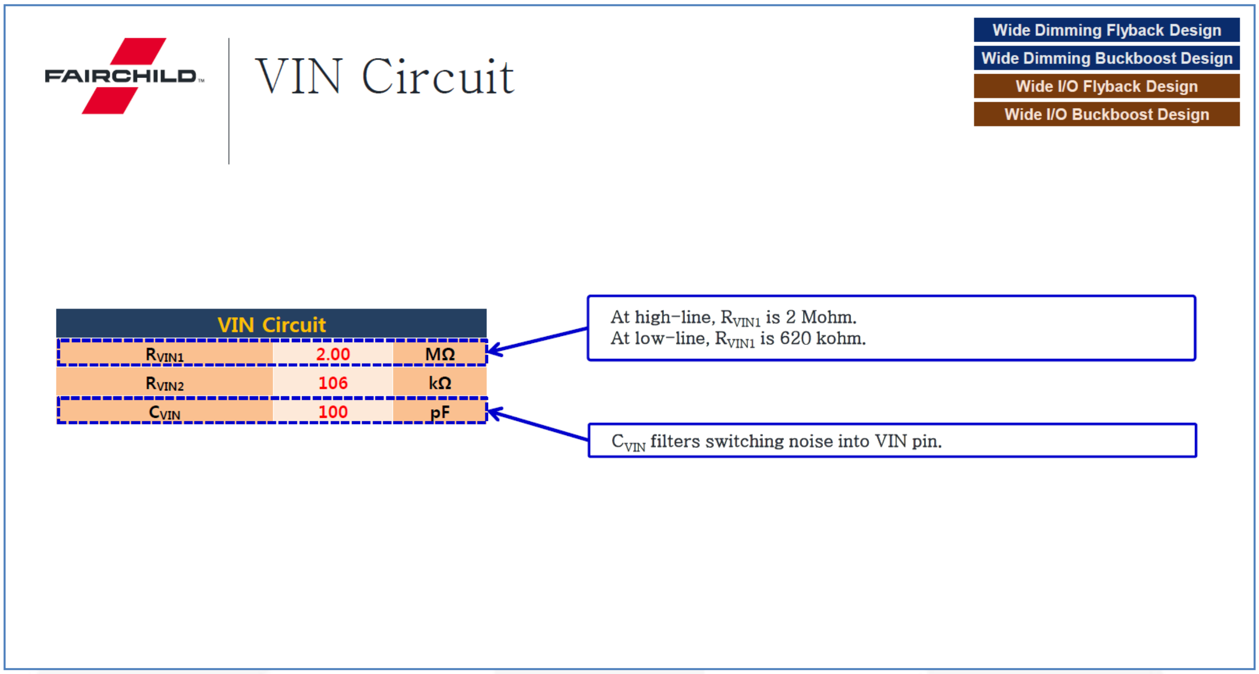
–R_{DIM1} and R_{DIM2} tolerance should be less than +/− 1%.

[$\frac{R_{DIM2}}{R_{DIM1}+R_{DIM2}}$ (=r_{DIM}) selection]

*Max. r_{DIM} limit
–At wide I/O design, calculated r_{DIM} is low enough and FB is hardly clamped by MOD at max. phase angle condition.
–Therefore, user doesn't need to check FB clamping like wide dimming design.

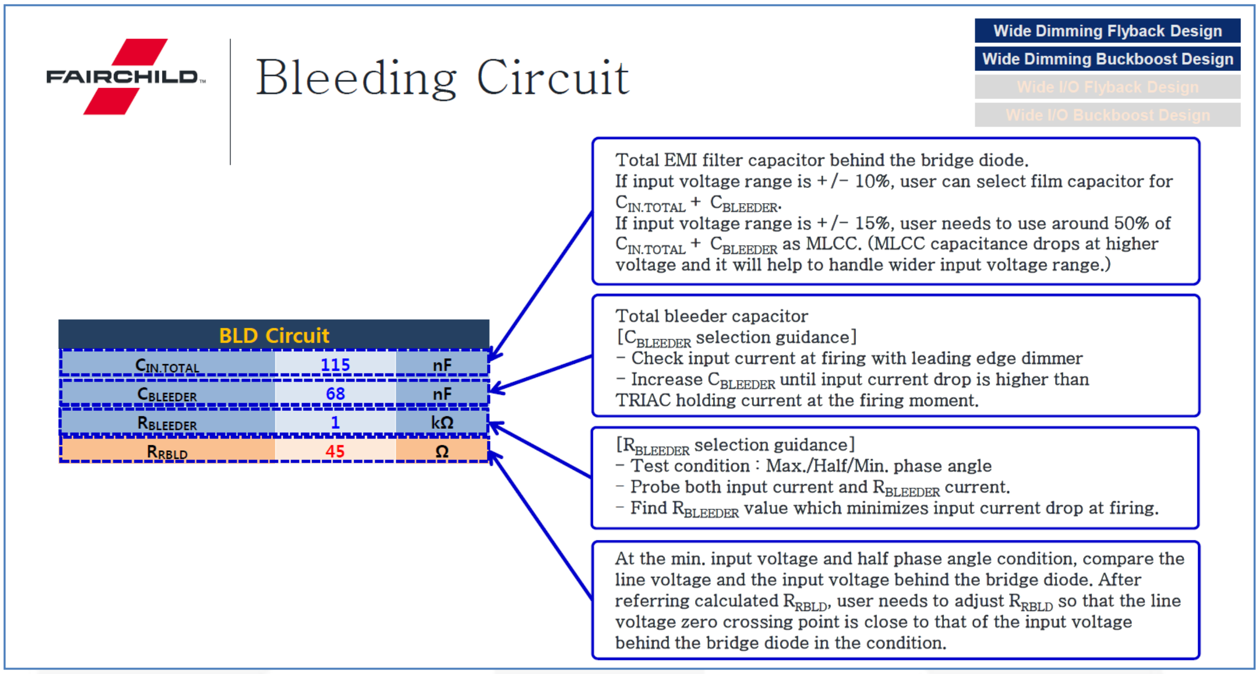
*Min. r_{DIM} limit
–At wide I/O design, there is no output current oscillation with periodic visible flicker.
–Therefore, user doesn't need to check periodic visible flicker like wide dimming design.

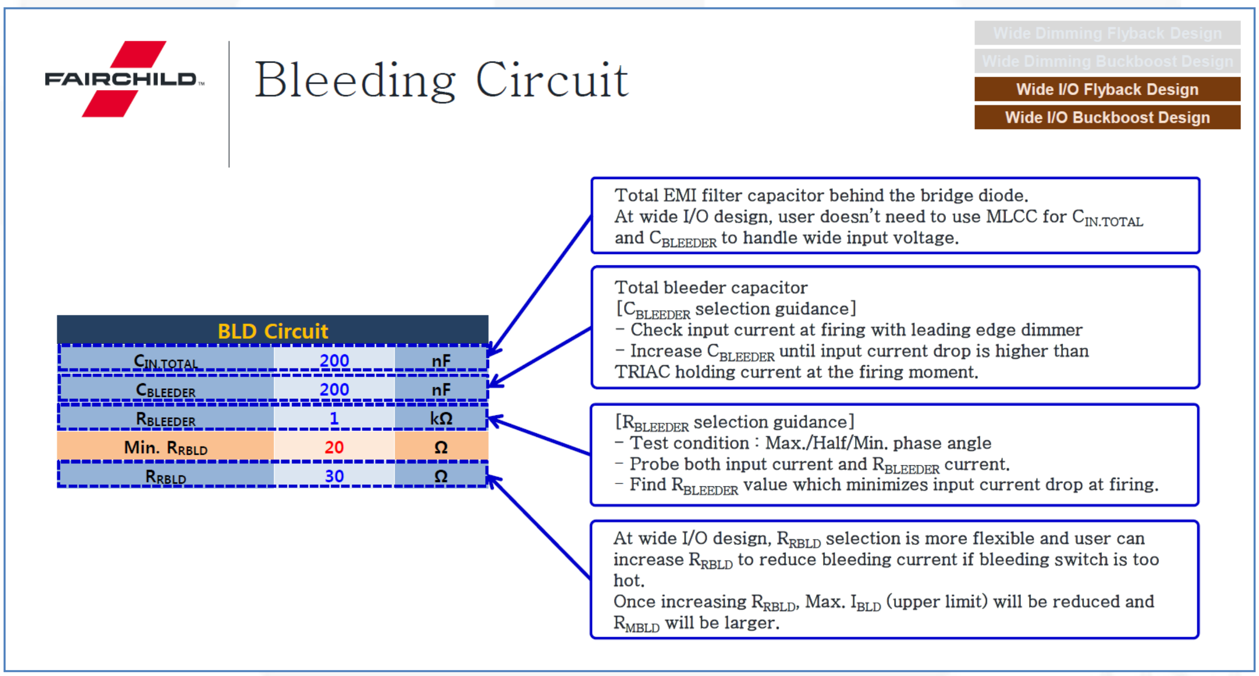
Step 10 – VIN Circuit



VIN Circuit		
R_{VIN1}	2.00	MΩ
R_{VIN2}	106	kΩ
C_{VIN}	100	pF

Step 11 – Bleeding Circuit





Bleeding Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

BLD Circuit		
Max. I_{BLD} (upper limit)	111	mA
Max. I_{BLD}	96	mA
R_{MBLD}	108	kΩ
R_{BLD}	63	Ω
R_{VDD1}	100	Ω

Max. bleeding current : Bleeding current during startup sequence and phase-cut time.
Select this value lower than Max. I_{BLD} (upper limit).

Higher Max. I_{BLD} can have more margin to maintain input current higher than holding current during startup sequence.

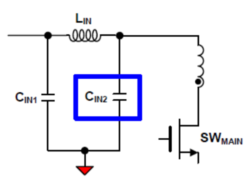
Lower Max. I_{BLD} can reduce the SW_{BLD} temperature during startup sequence and AR time.

R_{VDD1} dampens leading edge spike noise into VDD pin. 100 ohm is recommended at high-line and 50 ohm is recommended at low-line.

Bleeding Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

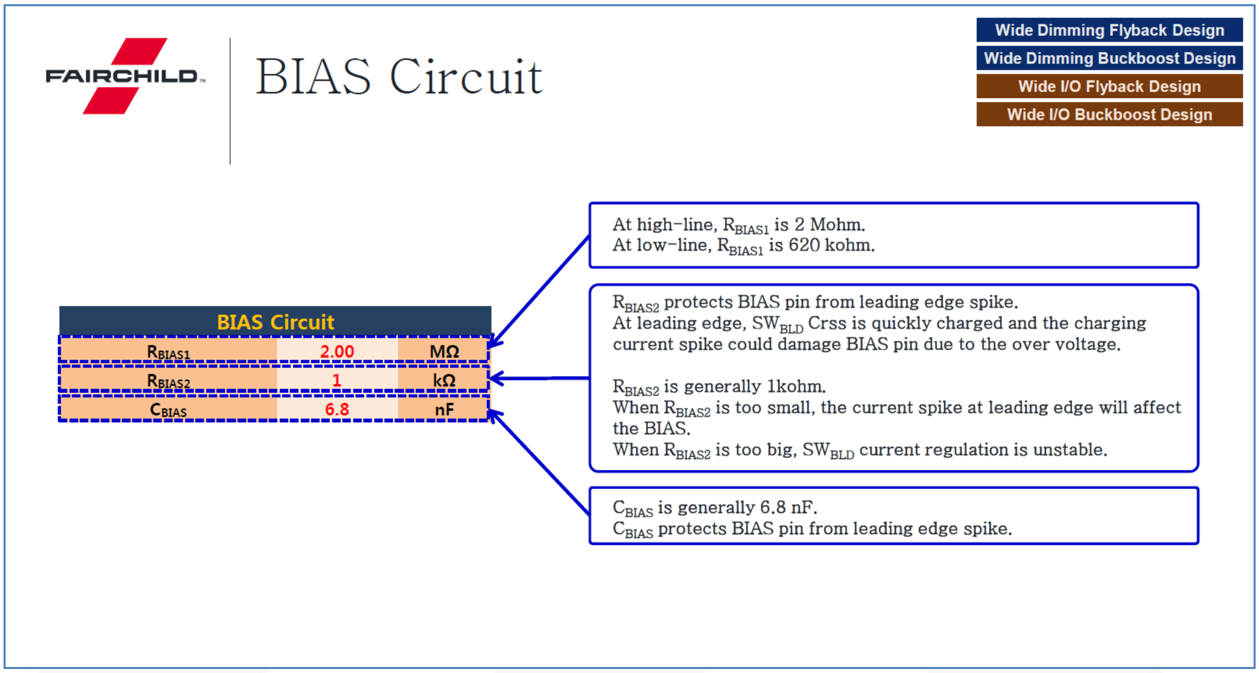
BLD Circuit		
C_{IN2}	68	nF
R_{OFFSET}	28	kΩ



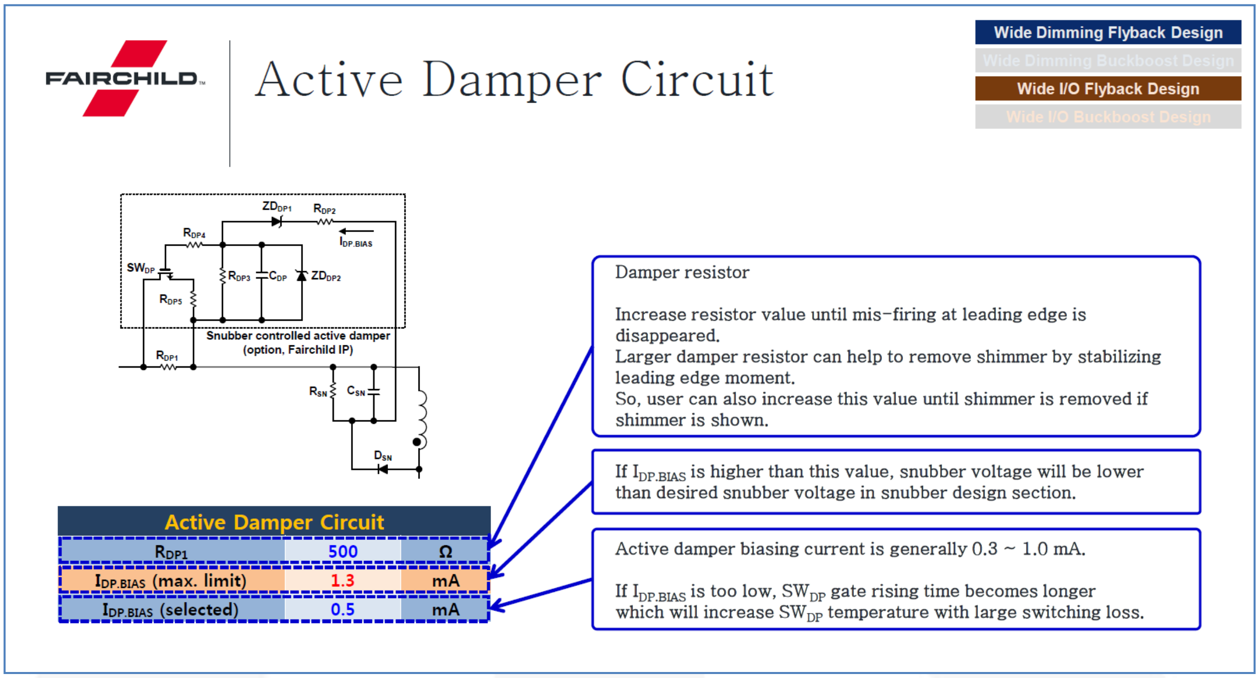
C_{IN2} is total EMI filter capacitor directly connected to transformer.

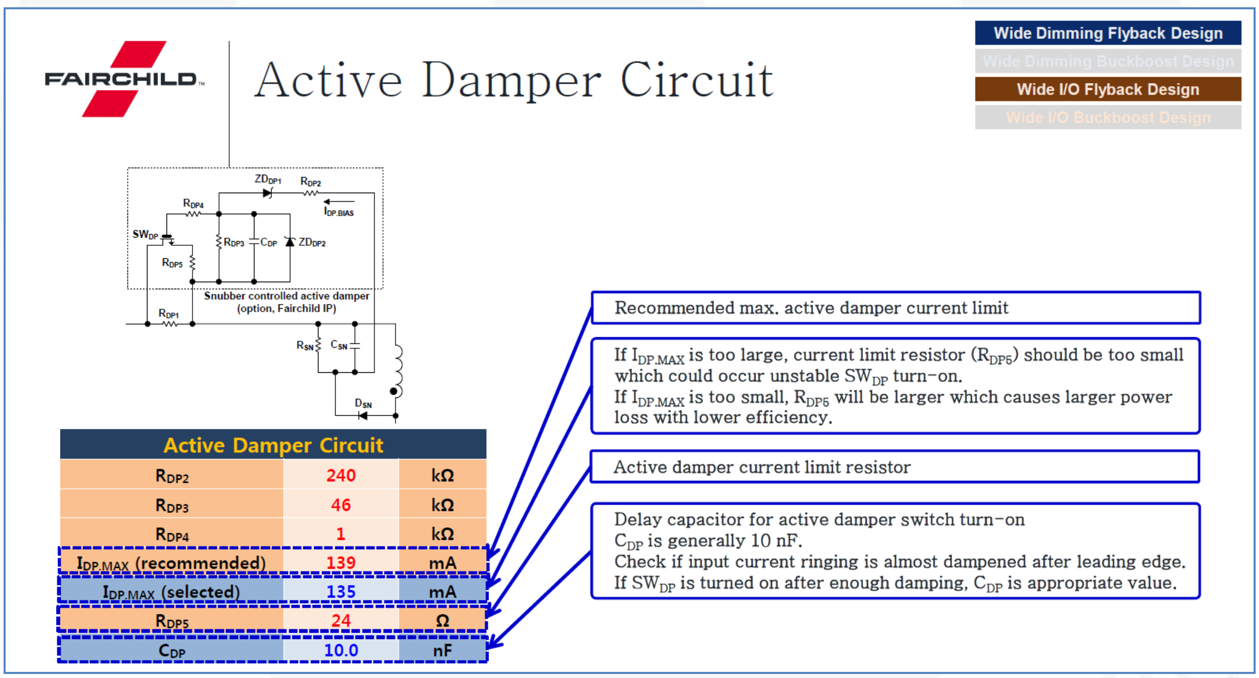
SRSP (sensing resistor short protection) is triggered when CS voltage is less than 0.1 V at first and second switching.
When Lm is highly designed, SRSP could be abnormally triggered due to low CS peak voltage.
R_{OFFSET} can protect system from abnormally triggered SRSP by building voltage offset on R_{COMP}.
If CS peak is much higher than 0.1 V with small Lm, "open" message will appear and user doesn't need to add R_{OFFSET}.

Step 12 – BIAS Circuit



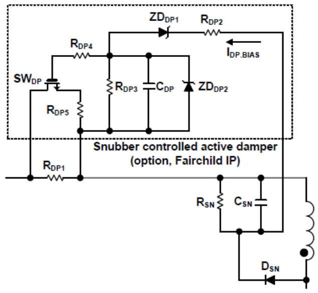
Step 13 – Active Damper Circuit

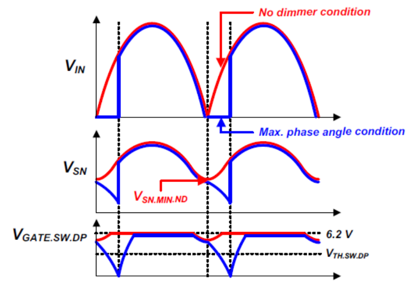




Active Damper Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design





Active Damper Circuit		
$V_{SN.MIN.ND}$	55	V
$V_{ZD.DP1}$	30	V
$V_{ZD.DP2}$	6.2	V

Minimum snubber voltage at ND.MODE.
Enter the snubber voltage at zero crossing voltage.

$V_{ZD.DP1}$ is generally 30 V and should be lower than $V_{SN.MIN.ND}$.
If SW_{DP} is always turned on at max. phase angle condition, increase $V_{ZD.DP1}$.
If SW_{DP} gate is turned off with efficiency drop at no dimmer condition, reduce $V_{ZD.DP1}$.

Related Resources

FL7734 –Single-Stage Primary-Side-Regulation PWM Controller for PFC and Phase Cut Dimmable LED Driving

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