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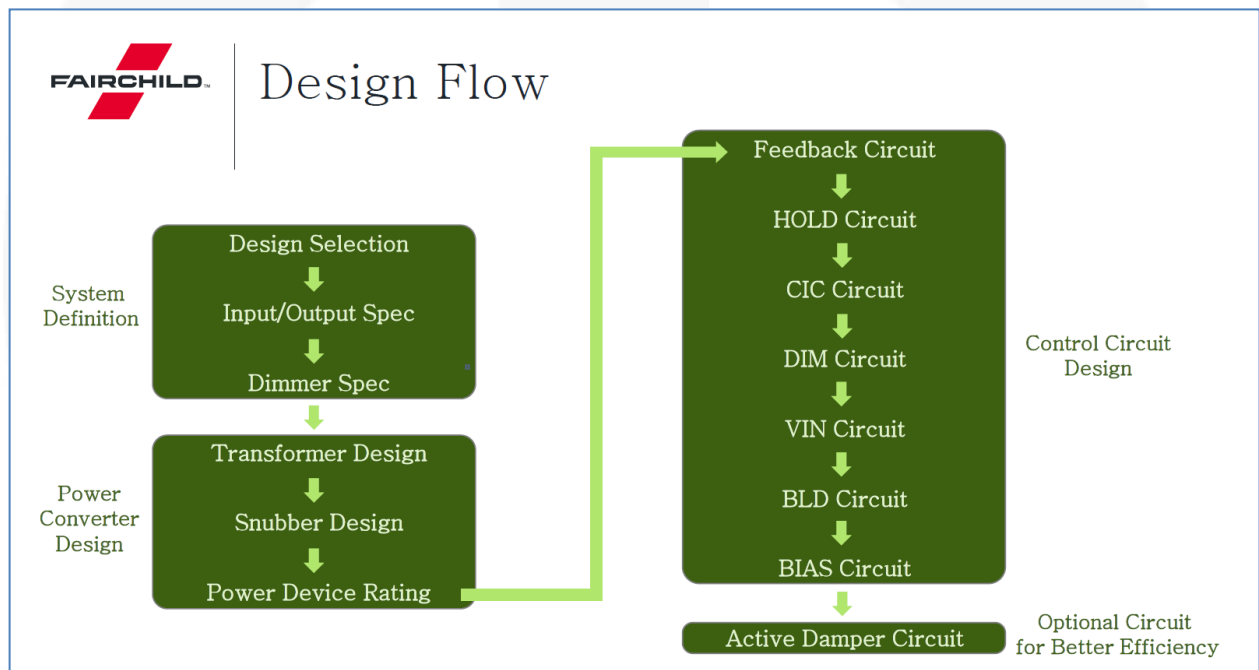
FL7734 Design Tool Flow

Overview

This application note provides a step-by-step guide for using the FL7734 Design Tool. It should be used in conjunction with the FL7734 product information.


Design Flow

The FL7734 design starts with system definition. Then design parameters will be calculated through the power converter design and control circuit design. In order to increase efficiency, an active damper circuit design can be completed according to user's preference.



Design Selection

User can select 4 different designs based on target specification.



Design Selection

Wide Dimming Design		
Line	High-line	Low-line
Output power range	> 3 W	> 3 W
Input voltage range	198~264 Vac (+/-14%)	108~132 Vac (+/-10%)
Features	Wide dimming range (min. I _{out} < 5%) Better flicker immunity against phase angle fluctuation	


Go to Wide Dimming Flyback Design

Go to Wide Dimming Buckboost Design

[Wide Dimming Design]

In case of high-line, min. phase angle of the most dimmers is large with narrow dimming range. Therefore, high-line driver less than 15 W is mostly designed based on the wide dimming design method.

In case of low-line, min. phase angle of the most dimmers reaches to 0 degree and wide dimming range is easily implemented. Another advantage of wide dimming design is better flicker immunity against phase angle fluctuation. Some dimmers have inherent random phase angle fluctuation which could induce weak flicker especially at small phase angle and the wide dimming design relieves the weak flicker by reducing output current.



Design Selection

Wide Input/Output Design		
Line	High-line	Low-line
Output power range	> 15 W	> 5 W
Input voltage range	180~264 Vac (+/-19%)	90~132 Vac (+/-19%)
Features	Wide input voltage range Wide output voltage range	

Go to Wide I/O Flyback Design

Go to Wide I/O Buckboost Design

[Wide Input/Output Design]

Wide I/O design can handle input voltage range over +/- 20%. This design method also can allow wide output voltage especially for ballast driver design which should be compatible with various LED load voltages.

In case of high-line, wide input design can be selected for high power design because dimming range can be widened at higher output power (over 15 W) whether high-line dimmers have large min. phase angle.

In case of low-line, the driver should be designed based on wide input design method when input voltage range is 90 ~ 132 Vac.

[Recommended output voltage range]

- Min. output power limit is 15 W at high-line and 5 W at low-line.
- If max. output power is 30 W at high-line, output voltage range is 50~100% (15W/30W ~ 30W/30W)
- If max. output power is 20 W at high-line, output voltage range is 75~100% (15W/20W ~ 20W/20W)
- If max. output power is 20 W at low-line, output voltage range is 25~100% (5W/20W ~ 20W/20W)
- If max. output power is 10 W at low-line, output voltage range is 50~100% (5W/10W ~ 10W/10W)




Design Selection

- Wide Dimming Flyback Design
- Wide Dimming Buckboost Design
- Wide I/O Flyback Design
- Wide I/O Buckboost Design

Every single slide has tag at the right top side.
After selecting design method, please follow the slide which includes the tag you select.



Step 1 – Input / Output Specs



Input/Output Spec

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

Input

Output

Blue box is input from user.
 Red box is calculated output.


Input/Output Spec		
Min. V_{IN}	207	V
Rated V_{IN}	230	V
Max. V_{IN}	264	V
Line freq.	50	Hz
Min. V_{OUT}	21	V
Rated V_{OUT}	24	V
Max. V_{OUT}	28	V
Rated I_{OUT}	360	mA
P_{OUT}	8.64	W

In wide I/O design, min. V_{OUT} can be lowered based on P_{OUT} .
 At high-line, Min. V_{OUT} can be reduced to $\text{Rated } V_{OUT} \times \frac{15W}{P_{OUT}}$
 At low-line, Min. V_{OUT} can be reduced to $\text{Rated } V_{OUT} \times \frac{5W}{P_{OUT}}$
 In wide dimming design, recommended min. V_{OUT} is 90% rated V_{OUT} .

Over voltage protection is triggered at Max. V_{OUT} .

Output current is Rated I_{OUT} at both dimming and non-dimming conditions.

Step 2 – Dimmer Specs

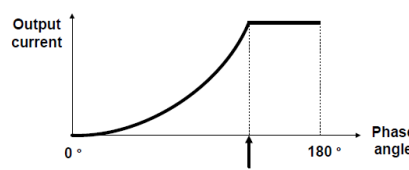


Dimmer Spec

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

Dimmer Spec

CC phase angle	130	
I_{HOLD} (recommended)	44	mA
I_{HOLD} (selected)	42	mA




Output current is constantly regulated from CC (Constant Current) phase angle to 180°.
CC phase angle is normally 130°.

Enter I_{HOLD} (selected) close to I_{HOLD} (recommended). The FL7734 system will be compatible with dimmers which have lower holding current than I_{HOLD} (selected).

In wide dimming design, I_{HOLD} (selected) close to I_{HOLD} (recommended) is strongly recommended for system stability.

In wide I/O design, I_{HOLD} (selected) could be determined higher than I_{HOLD} (recommended). But, it will reduce dimming range.

Step 3 –Transformer Specs



Transformer Spec

Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design

Transformer Design		
Max. Duty	20.6	%
Switching freq.	60	kHz
Max. Ton	3.4	us
Ae	36	mm ²
B _{MAX}	0.30	
L _M	1.49	mH
Min. N _P	97.7	T
N _P (selected)	124	T
N _S (recommended)	44.3	T
N _S (selected)	44	T
N _A (recommended)	39.5	T
N _A (selected)	40	T
L _{LK}	7.0	uH

Feedback Circuit	
Max. V _{CS} (expected)	0.57 V

Max. duty is generally between 10 ~ 30%.


Switching frequency at non-dimming mode. This is generally set around 65 kHz. In general, conduction EMI becomes better as switching freq. is lower.

Max. Ton should be less than 10 us.

Enter N_P higher than Min. N_P.

N_S & N_A (recommended) are dependent on Max. V_{CS} (expected) in Feedback Circuit Section. If N_S & N_A (recommended) are too many in the allowed window, increase Max. V_{CS} (expected).

Design transformer according to the above spec. Then, enter L_{LK} by measuring the transformer.



Transformer Spec

Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design

Transformer Design		
Max. Duty	13.0	%
Switching freq.	60	kHz
Max. Ton	2.2	us
Ae	24	mm ²
B _{MAX}	0.30	
L _M	0.85	mH
Min. N _P	92.2	T
N _P (selected)	106	T
N _A (recommended)	63.1	T
N _A (selected)	63	T

Max. duty is generally between 10 ~ 30%.

Switching frequency at non-dimming mode. This is generally set around 65 kHz. In general, conduction EMI becomes better as switching freq. is lower.

Max. Ton should be less than 10 us.

Enter N_P higher than Min. N_P.

Step 4 – Snubber Specs



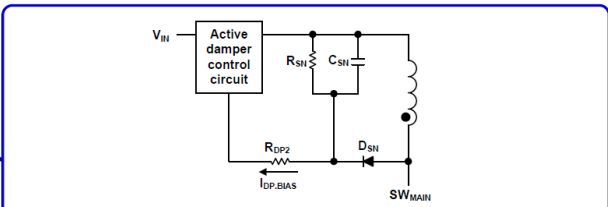
Snubber Spec

- Wide Dimming Flyback Design
- Wide Dimming Buckboost Design
- Wide I/O Flyback Design
- Wide I/O Buckboost Design

Snubber Design		
V_{SN}	150	V
ΔV_{SN}	10	V
R_{SN} (w/o active damper)	117	kohm
R_{SN} (w/ active damper)	193	kohm
C_{SN}	2	nF


V_{SN} is generally set as 2 ~ 2.5 times $n_{FS} \times V_{OUT}$.

ΔV_{SN} is generally set as 5% ripple of V_{SN} .



If active damper is not used, select R_{SN} (w/o active damper)
 If active damper is used, select R_{SN} (w/ active damper)
 Because R_{DP2} path provides biasing current for active damper, snubber voltage is determined by both R_{SN} and R_{DP2} path.

Step 5 – Power Device Rating



Power Device Rating

Wide Dimming Flyback Design

Wide Dimming Buckboost Design


Wide I/O Flyback Design

Wide I/O Buckboost Design

Power Device Rating		
$SW_{MAIN} V_{MAX}$	523	V
$SW_{MAIN} I_{PK}$	0.71	A
$SW_{MAIN} I_{RMS}$	0.11	A
$D_{OUT} V_{MAX}$	160	V
$D_{OUT} I_{PK}$	1.99	A
$D_{OUT} I_{AVG}$	0.36	A

$SW_{MAIN} V_{MAX}$: Main switch max. drain-source voltage
 $SW_{MAIN} I_{PK}$: Main switch peak current
 $SW_{MAIN} I_{RMS}$: Main switch RMS current

$D_{OUT} V_{MAX}$: Output diode max. reverse voltage
 $D_{OUT} I_{PK}$: Output diode peak current
 $D_{OUT} I_{AVG}$: Output diode average current



Power Device Rating

Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design


Power Device Rating		
$SW_{MAIN} \& D_{OUT} V_{MAX}$	415	V
$SW_{MAIN} \& D_{OUT} I_{PK}$	0.77	A
$SW_{MAIN} I_{RMS}$	0.10	A
$D_{OUT} I_{AVG}$	0.15	A

$SW_{MAIN} \& D_{OUT} V_{MAX}$: Main switch & output diode max. voltage
 $SW_{MAIN} \& D_{OUT} I_{PK}$: Main switch & output diode peak current

$SW_{MAIN} I_{RMS}$: Main switch RMS current

$D_{OUT} V_{MAX}$: Output diode max. reverse voltage
 $D_{OUT} I_{PK}$: Output diode peak current
 $D_{OUT} I_{AVG}$: Output diode average current

Step 6 – Feedback Circuits



Feedback Circuit

Wide Dimming Flyback Design

Wide Dimming Buckboost Design


Wide I/O Flyback Design

Wide I/O Buckboost Design

Feedback Circuit		
Max. V_{CS} (expected)	0.57	V
Max. V_{CS} (calculated)	0.60	V
R_{CS}	0.851	Ω

Max. V_{CS} should be lower than 1.08 V current-limit.
 Higher Max. V_{CS} increases R_{CS} and n_{PS} .
 [Effect of higher n_{PS}]

- widens DCM region and reduces BCM region.
- N_S and N_A are reduced. (more margin for window area)
- higher snubber loss or higher max. voltage of switching MOSFET
- lower max. voltage of output diode



Feedback Circuit

Wide Dimming Flyback Design

Wide Dimming Buckboost Design


Wide I/O Flyback Design

Wide I/O Buckboost Design

Feedback Circuit		
Max. V_{CS}	0.56	V
R_{CS}	0.725	Ω

In buckboost design, Max. V_{CS} is not set in Feedback Circuit Section.
 [Difference from flyback design]

- For wider DCM region, reduce Max. Duty in Transformer Section.
- For more margin in the window area, reduce Max. Duty in Transformer Section.
- Max. voltage of switching MOSFET and output diode is fixed.



Feedback Circuit

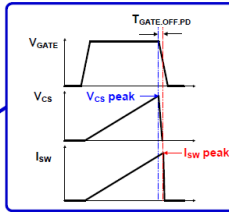
Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design

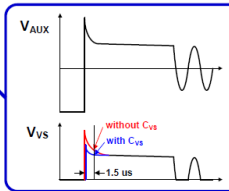
Feedback Circuit		
$T_{GATE,OFF,PD}$	90	ns
R_{COMP}	159	Ω
C_{FB}	1.0	uF
R_{VS1}	302	k Ω
R_{VS2}	38	k Ω
C_{VS}	10	pF



$T_{GATE,OFF,PD}$ is the time from V_{CS} peak to I_{SW} (Switch current) peak. I_{SW} should be measured at the node between transformer and MOSFET drain.


R_{COMP} compensates CC tolerance by line voltage change. (Line CC tolerance is caused by $T_{GATE,OFF,PD}$.)

C_{FB} is typically 1 ~ 2.2 uF. Larger C_{FB} makes slower feedback loop.



C_{VS} relieves voltage spike at gate-off. Increase C_{VS} until VS voltage at 1.5 us after gate-off is flat.

Step 7 – HOLD Circuits



HOLD Circuit

Wide Dimming Flyback Design

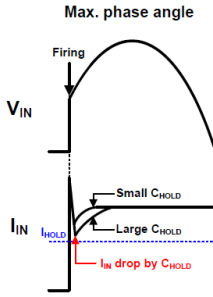
Wide Dimming Buckboost Design

Wide I/O Flyback Design

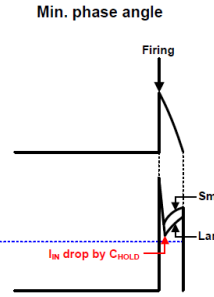
Wide I/O Buckboost Design

HOLD Circuit		
R_{HOLD}	18	k Ω
C_{HOLD}	1.0	nF

Max. phase angle



Min. phase angle



In general, C_{HOLD} is 1 ~ 5 nF.


Large C_{HOLD} has pros and cons.
 Pros : can remove LED shimmer if there is.
 Cons : input current at firing drops which can cause TRIAC mis-firing with flicker.

How to select C_{HOLD}

1. Select the worst dimmer which has the highest holding current in user's dimmer list.
2. Increase C_{HOLD} until input current drop at firing is not lower than TRIAC holding current.

(The test condition should be max. and min. phase angle, in which input current drop is the lowest.)

Step 8 – CIC Circuit



CIC Circuit

Wide Dimming Flyback Design

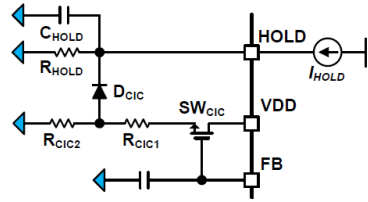
Wide Dimming Buckboost Design

Wide I/O Flyback Design


Wide I/O Buckboost Design

CIC Circuit		
R_{TCIC} (recommended)	333	k Ω
R_{TCIC} (selected)	330	k Ω
C_{TCIC}	33	nF
SW_{CIC}	2N7002	
D_{CIC}	1N4148WS	
R_{CIC1}	11.4	k Ω
R_{CIC2}	8.6	k Ω

Yield and temperature tolerance
 R_{TCIC} should be less than +/- 1%.
 C_{TCIC} should be less than +/- 5%.



FB voltage can control HOLD voltage by HOLD pull-up circuit (SW_{CIC} , D_{CIC} , R_{CIC1} and R_{CIC2}).
 When FB voltage is increased, HOLD voltage is pulled up and input current level is increased with more power delivery.



CIC Circuit

Wide Dimming Flyback Design

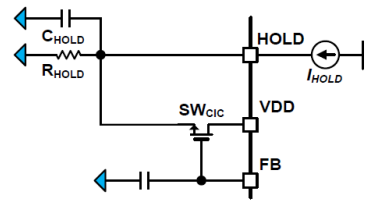
Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design


CIC Circuit		
SW_{CIC}	2N7002	

In wide I/O design, FB voltage controls HOLD voltage simply by SW_{CIC} .



In wide I/O design, FB voltage controls HOLD voltage simply by SW_{CIC} .

Step 9 – DIM Circuit



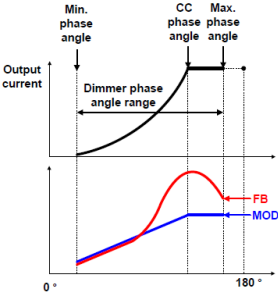
DIM Circuit

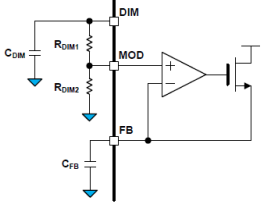
Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design






[Yield and temperature tolerance]

- R_{DIM1} and R_{DIM2} tolerance should be less than +/- 1%.

$$\left[\frac{R_{DIM2}}{R_{DIM1} + R_{DIM2}} (=r_{DIM}) \text{ selection} \right]$$

- *Max. r_{DIM} limit
- FB should not be clamped by MOD voltage at max. phase angle. (If MOD clamps FB voltage at max. phase angle, output current will be higher than the rated output current.)
- Therefore, check if FB is clamped by MOD voltage at max. phase angle condition.
- If FB is pulled up by MOD voltage, reduce r_{DIM}. (In order to reduce r_{DIM}, increase R_{DIM1} and decrease R_{DIM2}. Keep R_{DIM1} + R_{DIM2} same as design tool.)
- *Min. r_{DIM} limit
- If output current oscillation with periodic visible flicker is occurred, increase r_{DIM}.

DIM Circuit		
R _{DIM1}	24	kΩ
R _{DIM2}	90	kΩ
C _{DIM}	438	nF



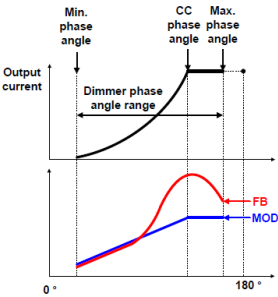
DIM Circuit

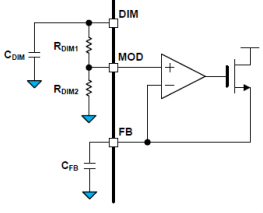
Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design





[Yield and temperature tolerance]


- R_{DIM1} and R_{DIM2} tolerance should be less than +/- 1%.

$$\left[\frac{R_{DIM2}}{R_{DIM1} + R_{DIM2}} (=r_{DIM}) \text{ selection} \right]$$

- *Max. r_{DIM} limit
- At wide I/O design, calculated r_{DIM} is low enough and FB is hardly clamped by MOD at max. phase angle condition.
- Therefore, user doesn't need to check FB clamping like wide dimming design.
- *Min. r_{DIM} limit
- At wide I/O design, there is no output current oscillation with periodic visible flicker.
- Therefore, user doesn't need to check periodic visible flicker like wide dimming design.

DIM Circuit		
R _{DIM1}	24	kΩ
R _{DIM2}	90	kΩ
C _{DIM}	438	nF

Step 10 – VIN Circuit



VIN Circuit

Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design


Wide I/O Buckboost Design

VIN Circuit		
R_{VIN1}	2.00	$M\Omega$
R_{VIN2}	106	$k\Omega$
C_{VIN}	100	μF

At high-line, R_{VIN1} is 2 Mohm.
At low-line, R_{VIN1} is 620 kohm.

C_{VIN} filters switching noise into VIN pin.

Step 11 – Bleeding Circuit



Bleeding Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design


BLD Circuit		
$C_{IN,TOTAL}$	115	nF
$C_{BLEEDER}$	68	nF
$R_{BLEEDER}$	1	k Ω
R_{RBLD}	45	Ω

Total EMI filter capacitor behind the bridge diode.
 If input voltage range is +/- 10%, user can select film capacitor for $C_{IN,TOTAL} + C_{BLEEDER}$.
 If input voltage range is +/- 15%, user needs to use around 50% of $C_{IN,TOTAL} + C_{BLEEDER}$ as MLCC. (MLCC capacitance drops at higher voltage and it will help to handle wider input voltage range.)

Total bleeder capacitor
 [$C_{BLEEDER}$ selection guidance]
 - Check input current at firing with leading edge dimmer
 - Increase $C_{BLEEDER}$ until input current drop is higher than TRIAC holding current at the firing moment.

[$R_{BLEEDER}$ selection guidance]
 - Test condition : Max./Half/Min. phase angle
 - Probe both input current and $R_{BLEEDER}$ current.
 - Find $R_{BLEEDER}$ value which minimizes input current drop at firing.

At the min. input voltage and half phase angle condition, compare the line voltage and the input voltage behind the bridge diode. After referring calculated R_{RBLD} , user needs to adjust R_{RBLD} so that the line voltage zero crossing point is close to that of the input voltage behind the bridge diode in the condition.



Bleeding Circuit

Wide Dimming Flyback Design
Wide Dimming Buckboost Design
Wide I/O Flyback Design
Wide I/O Buckboost Design

BLD Circuit		
$C_{IN,TOTAL}$	200	nF
$C_{BLEEDER}$	200	nF
$R_{BLEEDER}$	1	k Ω
Min. R_{RBLD}	20	Ω
R_{RBLD}	30	Ω

Total EMI filter capacitor behind the bridge diode.
 At wide I/O design, user doesn't need to use MLCC for $C_{IN,TOTAL}$ and $C_{BLEEDER}$ to handle wide input voltage.

Total bleeder capacitor
 [$C_{BLEEDER}$ selection guidance]
 - Check input current at firing with leading edge dimmer
 - Increase $C_{BLEEDER}$ until input current drop is higher than TRIAC holding current at the firing moment.

[$R_{BLEEDER}$ selection guidance]
 - Test condition : Max./Half/Min. phase angle
 - Probe both input current and $R_{BLEEDER}$ current.
 - Find $R_{BLEEDER}$ value which minimizes input current drop at firing.

At wide I/O design, R_{RBLD} selection is more flexible and user can increase R_{RBLD} to reduce bleeding current if bleeding switch is too hot. Once increasing R_{RBLD} , Max. I_{BLD} (upper limit) will be reduced and R_{MBLD} will be larger.



Bleeding Circuit

- Wide Dimming Flyback Design
- Wide Dimming Buckboost Design
- Wide I/O Flyback Design
- Wide I/O Buckboost Design

BLD Circuit		
Max. I_{BLD} (upper limit)	111	mA
Max. I_{BLD}	96	mA
R_{MBLD}	108	k Ω
R_{BLD}	63	Ω
R_{VDD1}	100	Ω

Max. bleeding current : Bleeding current during startup sequence and phase-cut time. Select this value lower than Max. I_{BLD} (upper limit).
 Higher Max. I_{BLD} can have more margin to maintain input current higher than holding current during startup sequence.
 Lower Max. I_{BLD} can reduce the SW_{BLD} temperature during startup sequence and AR time.

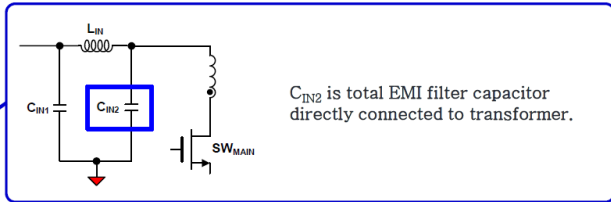
R_{VDD1} dampens leading edge spike noise into VDD pin. 100 ohm is recommended at high-line and 50 ohm is recommended at low-line.



Bleeding Circuit


- Wide Dimming Flyback Design
- Wide Dimming Buckboost Design
- Wide I/O Flyback Design
- Wide I/O Buckboost Design

BLD Circuit		
C_{IN2}	68	nF
R_{OFFSET}	28	k Ω



SRSP (sensing resistor short protection) is triggered when CS voltage is less than 0.1 V at first and second switching. When L_m is highly designed, SRSP could be abnormally triggered due to low CS peak voltage. R_{OFFSET} can protect system from abnormally triggered SRSP by building voltage offset on R_{COMP} . If CS peak is much higher than 0.1 V with small L_m , "open" message will appear and user doesn't need to add R_{OFFSET} .

Step 12 – BIAS Circuit



BIAS Circuit

- Wide Dimming Flyback Design
- Wide Dimming Buckboost Design
- Wide I/O Flyback Design
- Wide I/O Buckboost Design

BIAS Circuit		
R_{BIAS1}	2.00	$M\Omega$
R_{BIAS2}	1	$k\Omega$
C_{BIAS}	6.8	nF


At high-line, R_{BIAS1} is 2 Mohm.
At low-line, R_{BIAS1} is 620 kohm.

R_{BIAS2} protects BIAS pin from leading edge spike.
At leading edge, SW_{BLD} Crss is quickly charged and the charging current spike could damage BIAS pin due to the over voltage.

R_{BIAS2} is generally 1kohm.
When R_{BIAS2} is too small, the current spike at leading edge will affect the BIAS.
When R_{BIAS2} is too big, SW_{BLD} current regulation is unstable.

C_{BIAS} is generally 6.8 nF.
 C_{BIAS} protects BIAS pin from leading edge spike.

Step 13 – Active Damper Circuit



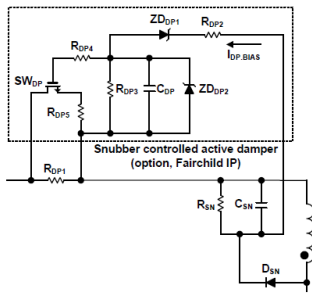
Active Damper Circuit

Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design



Active Damper Circuit		
R_DP1	500	Ω
I_DP_BIAS (max. limit)	1.3	mA
I_DP_BIAS (selected)	0.5	mA


Damper resistor

Increase resistor value until mis-firing at leading edge is disappeared.
Larger damper resistor can help to remove shimmer by stabilizing leading edge moment.
So, user can also increase this value until shimmer is removed if shimmer is shown.

If I_{DP_BIAS} is higher than this value, snubber voltage will be lower than desired snubber voltage in snubber design section.

Active damper biasing current is generally 0.3 ~ 1.0 mA.

If I_{DP_BIAS} is too low, SW_DP gate rising time becomes longer which will increase SW_DP temperature with large switching loss.



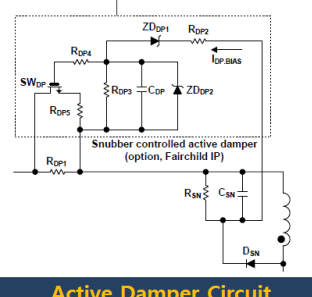
Active Damper Circuit

Wide Dimming Flyback Design

Wide Dimming Buckboost Design

Wide I/O Flyback Design

Wide I/O Buckboost Design



Active Damper Circuit		
R_DP2	240	kΩ
R_DP3	46	kΩ
R_DP4	1	kΩ
I_DP_MAX (recommended)	139	mA
I_DP_MAX (selected)	135	mA
R_DP5	24	Ω
C_DP	10.0	nF

Recommended max. active damper current limit

If I_{DP_MAX} is too large, current limit resistor (R_{DP5}) should be too small which could occur unstable SW_DP turn-on.
If I_{DP_MAX} is too small, R_{DP5} will be larger which causes larger power loss with lower efficiency.

Active damper current limit resistor

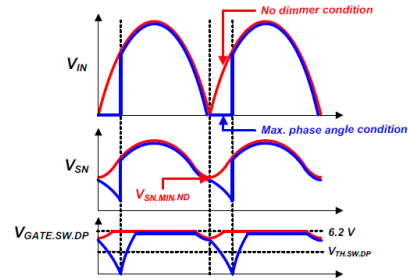
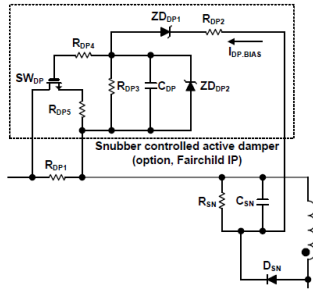
Delay capacitor for active damper switch turn-on

C_{DP} is generally 10 nF.
Check if input current ringing is almost damped after leading edge.
If SW_DP is turned on after enough damping, C_{DP} is appropriate value.



Active Damper Circuit

- Wide Dimming Flyback Design
- Wide Dimming Buckboost Design
- Wide I/O Flyback Design
- Wide I/O Buckboost Design



Active Damper Circuit		
$V_{SN_MIN_ND}$	55	V
V_{ZD_DP1}	30	V
V_{ZD_DP2}	6.2	V

Minimum snubber voltage at ND.MODE.
Enter the snubber voltage at zero crossing voltage.

V_{ZD_DP1} is generally 30 V and should be lower than $V_{SN_MIN_ND}$.
If SW_{DP} is always turned on at max. phase angle condition, increase V_{ZD_DP1} .
If SW_{DP} gate is turned off with efficiency drop at no dimmer condition, reduce V_{ZD_DP1} .

Related Resources

[FL7734 –Single-Stage Primary-Side-Regulation PWM Controller for PFC and Phase Cut Dimmable LED Driving](#)

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