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AN-4162 — Switch Node Ring Control in Synchronous Buck Regulators

Overview

To maximize system efficiency, buck regulators minimize power loss in the switching MOSFETs, inductor, capacitors, controller, and printed circuit board traces. Fairchild's FAN23xx family of synchronous buck regulators combines low $R_{DS,ON}$ MOSFETs with a driver capable of delivering fast switching speeds with short dead times in a single package. The fast switching speeds help minimize switching loss, but can contribute to voltage ringing on the switch node when the high-side MOSFET turns on. The ringing should be monitored and limited to levels that keep the MOSFET switches and controller pins within the safe operating region while meeting relevant derating guidelines.

This application note provides insight into the non-ideal circuit components that contribute to switch node ringing, along with methods that can be used to reduce ringing. Practical examples are presented to assist in the selection of components to control ringing by adding a boot resistor, snubber components, or a combination of the two. The data provided illustrates the tradeoffs between reduction in switch node ringing and efficiency.

Buck Switch Node Ringing

The need to control ringing produced by the switching of power semiconductors has existed in industry as long as semiconductor devices have been used in Switching Mode Power Supplies (SMPS). In general, the ringing must be monitored and controlled to within the datasheet limits of device voltage ratings to ensure reliable operation. The techniques to reduce and control switch-node ringing provide a secondary benefit because reduced ringing generally leads to reduced noise from the switcher that can be conducted or radiated from the power circuitry.

The non-isolated buck converter discussed in this note is a subset of the SMPS non-isolated topologies; including buck, boost, and buck-boost circuits that utilize a combination of switch/diode/inductor switching network to process power with efficient switching techniques. In high current applications, the diode is typically replaced by the low-side MOSFET and driven ON when the diode normally conducts, leading to the term "synchronous" buck converter.

Synchronous Buck Schematic with Parasitics

Figure 1 shows a FAN23xx circuit used to step down an input supply voltage to a lower output voltage to power a load; such as a system rail, I/O, memory, or bias power.

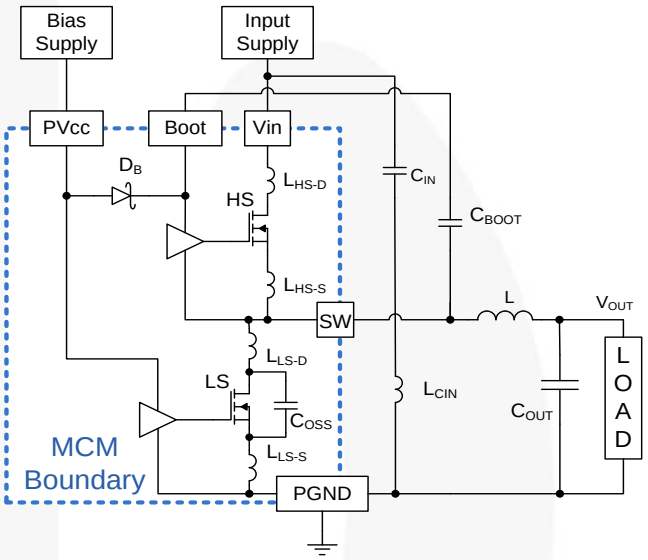

Figure 1. Synchronous Buck Circuit with Parasitic Components

The power components in the FAN23xx Multi-Chip Module (MCM) indicated by the dashed blue box include the High-Side (HS) MOSFET and Low-Side (LS) MOSFET, associated gate drive circuitry for each, and the boot diode, D_B. The junction of the MOSFETs and the output inductor is commonly referred to as the Switch (SW) Node and the voltage on the SW node is designated V_{SW}. Depending on the particular situation, the bias supply can be provided using the onboard linear regulator in the FAN23xx family members with "SV" in the name (for single-voltage operation) or supplied from an external 5 V source. The input, output, and boot capacitors and the power inductor are components external to the MCM.

In addition to the power processing components, Figure 1 shows parasitic components that play a significant role in creating the ring voltage waveform visible on the SW node.

- L_{HS-D}: parasitic inductance in series with HS drain
- L_{HS-S}: parasitic inductance in series with HS source
- C_{OSS}: parasitic output capacitance of LS MOSFET

- L_{LS-D}: parasitic inductance in series with LS drain
- L_{LS-S}: parasitic inductance in series with LS source
- L_{CIN}: parasitic inductance in series with input capacitor C_{IN}, with contributions from both the component and printed circuit board.

Synchronous Buck Switching Waveforms

Figure 2 represents steady-state operation in a buck converter operating in Continuous Conduction Mode (CCM). In this mode, the inductor current alternates between the high-side MOSFET and low-side MOSFET during each switching cycle. The cycle begins in the green interval when the LS gate is high and the low-side MOSFET is carrying the inductor current. When the LS gate signal goes LOW, the low-side MOSFET turns off and the inductor current flows through the body diode of the low-side MOSFET. After a short dead time, the high-side MOSFET is turned on and current flows to force the body diode of the low-side MOSFET off. As the body diode undergoes reverse recovery, the voltage on SW begins to rise and the ringing waveform results from the interaction of parasitic inductances and the switch node capacitance (primarily consisting of the C_{OSS} of the low-side MOSFET).

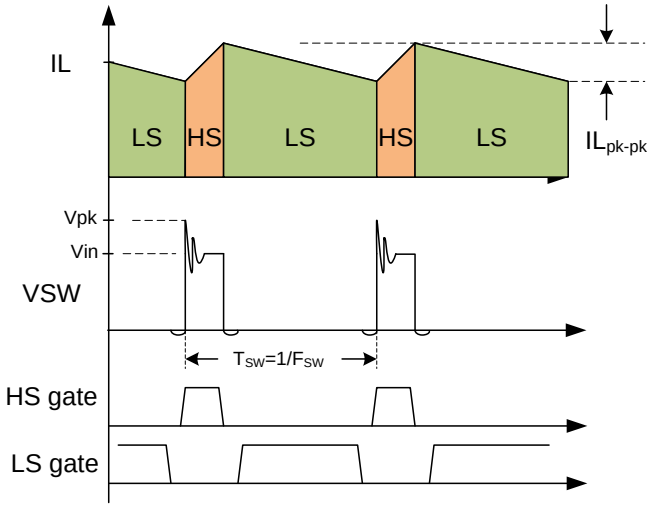

Figure 2. Synchronous Buck Steady-State Waveforms

Switch Node Probing Technique

Proper probing techniques are necessary to evaluate the switch node ringing in fast switching buck regulator circuits such as FAN23xx family. The probe must be capable of responding to very fast edge rates, on the order of a few nanoseconds, so the voltage probe should have a minimum bandwidth of 500 MHz. The circuit should be probed as close as possible to the terminals of the low-side MOSFET in the MCM package. In the FAN23xx MCM, the reference of the probe should be on PGND pins 18-21 and the probe tip should be on the SW node pins 12-17. The observed waveforms can vary significantly if the probe points move even a few millimeters from device terminals.

Figure 3 and Figure 4 show an example of probing the FAN23xx using two different oscilloscope probes. In Figure 3, the Tektronix TDP1000 1 GHz Differential Probe is shown. In Figure 4, the LeCroy PP008, 500 MHz Single-Ended Probe is used.

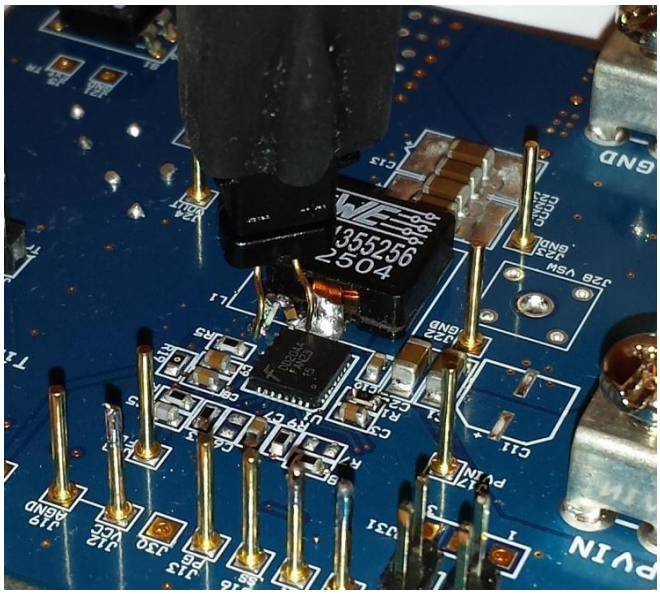

Figure 3. Probing Technique using Tektronix TDP1000

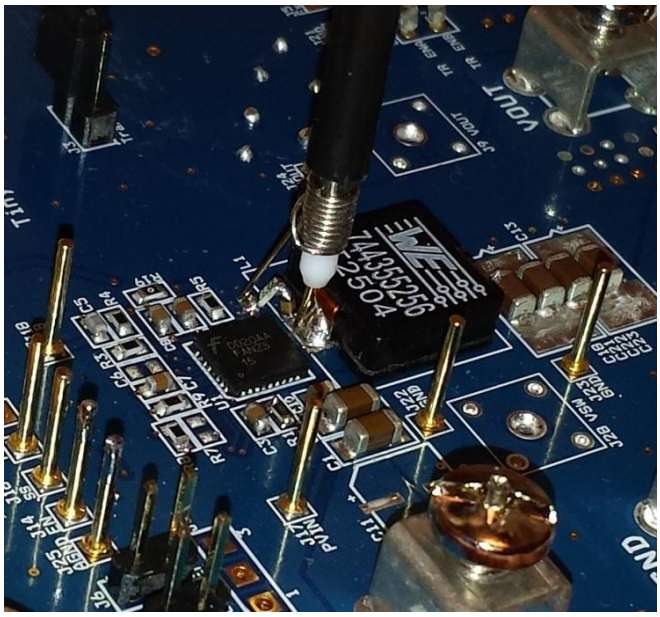

Figure 4. Probing Technique using LeCroy PP008

The differential probe is shown using the probe attachment with two short leads. With the single-ended probe, the tip cover and ground lead have been removed and the ground lead and clip have been replaced by the short ground spring installed on the lower body. In both examples, the area of the probe loop has been minimized and the probe connections made close to the MCM. Similar results were obtained when using both probe techniques.

Typical V_{SW} Waveform

Figure 5 shows an example of a typical V_{SW} waveform for the FAN2315 Synchronous Buck regulator installed on the FAN23xx evaluation board[(1)]. In the standard configuration, an input voltage rail of 12 V is converted to an output voltage of 1.2 V with a load current from 0-15 A. For the following discussion, the board is operated at the maximum recommended voltage of 15 V for FAN23xx products using 25 V MOSFETs, and the load is 15 A.

Figure 5. Switch Node Original Ring Waveform

In this waveform, the peak voltage is 24.2 V and the switch node ring frequency is 185 MHz. The peak voltage is approximately 97% of the MOSFET maximum voltage rating of 25 V. This provides only minimal margin compared to the MOSFET voltage rating of 25 V. Many corporate design guidelines recommend that the peak voltage be limited to 90% or less of the absolute maximum value. The following sections examine methods to reduce the peak V_{SW} ringing to these typical guidelines.

Methods to Reduce V_{SW} Ringing

The FAN23xx Synchronous Buck regulators have internal MOSFETs and drivers designed to work together for high system efficiency. However, in some applications, the V_{SW} ring voltage may need to be limited or reduced and there are techniques available to control the SW node ringing.

The first step is to optimize the PCB layout to reduce parasitic inductance of the primary power path, consisting of the input capacitor and switching MOSFETs. Guidelines for optimal PCB layout are included in each datasheet for the FAN23xx regulator family and are not repeated here. Second, a resistor, R_B, can be added in series with the bootstrap capacitor to slow down the turn-on transition of the high-side MOSFET, as discussed in the following section. Third, a snubber circuit can be installed from the SW node to GND to modify the SW node rise time and overshoot. This is discussed following the section on R_B.

R_B in Series with C_{BOOT}

Figure 6 shows the synchronous buck schematic with the highlighted resistor, R_B, installed in series with the bootstrap capacitor, C_{BOOT}. The voltage on C_{BOOT} allows the HS driver to provide a positive voltage from the gate to source of the HS MOSFET for turn on, then to hold the gate voltage constant as V_{SW} rises to V_{IN}. Internal to the MCM, the BOOT pin is tied to PVCC through diode D_B and, external to the MCM, the BOOT pin is connected to the more positive portion of the series combination of R_B and C_{BOOT}. The more negative terminal of C_{BOOT} is connected to the SW node. When the HS MOSFET turns off and the LS MOSFET turns on, the SW node falls to ground and C_{BOOT} is recharged through D_B.

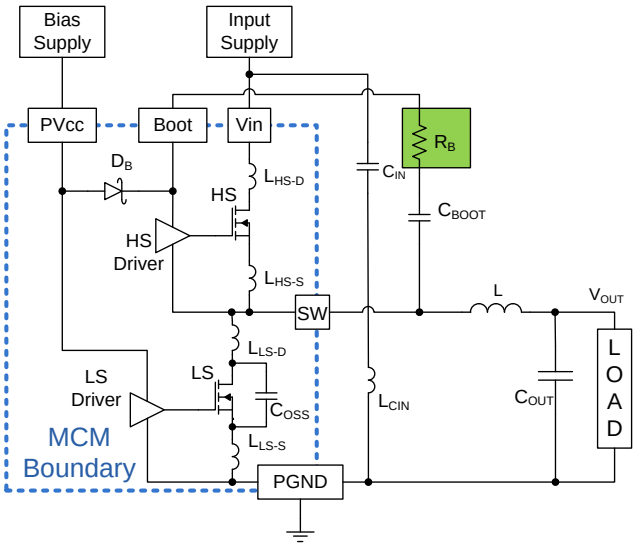

Figure 6. Boot Resistor in Series with C_{BOOT}

When the controller gives the command to turn the HS MOSFET on, the boot resistor limits the current available to charge the gate of the HS MOSFET, increasing the time needed to turn the HS MOSFET on. The increased switching time slows the SW node rate of rise and can have a significant impact on the peak voltage on the SW node.

Figure 7 shows a series of waveforms as the boot resistor is increased: 0 Ω, 1 Ω, 2.2 Ω, and 3.3 Ω. With R_B=0 Ω, the initial V_{SW} peak ring voltage is approximately 25 V and is decreased to below 20 V when R_B=3.3 Ω. As R_B is increased, the peaks and valleys of the switch node ringing are reduced while the ring frequency is relatively unchanged with each increase of the R_B value.

It should be noted that adding the boot resistor only affects the turn-on of the HS MOSFET and the associated rising edge of the SW node voltage. A similar function could be performed by moving the resistor in series with the gate of the HS MOSFET, but, in that location, the resistor reduces the switching speed for the turn-on and turn-off intervals.

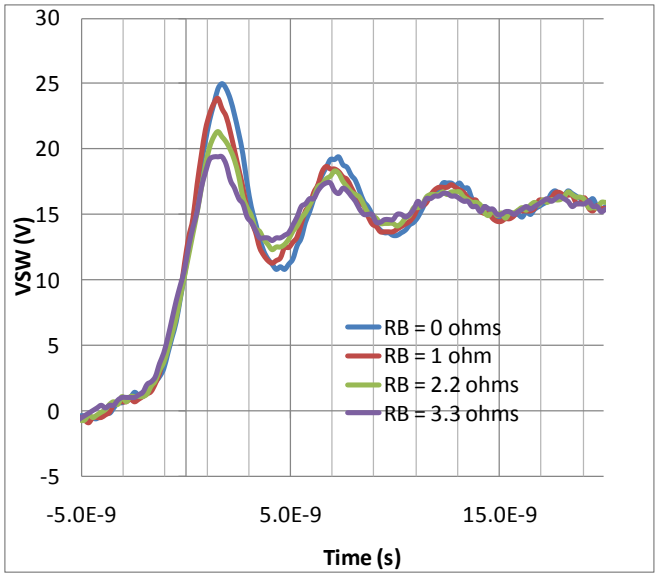

Figure 7. Effect of R_B Values on SW Ring Amplitude

Figure 8 shows an efficiency comparison with boot resistors of 0 Ω and 2.2 Ω. With R_B=2.2 Ω, the peak of the SW node voltage is <22 V, which provides a stress ratio < 90% of the MOSFET compared to the MOSFET voltage rating of 25 V. In this example, adding the boot resistor of 2.2 Ω does not cause a noticeable loss in efficiency below one-half load and only a small efficiency loss from one-half to full load.

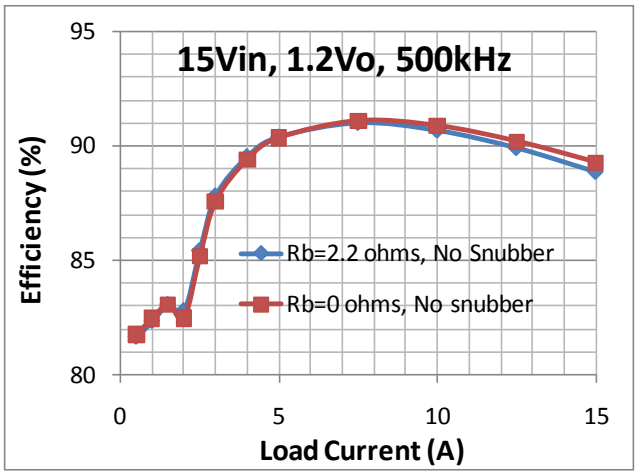

Figure 8. RB Effect on Efficiency

Considerations When Adding R_B

The addition of R_B can be used to reduce the V_{SW} ring voltage with a small impact on the total solution efficiency. However, it must be noted that adding a resistor in series with the bootstrap capacitor can introduce circuit effects beyond slowing the high-side MOSFET transition time.

For example, the voltage between the BOOT to SW pins serves as the bias power supply for the HS driver and the level-shift circuitry that transmits control information between the controller and HS gate driver. When the HS MOSFET is turned on, the current that flows from the bootstrap capacitor though R_B causes a drop in the voltage from the BOOT to SW pins. If this voltage drop is large, the voltage on the HS MOSFET gate-source is reduced, possibly leading to slow device turn-on. In applications with short on times resulting from combinations of low V_{OUT}, high V_{IN}, or high switching frequency; the internal timing of the level-shift circuitry may be affected.

For these reasons, the value of the boot resistor should be kept small and any modifications to the MOSFET drive circuitry should be tested and evaluated completely under all conditions of V_{IN}, V_{OUT}, and temperature extremes to ensure robust performance.

Snubbers

In electrical systems, the term “snubber” generally refers to a device or circuit used to suppress or “snub” voltage transients in a circuit. In this note, the term snubber refers to a series connection of a resistor and capacitor from the switch node to power ground across the LS MOSFET in a buck converter. The snubber can help control the rate of rise and fall time of the switch node voltage, while providing damping of the resonances in the parasitic components’ switching circuit.

Historical Perspective on Snubbers

There have been numerous articles and application notes concerning the use of snubbers to modify the behavior of switching circuits. Many of the earlier references were focused on offline power converters utilizing components in packages much larger than the packages in modern synchronous buck converters. In these publications, the circuit is treated as a second-order system and the snubber components are selected to damp the resonances of parasitic components in the power stage. In integrated buck regulators, the techniques are still useful, but careful attention is required to minimize total circuit losses to maintain high efficiency.

William McMurray authored a classic paper [2] that provided a framework for the selection of snubber components to either minimize voltage overshoot compared to the input voltage or to control the dv/dt (volts per second) to a minimum value. In subsequent work[3], Rudy Severns described a method for a quick snubber design technique and provided a practical example of an optimized snubber using the methods of McMurray. Philip C. Todd provided an extensive treatment of snubbers[4], including dissipative snubbers, such as the resistor-capacitor utilized to control switch node ringing and the class of non-dissipative snubbers that use resonant techniques to recycle stored energy to the input or output voltage rails to reduce the energy lost in the power switching process.

Yen-Ming Chen presents a thorough review[5] of the design and use of snubbers using the second-order approximation of preceding authors. This work includes an investigation into the validity of the second-order approximation using simulation and bench testing and shows that higher-order effects make different analysis techniques applicable. These higher-order effects arise due to the multiple resonant paths visible in the buck converter schematic, leading to

introduction of the Root-Loci approach for snubber optimization in buck converters.

This application note shows how snubbers fit in the designer's toolkit to help control switch node ringing, while keeping an eye on the resultant power loss. The second-order approximation is used to make the initial snubber component selections and lab data is provided to illustrate the tradeoffs when using different values of snubber capacitors and resistors.

Snubber Circuit Schematic

Figure 9 shows the connection of snubber components R_{SN} and C_{SN} in the schematic for the FAN23xx synchronous buck regulator schematic.

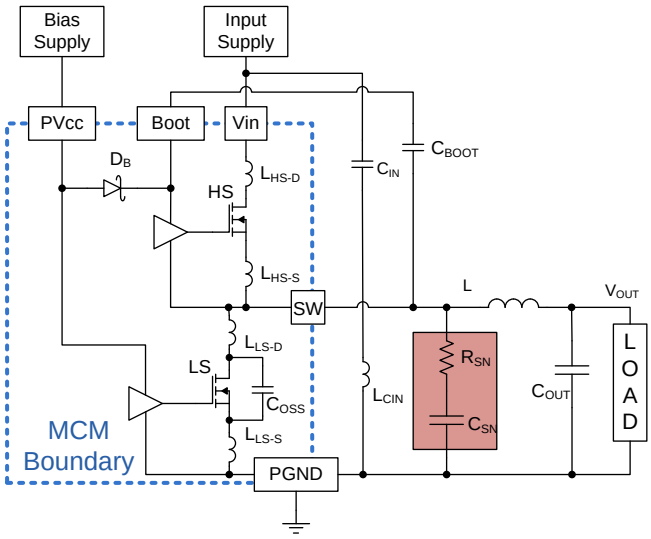

Figure 9. Circuit with Added R-C Snubber

In the typical application of the second-order approximation for snubber design as summarized by Chen[5], the snubber resistor value is selected to have an impedance similar in magnitude to the impedance of the power circuit parasitic components to be damped. The snubber capacitor value is selected to have a value slightly larger than the parasitic capacitance in the power circuit but constrained in value by practical limits related to power loss and component size requirements. In practical circuits, the snubber components are evaluated empirically using a procedure such as the one presented in the following paragraphs.

Determine Snubber Component Values

The following steps provide general guidelines to help select and apply snubber circuits using empirical methods:

1. Estimate parasitic circuit inductance
2. Estimate parasitic switch node capacitance
3. Determine snubber resistor value
4. Select initial snubber capacitor value

To determine an effective value for the snubber resistor, the approximate values of the parasitic inductance and capacitance of the switch node requires evaluation.

Estimate Parasitic Inductance

To estimate the parasitic inductance in series with the switch node, two waveform measurements are required. First, the initial ring frequency of the switch node with no added components is measured. Next, an external capacitor is attached from switch node to ground to reduce the ring frequency by approximately 50% and the measurement of ring frequency is repeated. The change in the period of the resonant ring frequency when changing from the original capacitance C_{SW} to $C_{SW}+C_{EXT}$ determines the parasitic inductance using the following procedure:

The natural resonant frequency of the L-C circuit can be expressed in radians per second ω_n and Hertz f_n as:

$$\omega_n = \frac{1}{\sqrt{L_p C_{SW}}} \quad (1)$$

$$f_n = \frac{1}{2\pi\sqrt{L_p C_{SW}}} \quad (2)$$

where L_p=parasitic inductance and C_{SW}=capacitance of switch node with no external capacitor attached.

The equation can be manipulated to provide an expression for the period (squared) of the resonant ring interval with no external capacitance:

$$T_1^2 = 4\pi^2 L_p C_{SW} \quad (3)$$

In a similar fashion, the resonant ring interval with added external capacitance can be expressed as:

$$T_2^2 = 4\pi^2 L_p (C_{SW} + C_{EXT}) \quad (4)$$

Subtracting Equation (3) from Equation (4) yields an expression[3] that calculates L_P in Equation (5):

$$L_p = \frac{T_2^2 - T_1^2}{4\pi^2 C_{EXT}} \quad (5)$$

These equations are applied to evaluate the parasitic inductance for the circuit used to produce the waveform in Figure 4, in which the cursor measurement shows the initial ring frequency is 185 MHz with no external capacitance on the switch node, resulting ring period T1=5.4 ns.

Figure 10 shows the V_{SW} waveform after C_{EXT}=2.2 nF is added to the switch node, in parallel with the drain and source of the LS MOSFET. This capacitor is installed on the top side of the PCB in close proximity to the MCM.

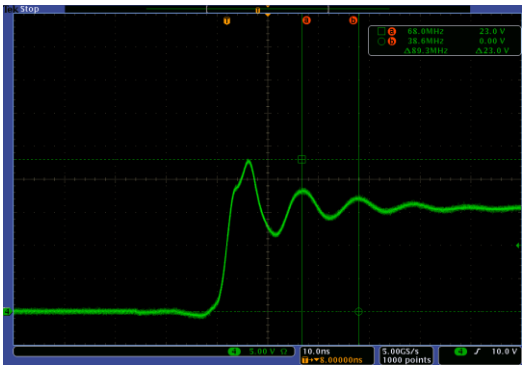

Figure 10. V_{SW} with Parallel 2.2 nF Capacitor Added

In this waveform, the peak ring voltage is reduced from 24.2 V to 23 V and the ring frequency has reduced from 185 MHz to 89 MHz, resulting in a ring period for T2=11.2 ns. There is an inflection visible near the peak of the initial ring, indicating there may be additional frequency components involved in the observed waveform. Plugging the values for T2, T1, and C_{EXT} into Equation (5) allows calculation for the parasitic inductance.

$$L_p = \frac{(11.2ns)^2-(5.4ns)^2}{4\pi^2(2.2nF)} = 1.1\text{nH}$$

This parasitic inductance value of 1.1 nH is used to calculate values for the snubber components.

Estimate Parasitic Switch Node Capacitance

The primary component of switch node capacitance C_{SW} is C_{OSS} of the LS MOSFET, in addition to other parasitic components. The following procedure does not require that the value of C_{OSS} be known and yields an estimate of the total C_{SW}. After the parasitic inductance is known, the estimated switch node capacitance can be evaluated by rearranging Equation (2).

$$C_{SW} \sim \frac{1}{4\pi^2 \cdot 1.1nH \cdot (185MHz)^2} = 673pF$$

Calculate Snubber Resistor Value/Size

The snubber resistor value is selected to ensure the damping ratio is close to unity for fast rise time with minimal overshoot. The damping ratio ζ is given by:

$$\zeta = \frac{1}{(R_{SN})2}\sqrt{\frac{L_p}{C_{SW}}} \quad (6)$$

Setting ζ=1 the value for the snubber resistor can be calculated as:

$$R_{Sn} = \frac{1}{2}\sqrt{\frac{L_p}{C_{SW}}} = \frac{1}{2}\sqrt{\frac{1.1nH}{673pF}} = 0.64\,\Omega \quad (7)$$

The resistor must charge and discharge the snubber capacitor in each switching cycle. Therefore, the power dissipated in the resistor can be calculated as:

$$P_{R_{SN}} = f_{SW} C_{SN} V_{SW}^2 \quad (8)$$

Determine Snubber Capacitor Value and Size

The snubber capacitor value should be selected with consideration of the engineering tradeoffs between controlling the switch node ringing and the power loss associated with larger capacitor size. The snubber capacitor should be larger than the circuit capacitance to be snubbed; often selected to be two to three times the value of the calculated parasitic capacitance. Using the calculated C_{SW} value of 673 pF, the snubber capacitor is evaluated using this guideline. Test data is presented using 1200 pF and 2.2 nF.

Snubber Test Data

Figure 11 includes both the original switch node ring waveform and the waveform using the calculated snubber (2.2 nF plus 0.68 Ω).

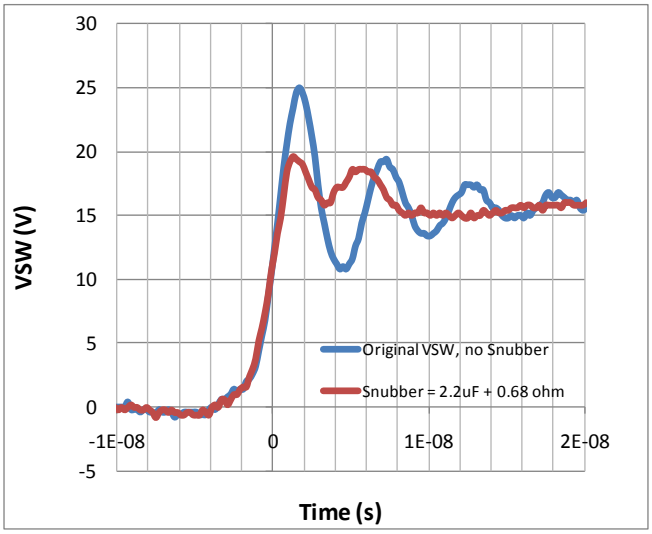

Figure 11. Snubber Effect on Switch Node

The snubber reduces the V_{SW} ring waveform below 20 V, which provides a stress rating slightly below 80% of the 25 V maximum rating of the MOSFETs. In this 500 kHz application operating in continuous conduction mode, the loss in the snubber is approximately 0.25 W during each switching cycle. To ensure that a resistor can handle the calculated power without excessive temperature rise, the selected package should be capable of dissipating a power equal to twice the calculated value.

In the data presented, the snubber is populated on the top (component) side of the PCB in close proximity to the FAN23xx MCM using a bridge connection, as shown in Figure 12. This snubber placement helps minimize the higher-order effects added because of the inductance through vias. Via inductance is often considered to be on the order of a few nH, but the actual via inductance is a complicated function of the PCB structure[6].

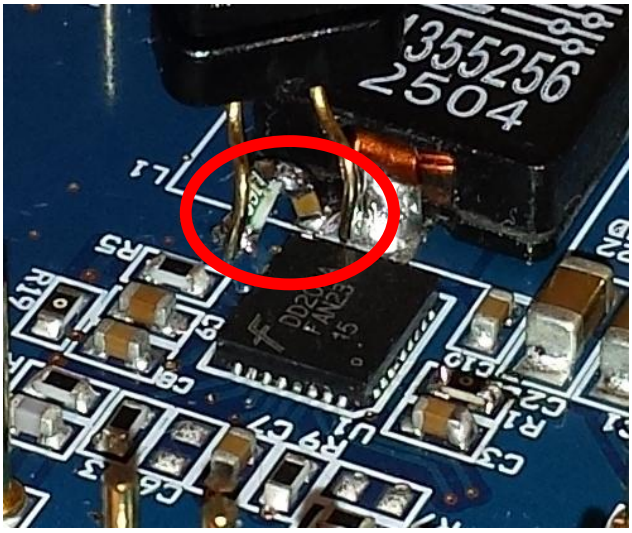

Figure 12. Snubber Installed Close to MCM

To verify performance of the selected damping resistance, the resistor value is varied from 0.47 Ω to 3.3 Ω with the snubber capacitor held constant at 2.2 nF. Figure 13 shows that for resistor values ≥ 1 Ω, the peak voltage is greater than that found using R_{SN}=0.68 Ω. With R_{SN}=0.47 Ω, the first voltage peak is less that the second voltage peak. This indicates that the value of 0.68 Ω is close to the maximally damped condition. Even though the V_{SW} ring characteristic changes, the snubber power loss is relatively constant because it is based on capacitor value, not the resistor value.

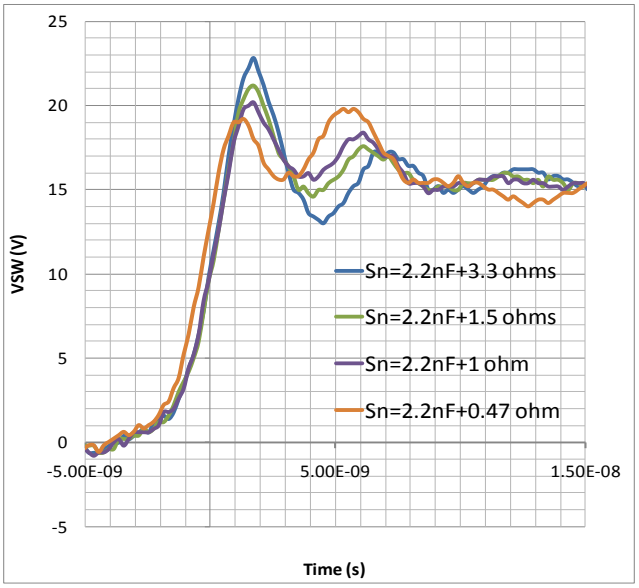

Figure 13. Snubber Resistor Varied with C_{SN}=2.2 nF

In the preceding example, the snubber capacitor is selected as 2.2 nF. It is important to consider the effect the snubber has on efficiency and to reduce the capacitor value and associated power loss to as small a value as possible. The following data includes snubber capacitor values of 2.2 nF and 1.2 nF. The 1.2 nF snubber capacitor introduces a power loss of 0.14 W; approximately one-half the loss contributed by the 2.2 nF snubber.

Figure 14 shows the converter efficiency with V_{IN}=15 V using three different configurations:

1. No snubber installed (top trace)
2. Snubber = 1.2nF + 0.68 Ω (middle trace)
3. Snubber = 2.2nF + 0.68 Ω (bottom trace)

With no snubber installed, the efficiency is highest and reaches a peak efficiency of 91% at one-half load (7.5 A). The middle curve shows the efficiency with the snubber capacitor reduced to 1.2 nF is 90% at 7.5 A. When the snubber with 2.2 nF is installed, the efficiency in the bottom curve is 89% at 7.5 A. These curves indicate the gradual loss in efficiency that can be expected with increasing the snubber capacitor size.

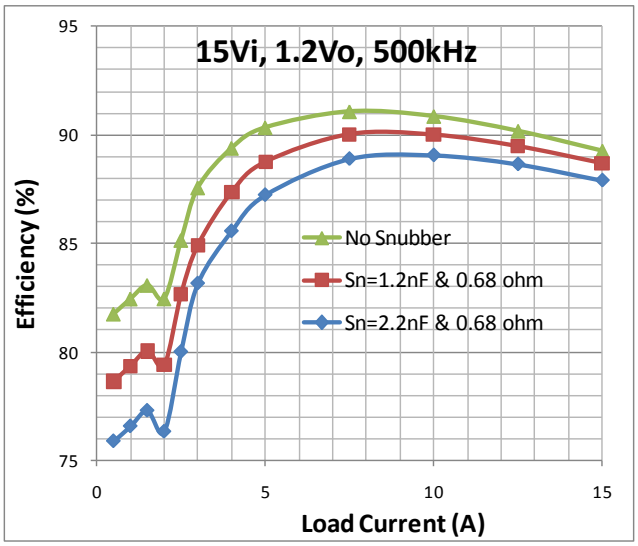

Figure 14. Efficiency Comparing Three Snubber Configurations

With the 1.2 nF snubber capacitor offering expected efficiency improvement, it is necessary to evaluate the effect of the reduced capacitance on snubber performance. Figure 15 shows the changes in the V_{SW} ring waveform as the snubber capacitor is reduced from 2.2 nF to 1.2 nF. The peak V_{SW} voltage increases slightly, but remains below 22 V to provide a stress ratio below 90%.

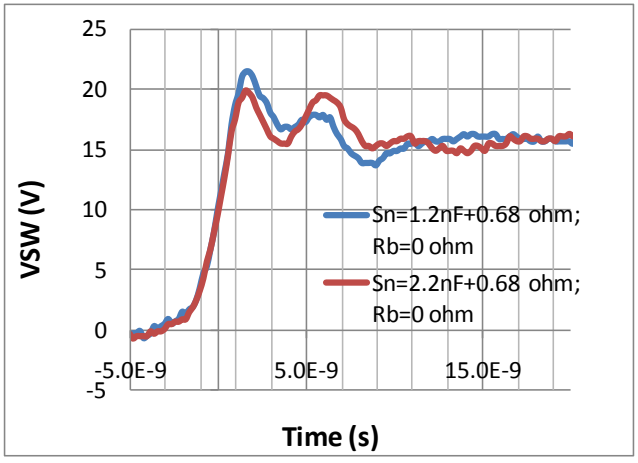

Figure 15. Comparison of Snubber, Two Capacitor Values

As a final step in selecting the best solution for a particular application, a boot resistor is combined with the smaller snubber capacitor of 1.2 nF. Figure 16 shows the combination of the snubber with a 1.2 nF capacitor with R_B=1 Ω.

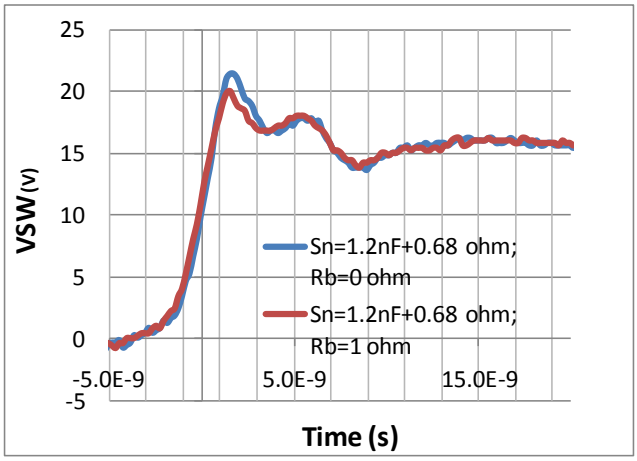

Figure 16. Small Snubber with / without R_B

The initial V_{SW} ring bump is reduced to below 20 V, while the second bump is not noticeably changed.

It is worthwhile to compare the V_{SW} waveforms of the 2.2 nF, 0.68 Ω snubber to the 1.2 nF, 0.68 Ω snubber with R_B=1 Ω, as shown in Figure 18. These waveforms show that using the smaller capacitor in conjunction with R_B=1 Ω can limit the peak V_{SW} voltage ≤ 20 V in a similar manner to the larger 2.2 nF snubber capacitor.

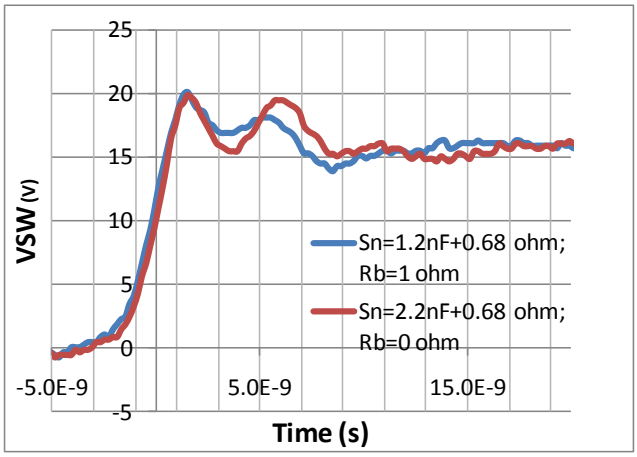

Figure 17. Two Configurations of Snubber and R_B

With the V_{SW} voltage of 20 V, it is useful to check the efficiency with the snubber of 1.2 nF + 0.68 Ω, using R_B=1 Ω. As shown in Figure 18, there is very minimal loss in efficiency with R_B=1 Ω.

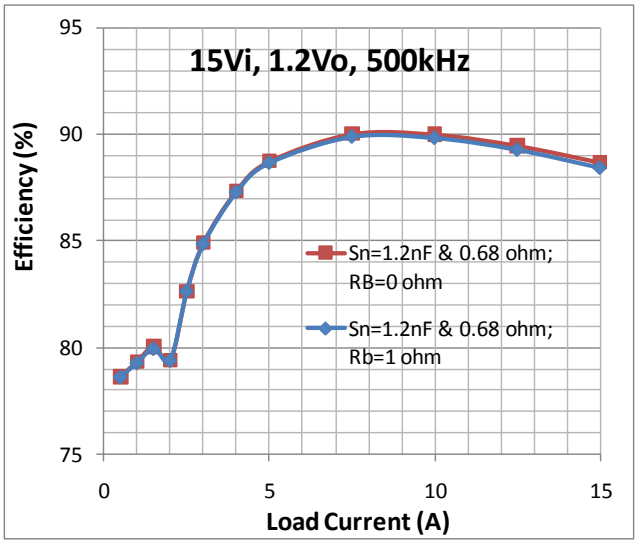

Figure 18. Efficiency Comparing Snubber with / without Small R_B

Summary

The design engineer has several tools available to help address switch node voltage ringing. First, the PCB should be optimized such that component placement provides the minimal circuit area and trace lengths. If careful probing shows that the switch node ringing is higher than desired; circuit modifications, such as a boot resistor and/or a snubber circuit, can be added to limit the V_{SW} ringing to acceptable levels.

This application note shows that a boot resistor can be used to reduce the amplitude of V_{SW} ringing with relatively small impact on converter efficiency. However, R_B does not reduce the frequency of the switch node ring waveform, which may be needed to address EMI issues.

In situations where additional switch node ring control is needed, a snubber can be added to reduce both the amplitude and the ring frequency found on V_{SW}. Guidelines are provided to select snubber components and to highlight the effects of different snubber component values on the V_{SW} ring voltage and efficiency of a typical buck regulator.

Related Product Resources

FAN2315 — 15 A Synchronous Buck Regulator

References

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[5] *Yen-Ming Chen, "RC Snubber Design using Root-Loci Approach for Synchronous Buck SMPS," http://www.collectionscanada.gc.ca/obj/s4/f2/dsk3/OWTU/TC-OWTU-526.pdf.*

[6] *Dr. Howard Johnson, Via Inductance, article published by Signal Consulting Inc, http://www.sigcon.com/Pubs/news/6_04.htm.*

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