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# Application Note AN4149

## Design Guidelines for Quasi-Resonant Converters Using KA5Q-series Fairchild Power Switch (FPS™)

### Abstract

In general, a Quasi-Resonant Converter (QRC) shows lower EMI and higher power conversion efficiency compared to the conventional hard switched converter with a fixed switching frequency. Therefore, it is well suited for color TV applications that are noise sensitive. This application note presents practical design considerations of Quasi-Resonant

Converters for color TV applications employing KA5Q-series FPS™ (Fairchild Power Switch). It includes designing the transformer, output filter and sync network, selecting the components and closing the feedback loop. The step-by-step design procedure described in this application note will help engineers design quasi-resonant converter easily.

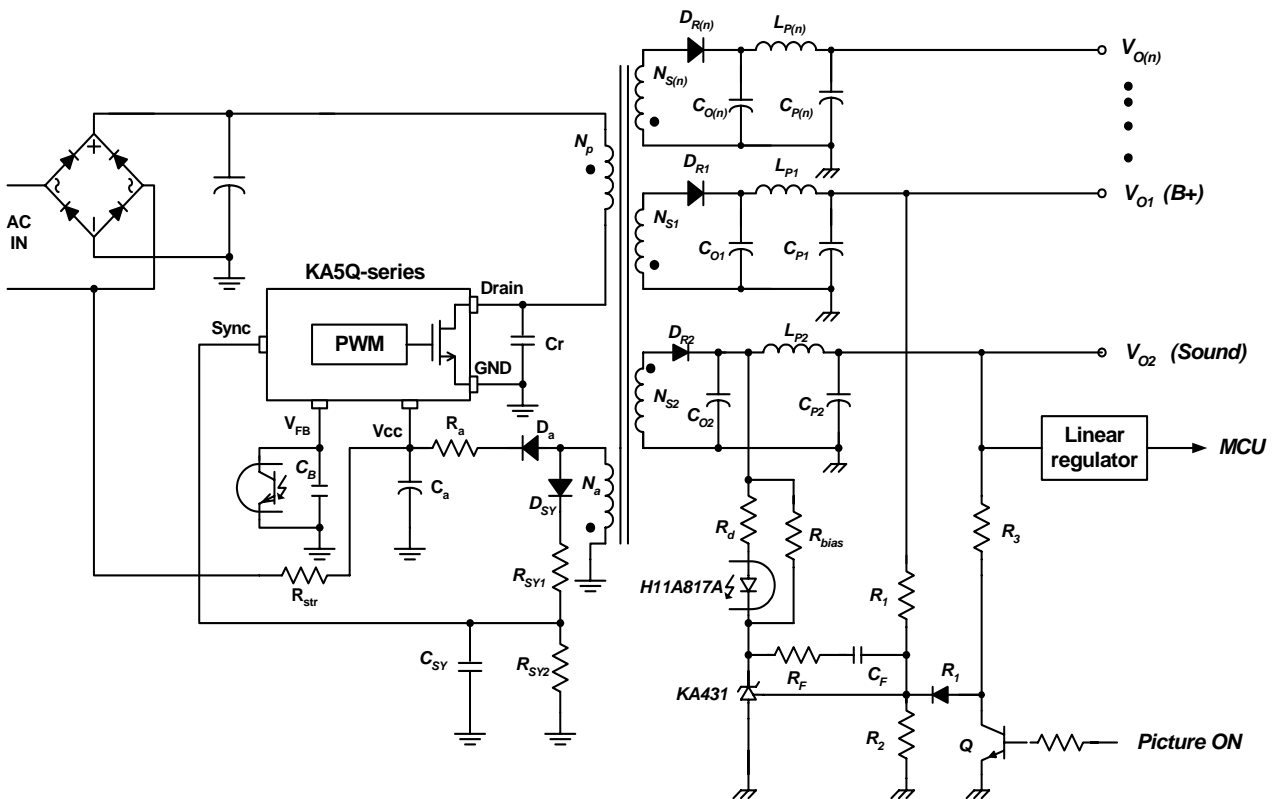


Figure 1. Basic Quasi Resonant Converter Using KA5Q-series (Color TV Application)

### 1. Introduction

The KA5Q-series FPS™ (Fairchild Power Switch) is an integrated Pulse Width Modulation (PWM) controller and a Sense FET specifically designed for quasi-resonant off-line Switch Mode Power Supplies (SMPS) with minimal external components. Compared with a discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight while simultaneously increasing efficiency,

system reliability and productivity.

Figure 1 shows the basic schematic of a quasi-resonant converter using KA5Q-series for the color TV application, which also serves as the reference circuit for the design process described in this paper.  $V_{01}$  is the output voltage that powers horizontal deflection circuit while  $V_{02}$  is the output voltage that supplies power to the Micro Controller Unit (MCU) through a linear regulator.

## 2. Step-by-step Design Procedure

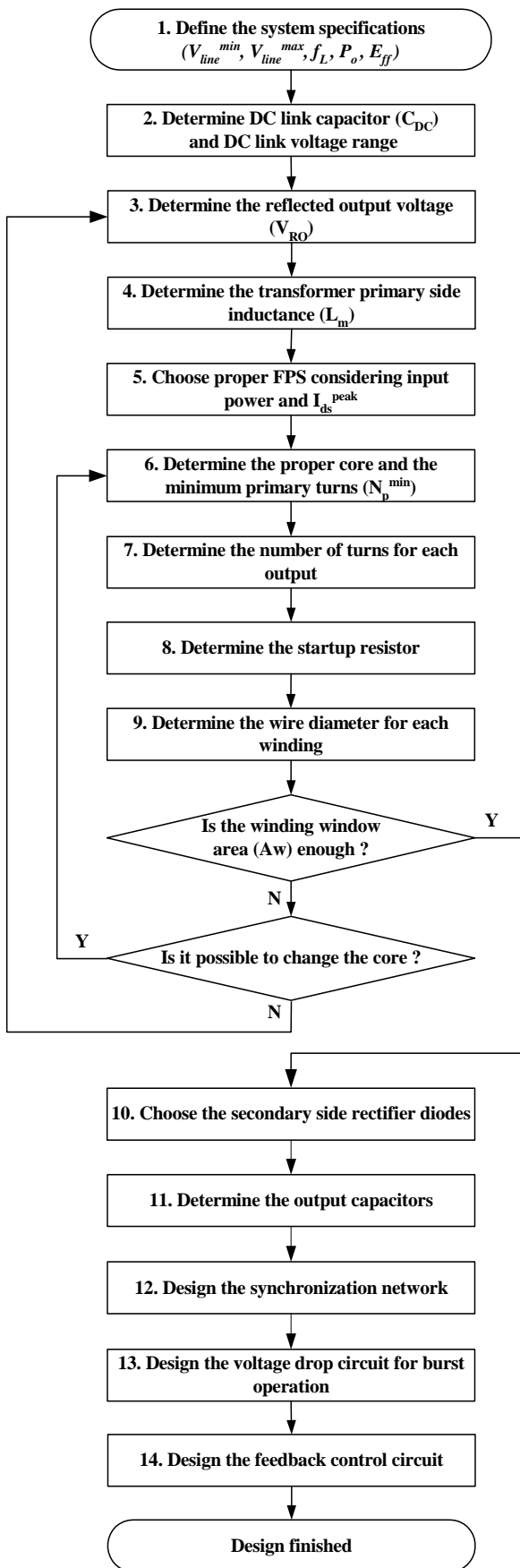


Figure 2. Flow Chart of Design Procedure

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. Figure 2 illustrates the design flow chart. The detailed design procedures are as follows:

### [STEP-1] Define the system specifications

- Line voltage range ( $V_{line}^{min}$  and  $V_{line}^{max}$ ).
- Line frequency ( $f_L$ ).
- Maximum output power ( $P_o$ ).
- Estimated efficiency ( $E_{ff}$ ): The power conversion efficiency must be estimated to calculate the maximum input power. If no reference data is available, set  $E_{ff} = 0.7\sim 0.75$  for low voltage output applications and  $E_{ff} = 0.8\sim 0.85$  for high voltage output applications. In the case of Color TV applications, the typical efficiency is 80~83%.

With the estimated efficiency, the maximum input power is given by

$$P_{in} = \frac{P_o}{E_{ff}} \quad (1)$$

For multiple output SMPS, the load occupying factor for each output is defined as

$$K_{L(n)} = \frac{P_{o(n)}}{P_o} \quad (2)$$

where  $P_{o(n)}$  is the maximum output power for the n-th output. For single output SMPS,  $K_{L(1)}=1$ . It is assumed that  $V_{o1}$  is the reference output that is regulated by the feedback control in normal operation.

### [STEP-2] Determine DC link capacitor ( $C_{DC}$ ) and the DC link voltage range.

It is typical to select the DC link capacitor as 2-3uF per watt of input power for universal input range (85-265Vrms) and 1uF per watt of input power for European input range (195V-265Vrms). With the DC link capacitor chosen, the minimum DC link voltage is obtained as

$$V_{DC}^{min} = \sqrt{2 \cdot (V_{line}^{min})^2 - \frac{P_{in} \cdot (1 - D_{ch})}{C_{DC} \cdot f_L}} \quad (3)$$

where  $C_{DC}$  is the DC link capacitor and  $D_{ch}$  is the duty cycle ratio for  $C_{DC}$  to be charged as defined in Figure 3, which is typically about 0.2.  $P_{in}$ ,  $V_{line}^{min}$  and  $f_L$  are specified in STEP-1.

The maximum DC link voltage is given as

$$V_{DC}^{max} = \sqrt{2} V_{line}^{max} \quad (4)$$

where  $V_{line}^{max}$  is specified in STEP-1.

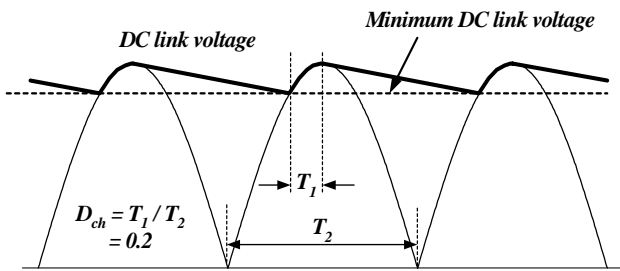


Figure 3. DC Link Voltage Waveform

**[STEP-3] Determine the reflected output voltage ( $V_{RO}$ )**

Figure 4 shows the typical waveforms of the drain voltage of quasi-resonant flyback converter. When the MOSFET is turned off, the DC link voltage ( $V_{DC}$ ) together with the output voltage reflected to the primary ( $V_{RO}$ ) are imposed on the MOSFET. The maximum nominal voltage across the MOSFET ( $V_{ds}^{nom}$ ) is

$$V_{ds}^{nom} = V_{DC}^{max} + V_{RO} \tag{5}$$

where  $V_{DC}^{max}$  is as specified in equation (4). By increasing  $V_{RO}$ , the capacitive switching loss and conduction loss of the MOSFET are reduced. However, this increases the voltage stress on the MOSFET as shown in Figure 4. Therefore, determine  $V_{RO}$  by a trade-off between the voltage margin of the MOSFET and the efficiency. Typically,  $V_{RO}$  is set as 120~180V so that  $V_{ds}^{norm}$  is 490~550V (75~85% of MOSFET rated voltage).

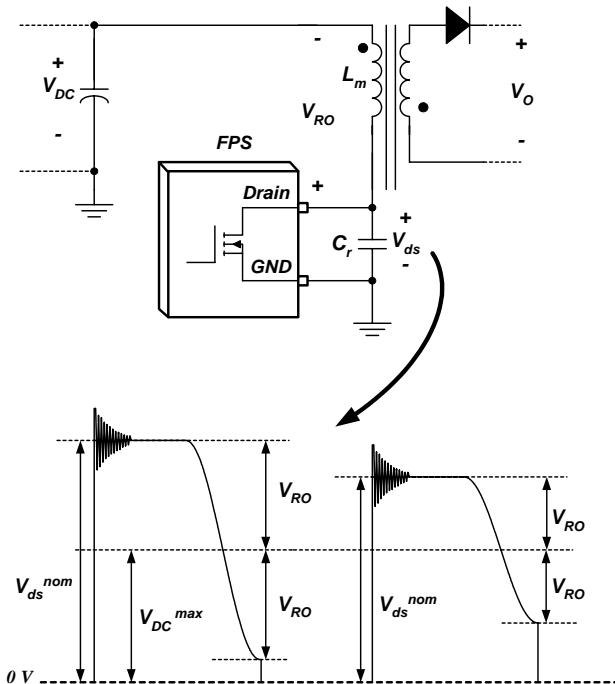


Figure 4. The Typical Waveform of MOSFET Drain Voltage for Quasi Resonant Converter

**[STEP-4] Determine the transformer primary side inductance ( $L_m$ )**

Figure 5 shows the typical waveforms of MOSFET drain current, secondary diode current and the MOSFET drain voltage of a Quasi Resonant Converter. During  $T_{OFF}$ , the current flows through the secondary side rectifier diode and the MOSFET drain voltage is clamped at  $(V_{DC}+V_{RO})$ . When the secondary side current reduces to zero, the drain voltage begins to drop by the resonance between the effective output capacitor of the MOSFET and the primary side inductance ( $L_m$ ). In order to minimize the switching loss, the KA5Q-series is designed to turn on the MOSFET when the drain voltage reaches its minimum voltage ( $V_{DC}-V_{RO}$ ).

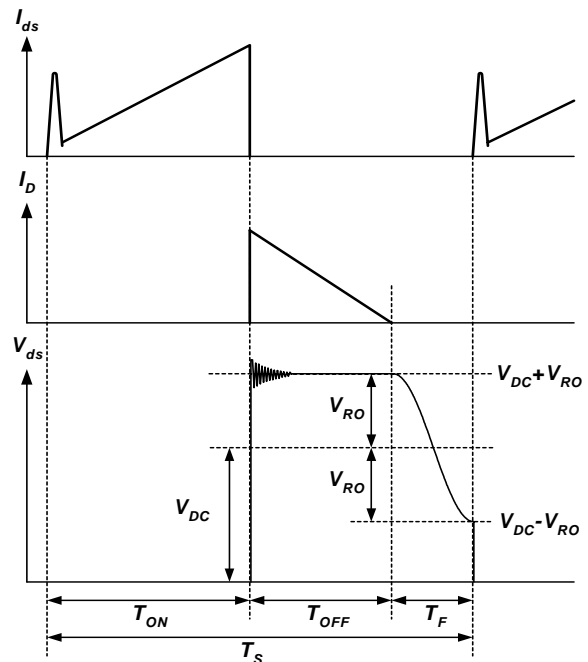


Figure 5. Typical Waveforms of Quasi-Resonant Converter

To determine the primary side inductance ( $L_m$ ), the following variables should be determined beforehand :

- **The minimum switching frequency ( $f_s^{min}$ ) :** The minimum switching frequency occurs at the minimum input voltage and full load condition and should be higher than the minimum switching frequency of FPS (20kHz). By increasing  $f_s^{min}$ , the transformer size can be reduced. However, this results in increased switching losses. Therefore, determine  $f_s^{min}$  by a trade-off between switching losses and transformer size. It is typical to set  $f_s^{min}$  to be around 25kHz.
- **The falling time of the MOSFET drain voltage ( $T_F$ ) :** As shown in Figure 5, the MOSFET drain voltage fall time is half of the resonant period of the MOSFET's effective output capacitance and primary side inductance. By increasing  $T_F$ , EMI can be reduced. However, this forces an increase of the resonant capacitor ( $Cr$ ) resulting in increased switching losses. The typical value for  $T_F$  is 2-2.5us.

After determining  $f_s^{min}$  and  $T_F$ , the maximum duty cycle is calculated as

$$D_{max} = \frac{V_{RO}}{V_{RO} + V_{DC}^{min}} \cdot (1 - f_s^{min} \times T_F) \quad (6)$$

where  $V_{DC}^{min}$  is specified in equation (3) and  $V_{RO}$  is determined in STEP-3.

Then, the primary side inductance is obtained as

$$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2 \cdot f_s^{min} \cdot P_{in}} \quad (7)$$

where  $P_{in}$ ,  $V_{DC}^{min}$  and  $D_{max}$  are specified in equations (1), (3), and (6), respectively and  $f_s^{min}$  is the minimum switching frequency.

Once  $L_m$  is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as

$$I_{ds}^{peak} = \frac{V_{DC}^{min} \cdot D_{max}}{L_m \cdot f_s^{min}} \quad (8)$$

$$I_{ds}^{rms} = \sqrt{\frac{D_{max}}{3}} \cdot I_{ds}^{peak} \quad (9)$$

where  $V_{DC}^{min}$ ,  $D_{max}$  and  $L_m$  are specified in equations (3), (6) and (7), respectively and  $f_s^{min}$  is the minimum switching frequency.

#### [STEP-5] Choose the proper FPS considering input power and peak drain current.

With the resulting maximum peak drain current of the MOSFET ( $I_{ds}^{peak}$ ) from equation (8), choose the proper FPS whose pulse-by-pulse current limit level ( $I_{LIM}$ ) is higher than  $I_{ds}^{peak}$ . Since FPS has  $\pm 12\%$  tolerance of  $I_{LIM}$ , there should be some margin for  $I_{LIM}$  when choosing the proper FPS device. Table 1 shows the lineups of KA5Q-series with rated output power and pulse-by-pulse current limit.

Maximum Output Power					
PRODUCT	230Vac $\pm 15\%$	85~ 265Vac	$I_{LIM}$		
			Min	Typ	Max
KA5Q0740RT	90 W (85~170Vac)		4.4A	5A	5.6A
KA5Q0565RT	75 W	60 W	3.08A	3.5A	3.92A
KA5Q0765RT	100 W	85 W	4.4A	5A	5.6A
KA5Q1265RT	150 W	120 W	5.28A	6A	6.72A
KA5Q1265RF	210 W	170 W	7.04A	8A	8.96A
KA5Q1565RF	250 W	210 W	10.12A	11.5A	12.88A

Table 1. FPS Lineups with Rated Output Power

#### [STEP-6] Determine the proper core and the minimum primary turns.

Table 2 shows the commonly used cores for C-TV application for different output powers. When designing the transformer, consider the maximum flux density swing in normal operation ( $\Delta B$ ) as well as the maximum flux density in transient ( $B_{max}$ ). The the maximum flux density swing in normal operation is related to the hysteresis loss in the core while the maximum flux density in transient is related to the core saturation.

With the chosen core, the minimum number of turns for the transformer primary side to avoid the over temperature in the core is given by

$$N_p^{min} = \frac{L_m I_{ds}^{peak}}{\Delta B A_e} \times 10^6 \quad (10)$$

where  $L_m$  is specified in equation (7),  $I_{ds}^{peak}$  is the peak drain current specified in equation (8),  $A_e$  is the cross-sectional area of the transformer core in  $\text{mm}^2$  as shown in Figure 6 and  $\Delta B$  is the maximum flux density swing in tesla. If there is no reference data, use  $\Delta B = 0.25 \sim 0.30$  T.

Since the MOSFET drain current exceeds  $I_{ds}^{peak}$  and reaches  $I_{LIM}$  in a transient or fault condition, the transformer should be designed not to be saturated when the MOSFET drain current reaches  $I_{LIM}$ . Therefore, the maximum flux density ( $B_{max}$ ) when drain current reaches  $I_{LIM}$  should be also considered as

$$N_p^{min} = \frac{L_m I_{LIM}}{B_{max} A_e} \times 10^6 \quad (11)$$

where  $L_m$  is specified in equation (7),  $I_{LIM}$  is the pulse-by-pulse current limit,  $A_e$  is the cross-sectional area of the core in  $\text{mm}^2$  as shown in Figure 6 and  $B_{max}$  is the maximum flux density in tesla. Figure 7 shows the typical characteristics of ferrite core from TDK (PC40). Since the core is saturated at low flux density as the temperature goes high, consider the high temperature characteristics. If there is no reference data, use  $B_{max} = 0.35 \sim 0.4$  T.

The primary turns should be determined as less than  $N_p^{min}$  values obtained from equation (10) and (11).

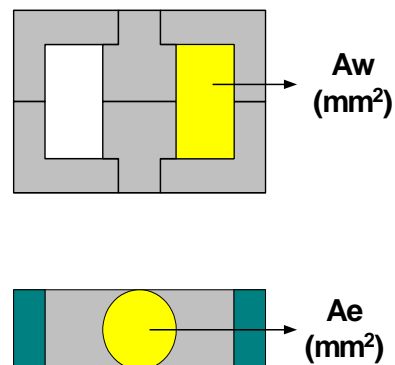


Figure 6. Window Area and Cross Sectional Area

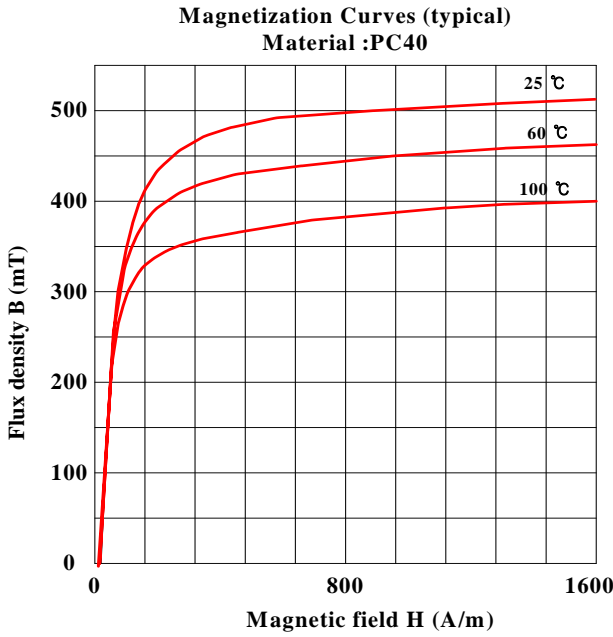


Figure 7. Typical B-H Characteristics of Ferrite Core (TDK/PC40)

Output Power	Core
70-100W	EER35
100-150W	EER40 EER42
150-200W	EER49

Table 2. Commonly Used Cores for C-TV Applications

**[STEP-7] Determine the number of turns for each output**

Figure 8 shows the simplified diagram of the transformer. It is assumed that  $V_{O1}$  is the reference output which is regulated by the feedback control in normal operation. It is also assumed that the linear regulator is connected to  $V_{O2}$  to supply a stable voltage for MCU.

First, calculate the turns ratio ( $n$ ) between the primary winding and reference output ( $V_{O1}$ ) winding as a reference

$$n = \frac{V_{RO}}{V_{O1} + V_{F1}} \tag{12}$$

where  $V_{RO}$  is determined in STEP-3 and  $V_{O1}$  is the reference output voltage and  $V_{F1}$  is the forward voltage drop of diode ( $D_{R1}$ ).

Then, determine the proper integer for  $N_{S1}$  so that the resulting  $N_p$  is larger than  $N_p^{min}$  as

$$N_p = n \cdot N_{S1} > N_p^{min} \tag{13}$$

where  $n$  is obtained in equation (12) and  $N_p$  and  $N_{S1}$  are the number of turns for the primary side and the reference output, respectively.

The number of turns for the other output ( $n$ -th output) is determined as

$$N_{S(n)} = \frac{V_{O(n)} + V_{F(n)}}{V_{O1} + V_{F1}} \cdot N_{S1} \tag{14}$$

where  $V_{O(n)}$  is the output voltage and  $V_{F(n)}$  is the diode ( $D_{R(n)}$ ) forward voltage drop of the  $n$ -th output.

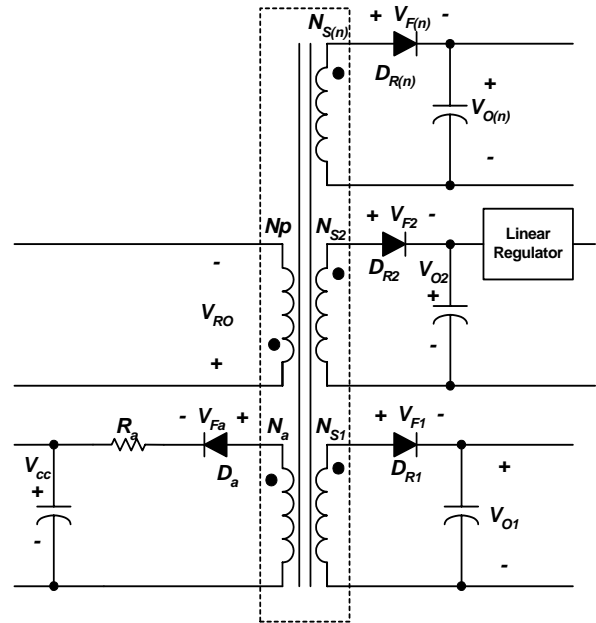


Figure 8. Simplified Diagram of the Transformer

- **Vcc winding design** : KA5Q-series drops all the outputs including the Vcc voltage in standby mode in order to minimize the power consumption. Once KA5Q-series enters into standby mode, Vcc voltage is hysteresis controlled between 11V and 12V as shown in Figure 9. The sync threshold voltage is also reduced from 2.6V to 1.3V in burst mode. Therefore, design the Vcc voltage to be around 24V in normal operation for proper quasi-resonant switching in standby mode as can be observed by

$$\frac{(11 + 12)/2}{24} \approx \frac{1.3}{2.6} \tag{15}$$

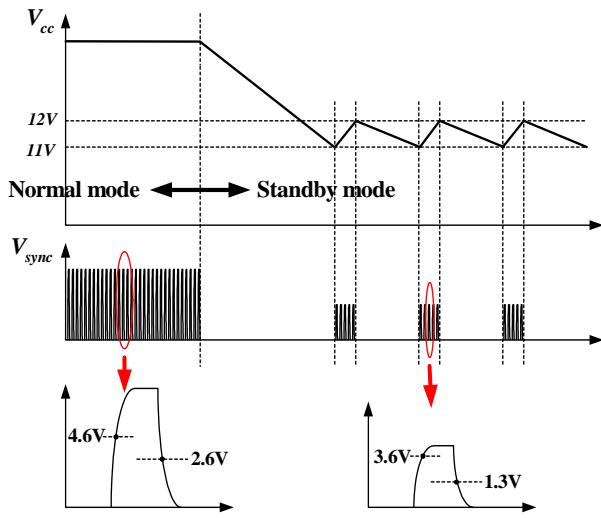


Figure 9. Burst operation in standby mode

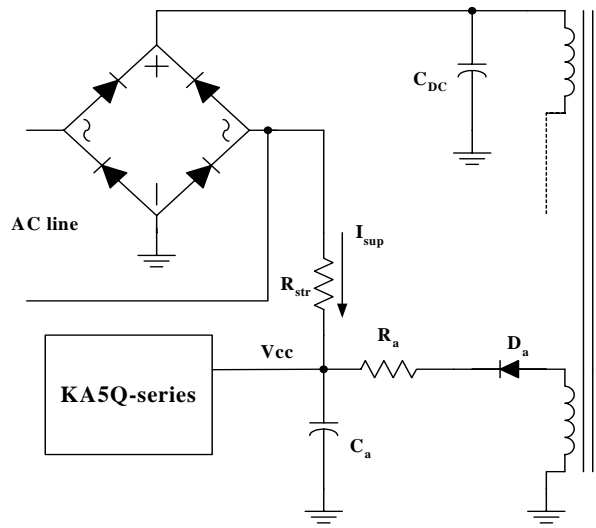


Figure. 10 Startup Resistor and Vcc Auxiliary Circuit

In general, switched mode power supply employs an error amplifier and an opto-coupler to regulate the output voltage. However, Primary Side Regulation (PSR) can be used for a low cost design if output regulation requirements are not very tight. PSR scheme regulates the output voltage indirectly by controlling the Vcc voltage without an opto-coupler. KA5Q-series has an internal error amplifier with a fixed reference voltage of 32.5V for PSR applications. If PSR is used, set Vcc to 32.5V.

After determining Vcc voltage in normal operation, the number of turns for the Vcc auxiliary winding (Na) is obtained as

$$N_a = \frac{V_{cc} + V_{Fa}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (\text{turns}) \quad (16)$$

where VFa is the forward voltage drop of Da as defined in Figure 8.

**[STEP-8] Determine the startup resistor**

Figure 10 shows the typical startup circuit for KA5Q-series. Because some protections are implemented as latch mode, AC startup is typically used to provide a fast reset. Initially, FPS consumes only startup current (max 200uA) before it begins switching. Therefore, the current supplied through the startup resistor (Rstr) can charge the capacitors Ca1 and Ca2 while supplying startup current to FPS. When Vcc reaches a start voltage of 15V (VSTART), FPS begins switching, and the current consumed by FPS increases. Then, the current required by FPS is supplied from the transformer’s auxiliary winding.

- **Startup resistor (Rstr)** : The average of the minimum current supplied through the startup resistor is given by

$$I_{sup}^{avg} = \left( \frac{\sqrt{2} \cdot V_{line}^{min}}{\pi} - \frac{V_{start}}{2} \right) \cdot \frac{1}{R_{str}} \quad (17)$$

where Vline<sup>min</sup> is the minimum input voltage, Vstart is the start voltage (15V) of FPS and Rstr is the startup resistor. The startup resistor should be chosen so that I<sub>sup</sub><sup>avg</sup> is larger than the maximum startup current (200uA). If not, Vcc can not be charged up to the start voltage and FPS will fail to start up.

The maximum startup time is determined as

$$T_{str}^{max} = C_a \cdot \frac{V_{start}}{(I_{sup}^{avg} - I_{start}^{max})} \quad (18)$$

Where Ca is the Vcc capacitor and I<sub>start</sub><sup>max</sup> is the maximum startup current (200uA) of FPS.

Once the startup resistor (Rstr) is determined, the maximum approximate power dissipation in Rstr is obtained as

$$P_{str} = \frac{1}{R_{str}} \cdot \left( \frac{(V_{line}^{max})^2}{2} + V_{start}^2 - \frac{2 \cdot \sqrt{2} \cdot V_{start} \cdot V_{line}^{max}}{\pi} \right) \quad (19)$$

where Vline<sup>max</sup> is the maximum input voltage, which is specified in STEP-1. The startup resistor should have a proper dissipation rating based on the value of Pstr



**[STEP-9] Determine the wire diameter for each winding based on the RMS current of each output.**

The RMS current of the n-th secondary winding is obtained as

$$I_{sec(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1-D_{max}}{D_{max}}} \cdot \frac{V_{RO} \cdot K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \quad (20)$$

where  $D_{max}$  and  $I_{ds}^{rms}$  are specified in equations (6) and (9),  $V_{o(n)}$  is the output voltage of the n-th output,  $V_{F(n)}$  is the diode ( $D_{R(n)}$ ) forward voltage drop,  $V_{RO}$  is specified in STEP-3 and  $K_{L(n)}$  is the load occupying factor for n-th output defined in equation (2).

The current density is typically  $5A/mm^2$  when the wire is long (>1m). When the wire is short with a small number of turns, a current density of  $6-10 A/mm^2$  is also acceptable. Do not use wire with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier. For high current output, it is recommended using parallel windings with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core,  $A_w$  (refer to Figure 6) is enough to accommodate the wires. The required winding window area ( $A_{wr}$ ) is given by

$$A_{wr} = A_c / K_F \quad (21)$$

where  $A_c$  is the actual conductor area and  $K_F$  is the fill factor. Typically the fill factor is 0.2~0.25 for single output applications and 0.15~0.2 for multiple output applications. If the required window ( $A_{wr}$ ) is larger than the actual window area ( $A_w$ ), go back to the STEP-6 and change the core to a bigger one. Sometimes it is impossible to change the core due to cost or size constraints. In that case, reduce  $V_{RO}$  in STEP-3 or increase  $f_s^{min}$ , which reduces the primary side inductance ( $L_m$ ) and the minimum number of turns for the primary ( $N_p^{min}$ ) as can be seen in equation (7) and (10).

**[STEP-10] Choose the proper rectifier diodes in the secondary side based on the voltage and current ratings.**

The maximum reverse voltage and the rms current of the rectifier diode ( $D_{R(n)}$ ) of the n-th output are obtained as

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max} \cdot (V_{o(n)} + V_{F(n)})}{V_{RO}} \quad (22)$$

$$I_{D(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1-D_{max}}{D_{max}}} \cdot \frac{V_{RO} K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \quad (23)$$

where  $K_{L(n)}$ ,  $V_{DC}^{max}$ ,  $D_{max}$  and  $I_{ds}^{rms}$  are specified in equations (2), (4), (6) and (9), respectively,  $V_{RO}$  is specified in STEP-3,  $V_{o(n)}$  is the output voltage of the n-th output and  $V_{F(n)}$  is the diode ( $D_{R(n)}$ ) forward voltage drop. The typical

voltage and current margins for the rectifier diode are as follows

$$V_{RRM} > 1.3 \cdot V_{D(n)} \quad (24)$$

$$I_F > 1.5 \cdot I_{D(n)}^{rms} \quad (25)$$

where  $V_{RRM}$  is the maximum reverse voltage and  $I_F$  is the average forward current of the diode.

A quick selection guide for the Fairchild Semiconductor rectifier diodes is given in Table 3. In this table,  $t_{rr}$  is the maximum reverse recovery time.

Ultra Fast Recovery Diode				
Products	$V_{RRM}$	$I_F$	$t_{rr}$	Package
EGP10B	100 V	1 A	50 ns	DO-41
UF4002	100 V	1 A	50 ns	DO-41
EGP20B	100 V	2 A	50 ns	DO-15
EGP30B	100 V	3 A	50 ns	DO-210AD
FES16BT	100 V	16 A	35 ns	TO-220AC
EGP10C	150 V	1 A	50 ns	DO-41
EGP20C	150 V	2 A	50 ns	DO-15
EGP30C	150 V	3 A	50 ns	DO-210AD
FES16CT	150 V	16 A	35 ns	TO-220AC
EGP10D	200 V	1 A	50 ns	DO-41
UF4003	200 V	1 A	50 ns	DO-41
EGP20D	200 V	2 A	50 ns	DO-15
EGP30D	200 V	3 A	50 ns	DO-210AD
FES16DT	200 V	16 A	35 ns	TO-220AC
EGP10F	300 V	1 A	50 ns	DO-41
EGP20F	300 V	2 A	50 ns	DO-15
EGP30F	300 V	3 A	50 ns	DO-210AD
EGP10G	400 V	1 A	50 ns	DO-41
UF4004	400 V	1 A	50 ns	DO-41
EGP20G	400 V	2 A	50 ns	DO-15
EGP30G	400 V	3 A	50 ns	DO-210AD
UF4005	600 V	1 A	75 ns	DO-41
EGP10J	600 V	1A	75 ns	DO-41
EGP20J	600 V	2 A	75 ns	DO-15
EGP30J	600 V	3 A	75 ns	DO-210AD
UF4006	800 V	1 A	75 ns	TO-41
UF4007	1000 V	1 A	75 ns	TO-41

Table 3. Fairchild Diode Quick Selection Table

**[STEP-11] Determine the output capacitors considering the voltage and current ripple.**

The ripple current of the n-th output capacitor ( $C_{o(n)}$ ) is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2} \quad (26)$$

where  $I_{o(n)}$  is the load current of the n-th output and  $I_{D(n)}^{rms}$  is specified in equation (23). The ripple current should be smaller than the maximum ripple current specification of the capacitor. The voltage ripple on the n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)} D_{max}}{C_{o(n)} f_s} + \frac{I_{ds}^{peak} V_{RO} R_{C(n)} K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \quad (27)$$

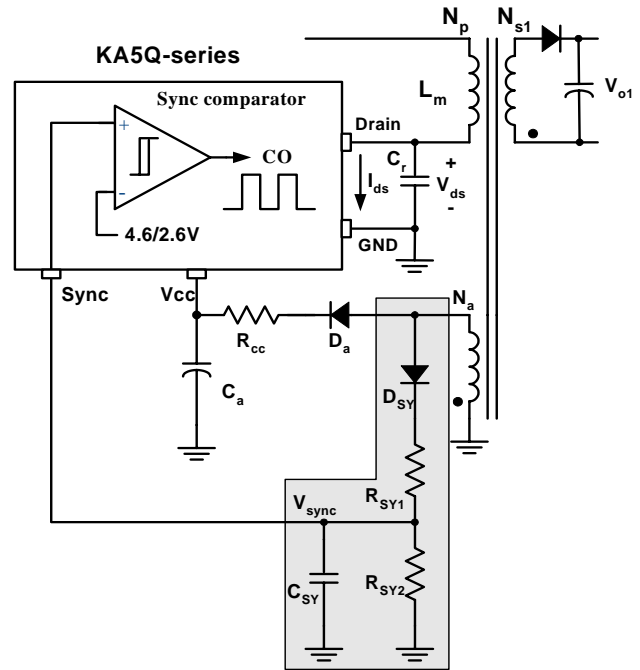
where  $C_{o(n)}$  is the capacitance,  $R_{C(n)}$  is the effective series resistance (ESR) of the n-th output capacitor,  $K_{L(n)}$ ,  $D_{max}$  and  $I_{ds}^{peak}$  are specified in equations (2), (6) and (8) respectively,  $V_{RO}$  is specified in STEP-3,  $I_{o(n)}$  and  $V_{o(n)}$  are the load current and output voltage of the n-th output, respectively and  $V_{F(n)}$  is the diode ( $D_{R(n)}$ ) forward voltage drop.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. In those cases, additional L-C filter stages (post filter) can be used to reduce the ripple on the output.

**[STEP-12] Design the synchronization network.**

KA5Q-series employs a quasi resonant switching technique to minimize the switching noise as well as switching loss. In this technique, a capacitor ( $C_r$ ) is added between the MOSFET drain and source as shown in Figure 11. The basic waveforms of a quasi-resonant converter are shown in Figure 12. The external capacitor lowers the rising slope of drain voltage, which reduces the EMI caused by the MOSFET turn-off. To minimize the MOSFET switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value as shown in Figure 12.

The optimum MOSFET turn-on time is indirectly detected by monitoring the Vcc winding voltage as shown in Figure 11 and 12. The output of the sync detect comparator (CO) becomes high when the sync voltage ( $V_{sync}$ ) exceeds 4.6V and low when the  $V_{sync}$  reduces below 2.6V. The MOSFET is turned on at the falling edge of the sync detect comparator output (CO).



**Figure. 11 Synchronization Circuit**

The peak value of the sync signal is determined by the voltage divider network  $R_{SY1}$  and  $R_{SY2}$  as

$$V_{sync}^{pk} = \frac{R_{SY2}}{R_{SY1} + R_{SY2}} \cdot V_{cc} \quad (28)$$

Choose the voltage divider  $R_{SY1}$  and  $R_{SY2}$  so that the peak value of sync voltage ( $V_{sync}^{pk}$ ) is lower than the OVP threshold voltage (12V) in order to avoid triggering OVP in normal operation. Typically,  $V_{sync}^{pk}$  is set to 8~10V.

To synchronize the  $V_{sync}$  with the MOSFET drain voltage, choose the sync capacitor ( $C_{SY}$ ) so that  $T_F$  is same as  $T_Q$  as shown in Figure 12.  $T_F$  and  $T_Q$  are given, respectively, as

$$T_F = \pi \cdot \sqrt{L_m \cdot C_{e0}} \quad (29)$$

$$T_Q = R_{SY2} \cdot C_{SY} \cdot \ln\left(\frac{V_{cc}}{2.6} \cdot \frac{R_{SY2}}{R_{SY1} + R_{SY2}}\right) \quad (30)$$

where  $L_m$  is the primary side inductance of the transformer,  $N_s$  and  $N_a$  are the number of turns for the output winding and Vcc winding, respectively and  $C_{e0}$  is the effective MOSFET output capacitance ( $C_{oss} + C_r$ ).

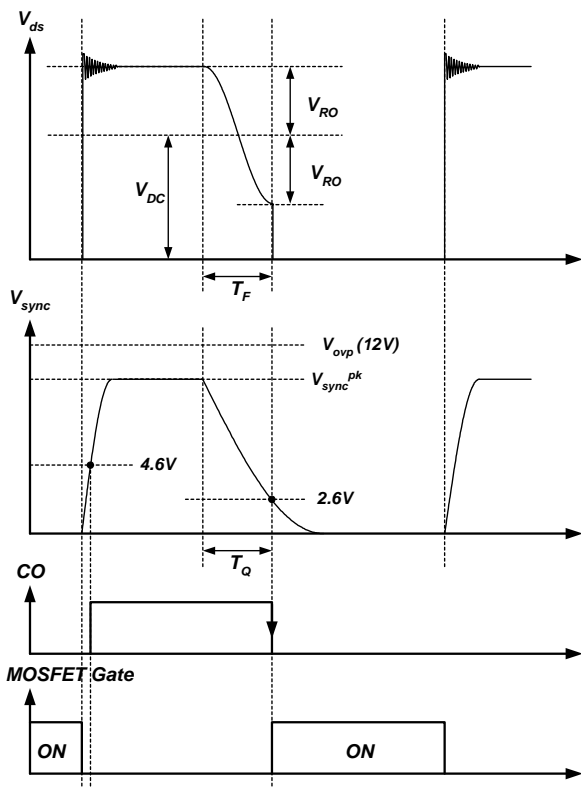


Figure 12 Synchronization Waveforms

**[STEP-13] Design voltage drop circuit for the burst operation.**

To minimize the power consumption in the standby mode, KA5Q-series employs burst operation. Once FPS enters into burst mode, all the output voltages as well as effective switching frequencies are reduced as shown in Figure 13. Figure 14 shows the typical output voltage drop circuit for C-TV applications. Under normal operation, the picture on signal is applied and the transistor  $Q_1$  is turned on, which decouples  $R_3$  and  $D_1$  from the feedback network. Therefore, only  $V_{o1}$  is regulated by the feedback circuit in normal operation and is determined as

$$V_{o1} = 2.5 \cdot \left( \frac{R_1 + R_2}{R_2} \right) \quad (31)$$

In standby mode, the picture on signal is disabled and the transistor  $Q_1$  is turned off, which couples  $R_3$  and  $D_1$  to the reference pin of KA431. If  $R_3$  is small enough to make the reference pin voltage of KA431 higher than 2.5V, the current through the opto LED pulls down the feedback voltage ( $V_{FB}$ ) of FPS and forces FPS to stop switching. Once FPS stops switching,  $V_{cc}$  decreases, and when  $V_{cc}$  reaches 11V, it resumes switching with a predetermined peak drain current until  $V_{cc}$  reaches 12V. When  $V_{cc}$  reaches 12V, the switching operation is terminated again until  $V_{cc}$  reduces to 11V. In this way,  $V_{cc}$  is hysteresis controlled between 11V and 12V in the burst mode operation.

Assuming that both  $V_{o1}$  and  $V_{o2}$  drop to half of their normal values, the maximum value of  $R_3$  for proper burst operation is given by

$$R_3 = \frac{(V_{o2}/2 - 0.7 - 2.5) \cdot R_1 \cdot R_2}{2.5 \cdot (R_1 + R_2) - (R_2 \cdot V_{o1}/2)} \quad (32)$$

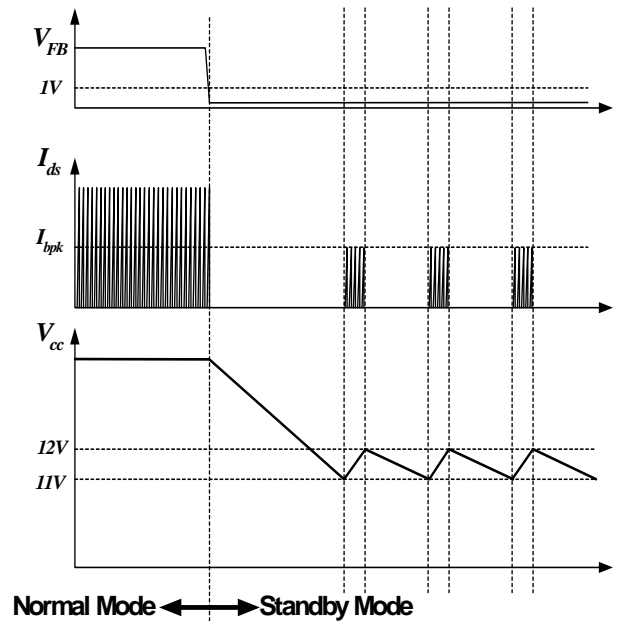


Figure 13. Burst Operation Waveforms

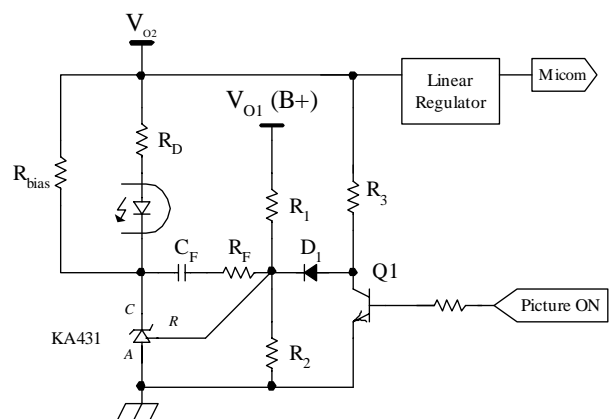


Figure 14. Typical Feedback Circuit to Drop Output Voltage in Standby Mode

**[STEP-14] Design the feedback control circuit.**

Since the KA5Q-series employs current mode control as shown in Figure 15, the feedback loop can be easily implemented with a one-pole and one-zero compensation circuit. The current control factor of FPS,  $K$  is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{LIM}}{V_{FBsat}} \quad (33)$$

where  $I_{pk}$  is the peak drain current and  $V_{FB}$  is the feedback voltage for a given operating condition,  $I_{LIM}$  is the current limit of the FPS and  $V_{FBsat}$  is the internal feedback saturation voltage, which is typically 2.5V.

In order to express the small signal AC transfer functions, the small signal variations of feedback voltage ( $v_{FB}$ ) and controlled output voltage ( $v_{o1}$ ) are introduced as  $\hat{v}_{FB}$  and  $\hat{v}_{o1}$ .

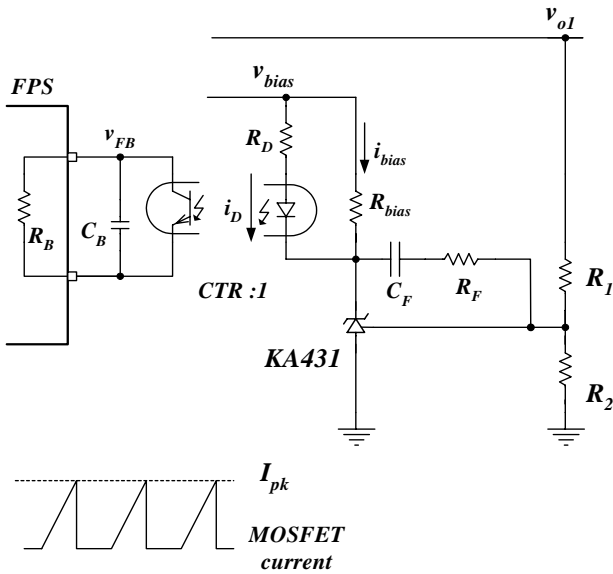


Figure 15. Control Block Diagram

For quasi-resonant flyback converters, the control-to-output transfer function using current mode control is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{V_{FB}} = \frac{K \cdot R_L V_{DC} (N_p / N_{s1}) \cdot (1 + s/w_z)(1 - s/w_{rz})}{2(2V_{RO} + v_{DC}) \cdot (1 + s/w_p)} \quad (34)$$

where  $V_{DC}$  is the DC input voltage,  $R_L$  is the effective total load resistance of the controlled output, which is defined as  $V_{o1}^2/P_o$ . Additionally,  $N_p$  and  $N_{s1}$  are specified in STEP-7,  $V_{RO}$  is specified in STEP-3,  $V_{o1}$  is the reference output voltage,  $P_o$  is specified in STEP-1 and  $K$  is specified in equation (33). The pole and zeros of equation (34) are defined as

$$w_z = \frac{1}{R_{c1}C_{o1}}, w_{rz} = \frac{R_L(1-D)^2}{DL_m(N_{s1}/N_p)^2} \text{ and } w_p = \frac{(1+D)}{R_L C_{o1}}$$

where  $L_m$  is specified in equation (7),  $D$  is the duty cycle of the FPS,  $C_{o1}$  is the output capacitor of  $V_{o1}$  and  $R_{c1}$  is the ESR of  $C_{o1}$ .

When the converter has more than one output, the low frequency control-to-output transfer function is proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective load resistance is used in equation (34) instead of the actual load resistance of  $V_{o1}$ . Notice that there is a right half plane (RHP) zero ( $w_{rz}$ ) in the control-to-output transfer function of equation (34). Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

The Figure 16 shows the variation of a quasi-resonant flyback converter's control-to-output transfer function for different input voltages. This figure shows the system poles and zeros together with the DC gain change for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

Figure 17 shows the variation of a quasi-resonant flyback converter's control-to-output transfer function for different loads. This figure shows that the gain between  $f_p$  and  $f_z$  does not change for different loads and the RHP zero is lowest at the full load condition.

The feedback compensation network transfer function of Figure 15 is obtained as

$$\frac{\hat{v}_{FB}}{\hat{v}_{o1}} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + s/w_{pc}} \quad (35)$$

$$\text{where } w_i = \frac{R_B \cdot CTR}{R_1 R_D C_F}, w_{zc} = \frac{1}{R_F C_F}, w_{pc} = \frac{1}{R_B C_B}$$

and  $R_B$  is the internal feedback bias resistor of FPS, which is typically 2.8kΩ,  $CTR$  is the current transfer ratio of opto coupler and  $R_1, R_D, R_F, C_F$  and  $C_B$  are shown in Figure 15.

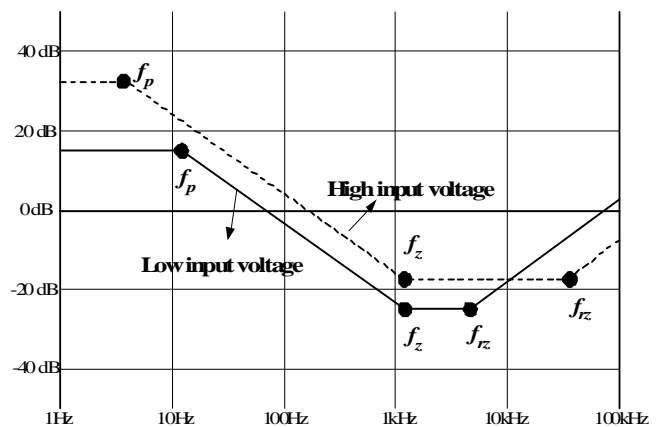
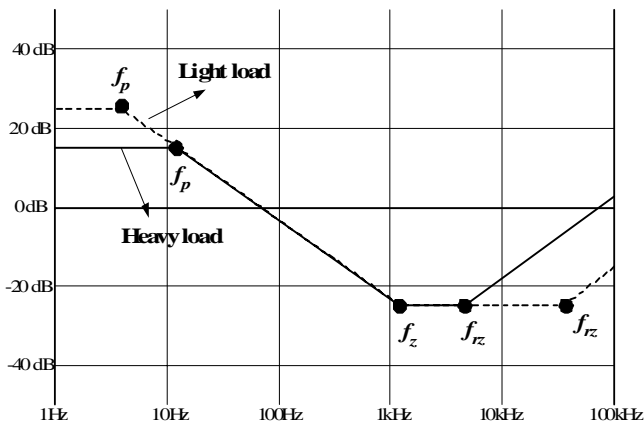


Figure 16. QR Flyback Converter Control-to Output Transfer Function Variation for Different Input Voltages



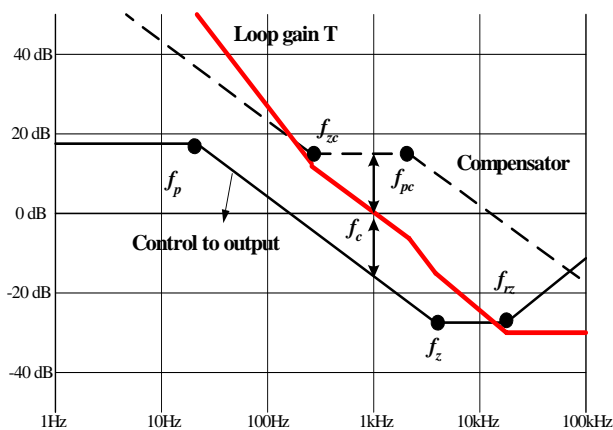
**Figure 17. QR Flyback Converter Control-to Output Transfer Function Variation for Different Loads**

When the input voltage and the load current vary over a wide range, determining the worst case for the feedback loop design is difficult. The gain together with zeros and poles varies according to the operating conditions.

One simple and practical solution to this problem is designing the feedback loop for low input voltage and full load condition with enough phase and gain margin. The RHP zero is lowest at low input voltage and full load condition. The gain increases only about 6dB as the operating condition is changed from the lowest input voltage to the highest input voltage condition under universal input condition.

The procedure to design the feedback loop is as follows

- (a) Set the crossover frequency ( $f_c$ ) below 1/3 of RHP zero to minimize the effect of the RHP zero. Set the crossover frequency below half of the minimum switching frequency ( $f_s^{min}$ ).
- (b) Determine the DC gain of the compensator ( $w_i/w_{zc}$ ) to cancel the control-to-output gain at  $f_c$ .
- (c) Place a compensator zero ( $f_{zc}$ ) around  $f_c/3$ .
- (d) Place a compensator pole ( $f_{pc}$ ) around  $3f_c$ .



**Figure 18. Compensator Design**

When determining the feedback circuit component, there are some restrictions as described below:

- (a) Design the voltage divider network of  $R_1$  and  $R_2$  to provide 2.5V to the reference pin of the KA431. The relationship between  $R_1$  and  $R_2$  is given as

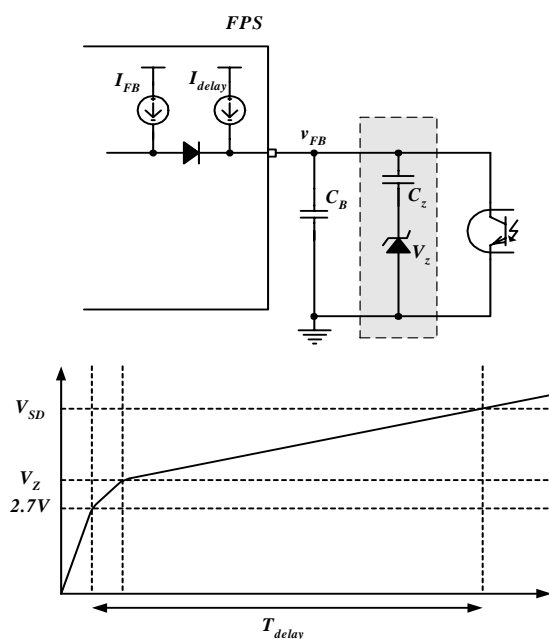
$$R_2 = \frac{2.5 \cdot R_1}{V_{O1} - 2.5} \tag{36}$$

where  $V_{O1}$  is the reference output voltage.

- (b) The capacitor connected to feedback pin ( $C_B$ ) is related to the shutdown delay time in an overload condition by

$$T_{delay} = (V_{SD} - 2.5) \cdot C_B / I_{delay} \tag{37}$$

where  $V_{SD}$  is the shutdown feedback voltage and  $I_{delay}$  is the shutdown delay current. Typical values for  $V_{SD}$  and  $I_{delay}$  are 7.5V and 5uA, respectively. In general, a delay of 20 ~ 50 ms is typical for most applications. Because  $C_B$  also determines the high frequency pole ( $w_{pc}$ ) of the compensator transfer function as shown in equation (35), too large a  $C_B$  can limit the control bandwidth by placing  $w_{pc}$  at too low a frequency. Typical value for  $C_B$  is 10-50nF. Application circuit to extend the shutdown time without limiting the control bandwidth is shown in Figure 19. By setting the zener breakdown voltage ( $V_z$ ) slightly higher than 2.7V, the additional delay capacitor ( $C_z$ ) is de-coupled from the feedback circuit in normal operation. When the feedback voltage exceeds the zener breakdown voltage ( $V_z$ ),  $C_z$  and  $C_B$  determine the shutdown time.



**Figure 19. Delayed Shutdown**

(c) The resistors  $R_{bias}$  and  $R_D$  used together with the optocoupler H11A817A and the shunt regulator KA431 should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage for the FPS device chosen. In general, the minimum values of cathode voltage and current for the KA431 are 2.5V and 1mA, respectively. Therefore,  $R_{bias}$  and  $R_D$  should be designed to satisfy the following conditions:

$$\frac{V_{bias} - V_{OP} - 2.5}{R_D} > I_{FB} \quad (38)$$

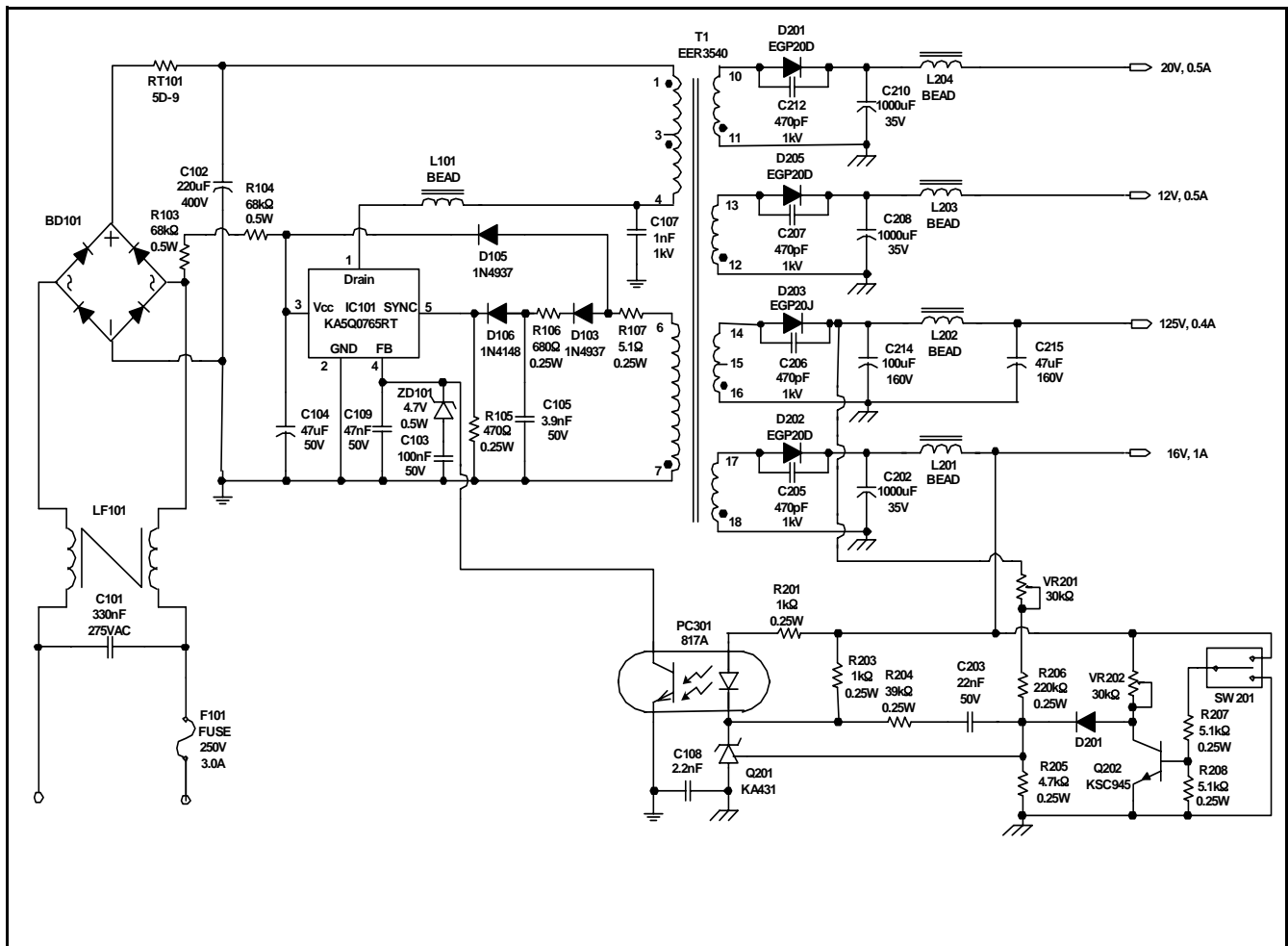
$$\frac{V_{OP}}{R_{bias}} > 1mA \quad (39)$$

where  $V_{bias}$  is the KA431 bias voltage as shown in Figure 16 and  $V_{OP}$  is opto-diode forward voltage drop, which is typically 1V.  $I_{FB}$  is the feedback current of FPS, which is typically 1mA.

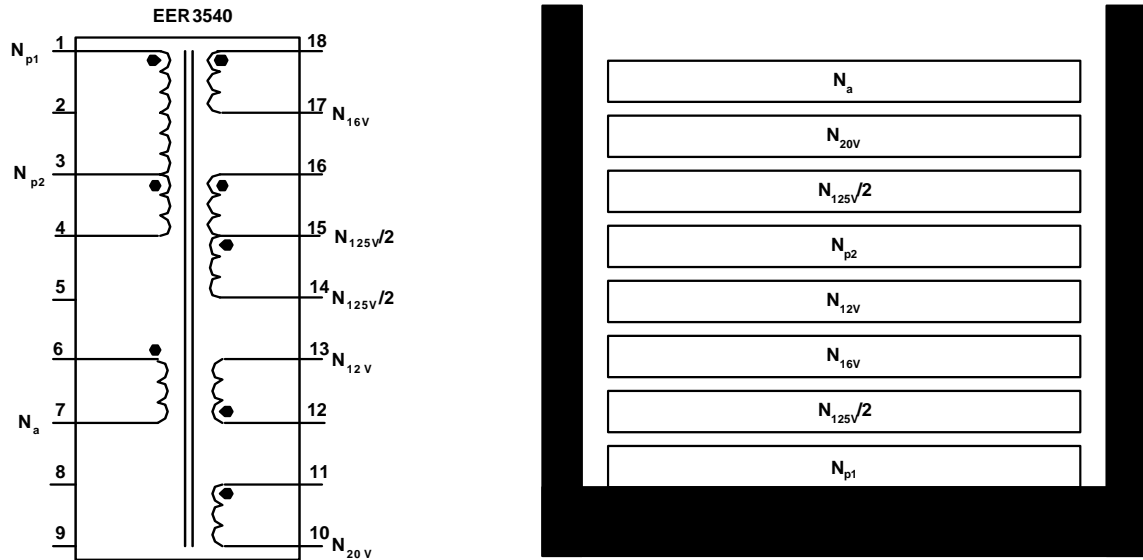
## Design Example I (KA5Q0765RT)

Application	Device	Input Voltage	Output Power	Output Voltage (Rated Current)
Color TV	KA5Q0765RT	85-265Vac (60Hz)	82W	125V (0.4A) 20V (0.5A) 16V (1.0A) 12V (0.5A)

### Schematic



## Transformer Specifications



Transformer Schematic Diagram

## Winding Specifications

No	Pin (s→f)	Wire	Turns	Winding Method
$N_{p1}$	1 - 3	$0.6^{\phi} \times 1$	35	Center Winding
$N_{125V/2}$	16 - 15	$0.6^{\phi} \times 1$	28	Center Winding
$N_{16V}$	18 - 17	$0.4^{\phi} \times 2$	8	Center Winding
$N_{12V}$	12 - 13	$0.5^{\phi} \times 1$	6	Center Winding
$N_{p2}$	3 - 4	$0.6^{\phi} \times 1$	35	Center Winding
$N_{125V/2}$	15 - 14	$0.5^{\phi} \times 1$	28	Center Winding
$N_{20V}$	11 - 10	$0.5^{\phi} \times 1$	10	Center Winding
$N_a$	7 - 6	$0.3^{\phi} \times 1$	11	Center Winding

## Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 4	$565\mu\text{H} \pm 5\%$	1kHz, 1V
Leakage Inductance	1 - 4	10uH Max	2 <sup>nd</sup> all short

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Core : EER 3540

Bobbin : EER3540

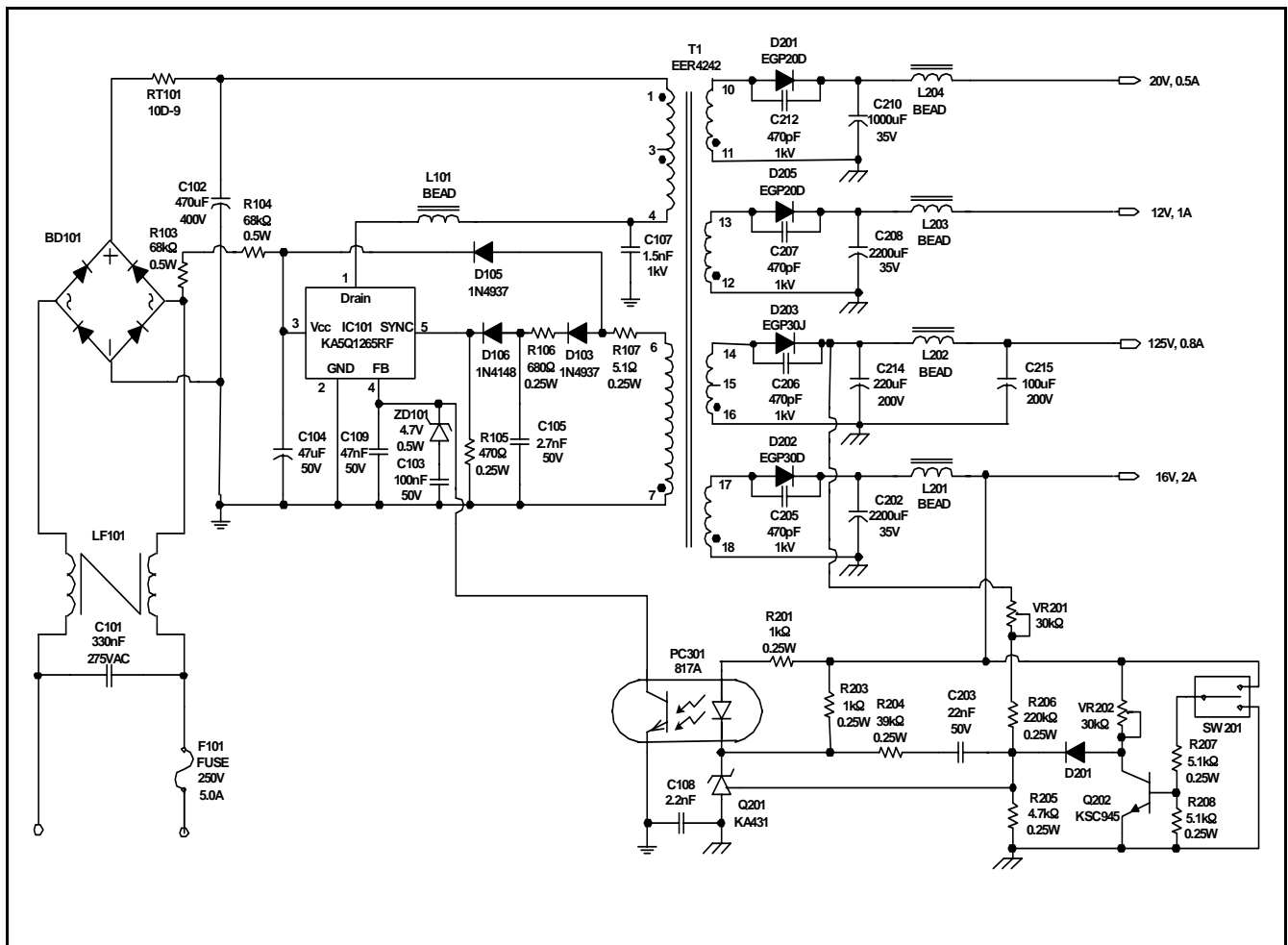
$A_e : 109 \text{ mm}^2$



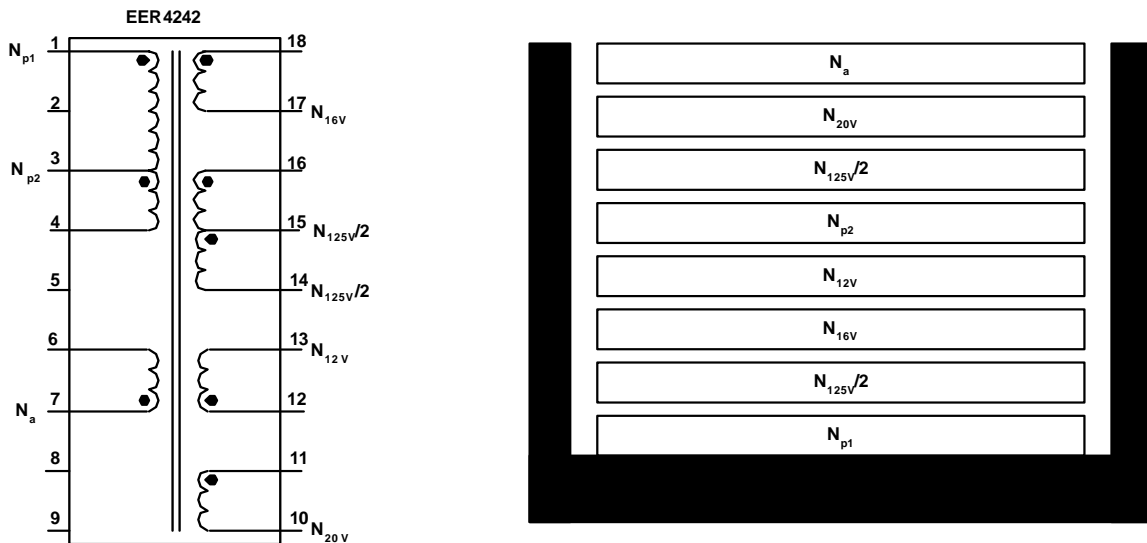
## Design Example II (KA5Q1265RF)

Application	Device	Input Voltage	Output Power	Output Voltage (Rated Current)
Color TV	KA5Q1265RF	85-265Vac (60Hz)	154W	125V (0.8A) 20V (0.5A) 16V (2.0A) 12V (1.0A)

### Schematic



## Transformer Specifications



Transformer Schematic Diagram

## Winding Specifications

No	Pin (s→f)	Wire	Turns	Winding Method
$N_{p1}$	1 - 3	$0.5^{\phi} \times 2$	22	Center Winding
$N_{125V/2}$	16 - 15	$0.5^{\phi} \times 2$	18	Center Winding
$N_{16V}$	18 - 17	$0.5^{\phi} \times 2$	5	Center Winding
$N_{12V}$	12 - 13	$0.4^{\phi} \times 2$	4	Center Winding
$N_{p2}$	3 - 4	$0.5^{\phi} \times 2$	22	Center Winding
$N_{125V/2}$	15 - 14	$0.5^{\phi} \times 2$	18	Center Winding
$N_{20V}$	11 - 10	$0.5^{\phi} \times 1$	6	Center Winding
$N_a$	7 - 6	$0.3^{\phi} \times 1$	7	Center Winding

## Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 4	$385\mu\text{H} \pm 5\%$	1kHz, 1V
Leakage Inductance	1 - 4	10uH Max	2 <sup>nd</sup> all short

## Core & Bobbin

Core : EER 4242

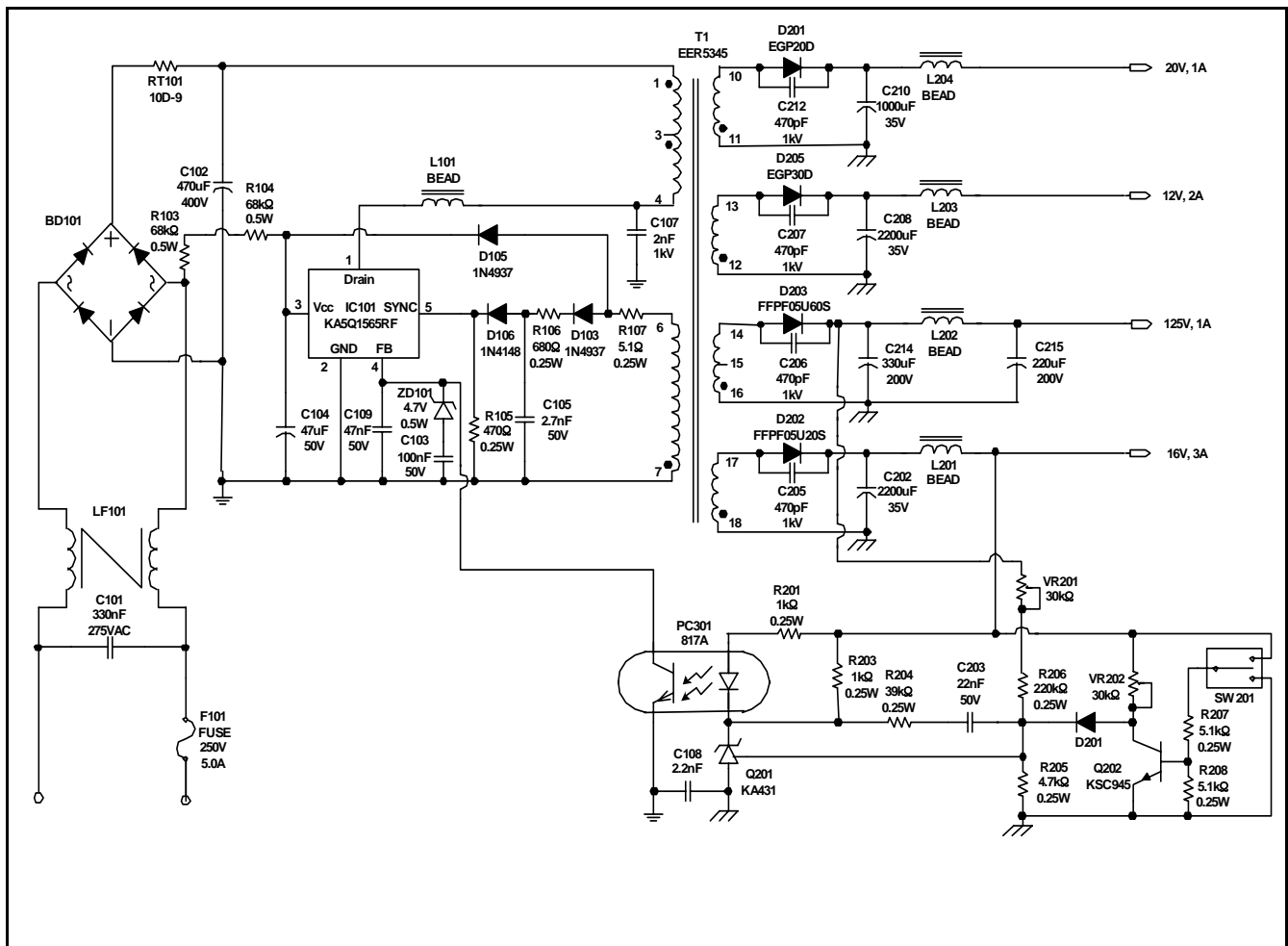
Bobbin : EER4242

$A_e : 234 \text{ mm}^2$

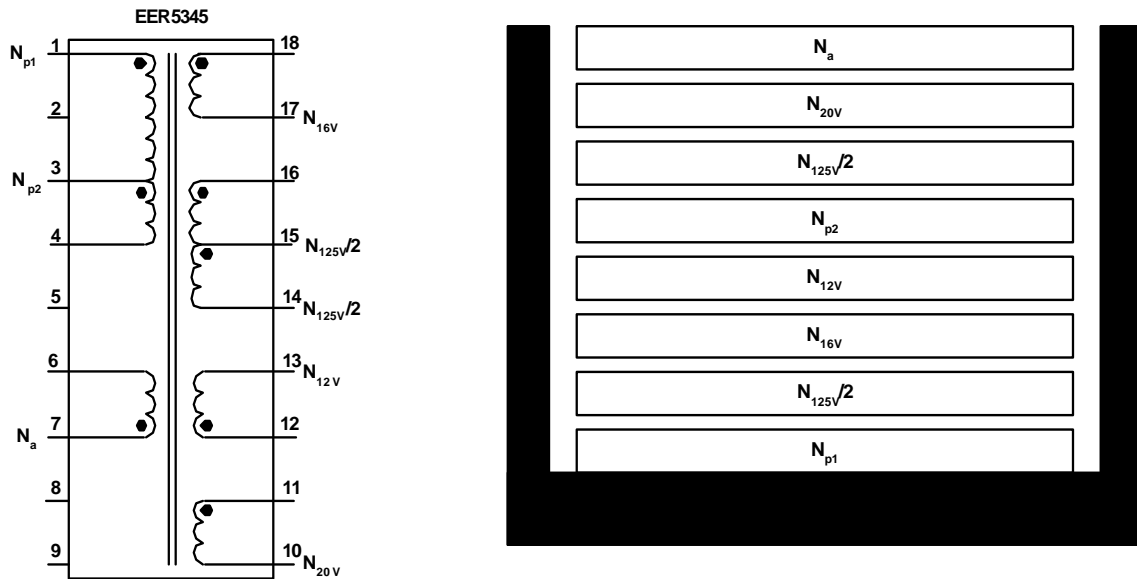
## Design Example III (KA5Q1565RF)

Application	Device	Input Voltage	Output Power	Output Voltage (Rated Current)
Color TV	KA5Q1565RF	85-265Vac (60Hz)	217W	125V (1.0A) 20V (1.0A) 16V (3.0A) 12V (2.0A)

### Schematic



## Transformer Specifications



Transformer Schematic Diagram

## Winding Specifications

No	Pin (s→f)	Wire	Turns	Winding Method
$N_{p1}$	1 - 3	$0.6^{\phi} \times 2$	21	Center Winding
$N_{125V/2}$	16 - 15	$0.6^{\phi} \times 2$	17	Center Winding
$N_{16V}$	18 - 17	$0.6^{\phi} \times 3$	5	Center Winding
$N_{12V}$	12 - 13	$0.6^{\phi} \times 2$	4	Center Winding
$N_{p2}$	3 - 4	$0.6^{\phi} \times 2$	21	Center Winding
$N_{125V/2}$	15 - 14	$0.6^{\phi} \times 2$	17	Center Winding
$N_{20V}$	11 - 10	$0.5^{\phi} \times 1$	6	Center Winding
$N_a$	7 - 6	$0.3^{\phi} \times 1$	7	Center Winding

## Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 4	$325\mu\text{H} \pm 5\%$	1kHz, 1V
Leakage Inductance	1 - 4	10uH Max	2 <sup>nd</sup> all short

## Core & Bobbin

Core : EER 5345

Bobbin : EER5345

$A_e : 318 \text{ mm}^2$

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