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Comparison of MM74HC to 74LS, 74S and 74ALS Logic

Fairchild Semiconductor
Application Note 319
June 1983

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The MM54HC/MM74HC family of high speed logic components provides a combination of speed and power characteristics that is not duplicated by bipolar logic families or any other CMOS family. This CMOS family has operating speeds similar to low power Schottky (54LS/74LS) technology. MM54HC/MM74HC is approximately half as fast (delays are twice as long) as the 54ALS/74ALS and 54S/74S logic. Compared to CD4000 and 54C/74C, this is an order of magnitude improvement in speed, which is achieved by utilizing an advanced 3.5 micron silicon gate-recessed oxide CMOS process. The MM54HC/MM74HC components are designed to retain all the advantages of older metal gate CMOS, plus provide the speeds required by today's high speed systems.

Another key advantage of the MM54HC/MM74HC family is that it provides the functions and pin outs of the popular 54LS/74LS series logic components. Many functions which are unique to the CD4000 metal gate CMOS family have also been implemented in this high speed technology. In addition, the MM54HC/MM74HC family contains several special functions not previously implemented in CD4000 or 54LS/74LS.

Although the functions and the speeds are the same as 54LS/74LS, some of the electrical characteristics are different from either LS-TTL, S-TTL or ALS-TTL. The following discusses these differences and highlights the advantages and disadvantages of high speed CMOS.

AC PERFORMANCE

As mentioned previously, the MM54HC/MM74HC logic family has been designed to have speeds equivalent to LS-TTL, and to be 8–10 times faster than CD4000B and MM54C/MM74C logic. *Table 1* compares high speed CMOS to the bipolar logic families. HC-CMOS gate delays are typically the same as LS-TTL, and ALS-TTL is two to three times faster. S-TTL is also about twice as fast as HC-CMOS. Flip-flop and counter speeds also follow the same pattern.

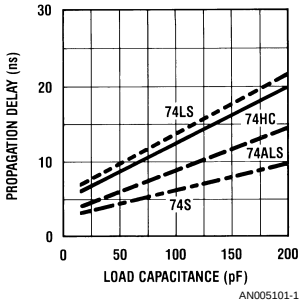

FIGURE 1. HC, LS, ALS, S Comparison of Propagation Delay vs Load for a NAND Gate

TABLE 1. Comparison of Typical AC Performance of LS-TTL, S-TTL, ALS-TTL and HC-CMOS

Gates		LS-TTL	ALS-TTL	HC-CMOS	S-TTL	Units
74XX00	Propagation Delay	8	5	8	4	ns
74XX04	Propagation Delay	8	4	8	3	ns
Combinational MSI						
74XX139	Propagation Delay					
	Select	25	8	25	8	ns
	Enable	21	8	20	7	ns
74XX151	Propagation Delay					
	Address	27	8	26	12	ns
	Strobe	26	7	17	12	ns
74XX240	Propagation Delay	12	3	10	5	ns
	Enable/Disable Time	20	7	17	10	ns
Clocked MSI						
74XX174	Propagation Delay	20	7	18	13	ns
	Operating Frequency	40	50	50	100	MHz
74XX374	Propagation Delay	19	7	16	11	ns
	Enable/Disable Time	21	9	17	11	ns
	Operating Frequency	50	50	50	100	MHz

Also, HC logic's propagation delay variation due to changes in capacitive loading is very similar to LS-TTL. *Figure 1* illustrates this by plotting delay versus loading for the various bipolar logic families and MM54HC/MM74HC. HC-CMOS has virtually the same speed and load-delay variation as LS-TTL and, as is expected, is slower than ALS and S-TTL logic. The slopes of these lines indicate the amount of variation in speed with loading, and are dependent on the output impedance of the particular logic gate. The delay variation of LS-TTL and HC-CMOS is similar whereas ALS-TTL and S-TTL have slightly less variation.

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POWER DISSIPATION

CD4000B and MM54C/MM74C CMOS devices are well known for extremely low quiescent power dissipation, and high speed CMOS retains this feature. *Table 2* compares typical HC static power consumption with LS, ALS and S-TTL. Even CMOS MSI dissipation is well below 1 µW while LS-TTL dissipation is many milliwatts. This makes MM54HC/MM74HC ideal for battery operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

TABLE 2. Comparison of Typical Quiescent Supply Current for Various Logic Families

	HC-CMOS	LS-TTL	ALS-TTL	S-TTL
SSI	0.0025 µW	5.0 mW	2.0 mW	75 mW
Flip-Flop	0.005 µW	20.0 mW	10 mW	150 mW
MSI	0.25 µW	90 mW	40 mW	470 mW

CMOS dissipation increases proportionately with operating frequency. Doubling the operating frequency doubles the current consumption. This is due to currents generated by charging internal and load capacitances. *Figure 3* shows power dissipation versus frequency for a completely unloaded NAND gate, flip-flop and counter implemented in all 4 technologies.

The LS, S and ALS curves are essentially flat because the quiescent currents mask out capacitive effects, except at very high frequencies. Capacitive effects are slightly lower for the TTL families, so that, at high frequencies, CMOS dissipation may actually be more than ALS and LS. However, the power crossover frequency is usually well above the maximum operating frequency of MM54HC/MM74HC.

The previously mentioned curves plot unloaded circuits. When considering typical system power consumption, capacitive loading should also be considered. *Table 3* lists components to implement all the support logic for a small microprocessor based system. By assuming a typical load capacitance of 50 pF, the power dissipation for these devices can be calculated at various average system clock frequencies. *Figure 2* plots power consumption for 74HC, 74LS, 74ALS and 74S logic implementations. Above 1 MHz, capacitive currents now also tend to dominate bipolar power dissipation as well.

TABLE 3. Hypothetical "Glue" Logic for a Typical Microprocessor System

System Components	# of ICs
Address Decoders ('138)	10
Address Comparators ('688)	5
Address/Data Buffers ('240/4)	10
Address/Data Latches ('373/4)	20
MSI Control/Gating ('00, '10)	30
Misc. Counter/Shift Reg ('161, '164)	20
Flip-Flops ('73/4)	10

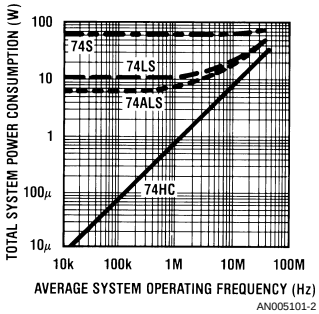
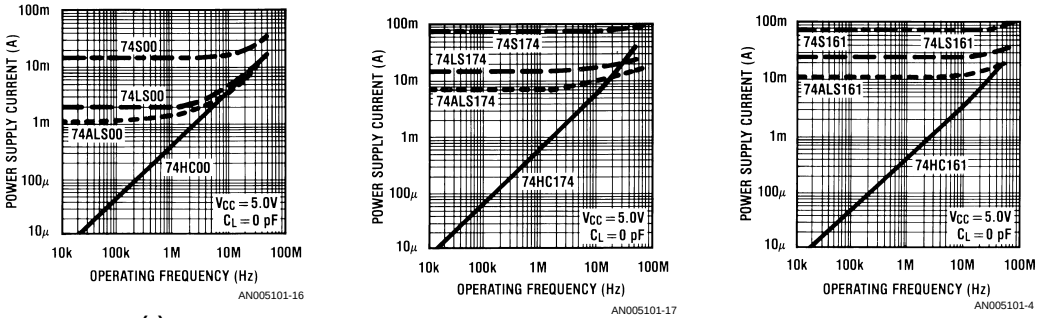


FIGURE 2. Power Consumption for Hypothetical Microprocessor System Support Logic



(a) **(b)** **(c)**

FIGURE 3. Supply Current Consumption Comparison for (a) 74XX00 (b) 74XX714 (c) 74XX161 Circuits

Since, in a typical system, some sections will operate at a high frequency and other parts at lower frequencies, the average system clock frequency is a simplification. For example, a 10 MHz microprocessor will have a bus cycle frequency of 2 to 5 MHz. Most system and memory components will be accessed a small amount of the time, resulting in effective clock frequencies on the order of 100 kHz for these sections. Thus, the average system clock frequency would be around 1 to 2 MHz, and an 8 to 1 power savings would be realized by using CMOS.

Another simplification was made to calculate system power. CMOS circuits will dissipate much less power when 3-STATE, which would save much power since, in a given

bus cycle, only a few buffers will be enabled. LS, ALS and S, however, actually dissipate more power when their outputs are disabled.

Several interesting conclusions can be drawn from *Figure 2*. First, notice that, at higher frequencies, the bipolar logic families start to dissipate more power. This is a result of current consumption due to switching the load. As the operating frequency approaches infinity, this will be the dominant effect. So, for extremely fast low power systems, minimizing load capacitance and overall operating frequency becomes more important. As lower power TTL logic is introduced, system power will be increasingly dependent on capacitive load effects similar to CMOS.

Second, TTL logic has a slightly smaller logic voltage swing than CMOS. Thus, for a given load, TTL will actually have a lower average load current. So, similar to the unloaded example, at very high frequencies, CMOS could consume more power than TTL. As *Figure 5* indicates, these frequencies are usually far above the 30 MHz limit of HC-CMOS or LS-TTL.

INPUT VOLTAGE CHARACTERISTICS AND NOISE IMMUNITY

To maintain the advantage CMOS has in noise immunity, the input logic levels are defined to be similar to metal gate CMOS. At V_{CC}=5V, MM54HC/MM74HC is designed to have input voltages of V_{IH}=3.5V and V_{IL}=1.0V. Additionally, input voltage over the operating supply voltage range is: V_{IH}=0.7V_{CC} and V_{IL}=0.2V_{CC}. This compares to V_{IH}=2.0V and V_{IL}=0.8V specified for LS-TTL over its supply range. *Figure 4* illustrates the input voltage differences, and the greater noise immunity HC logic has over its supply range. Maintaining wide noise immunity gives HC-CMOS an advantage in many industrial, automotive, and computer applications where high noise levels exist.

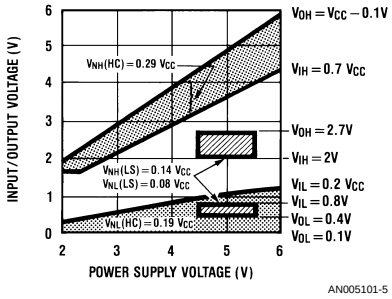


FIGURE 4. Worst-Case Input and Output Voltages Over Operating Supply Range for HC and LS Logic

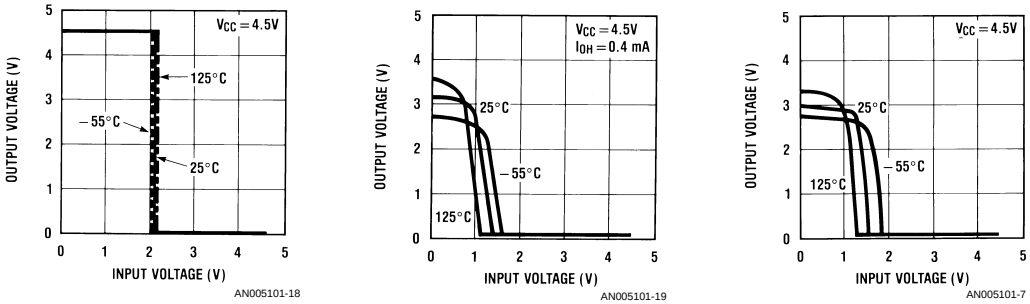


FIGURE 5. Input-Output Transfer Characteristics for 74XX00 NAND Gate Implemented in (a) HC-CMOS (b) LS-TTL (c) ALS-TTL

Another indication of DC noise immunity is the typical transfer characteristics for the logic families. *Figure 5* shows the transfer function of the 74XX00 NAND gate for HC-CMOS, LS-TTL and ALS-TTL. High speed CMOS has a very sharp transition typically at 2.25V, and this transition point is very stable over temperature. The bipolar logic transfer functions are not as sharp and vary several hundred millivolts over temperature. This sharp transition is due to the large circuit gains provided by triple buffering the HC-CMOS gate compared to the single bipolar gain stage. *Figure 6* compares the transfer function of the 'HC08 and the 'ALS08, both of which are double buffered. The 'ALS08 has a sharper transition, but the CMOS gate still has less temperature variation and a more centered trip point. However, the TTL trip point is not dependent on V_{CC} variation as CMOS is.

The high speed CMOS input levels are not totally compatible with TTL output voltage specifications. To make them com-

patible would compromise noise immunity, die size, and significant speed. The designer may improve compatibility by adding a pull-up resistor to the TTL output. He may also utilize a series of TTL-to-CMOS level converters which are being provided to ease design of mixed HC/LS/ALS/S systems. These buffers have 0.8V and 2.0V TTL input voltage specifications, and provide CMOS compatible outputs. When mixing logic, the noise immunity at the TTL to CMOS interface is no better than LS-TTL, but a substantial savings in power will occur when using MM54HC/MM74HC logic.

INPUT CURRENT

The HC family maintains the ultra-low input currents typical of CMOS circuits. This current is less than 1 µA and is caused by input protection diode leakages. This compares to the much larger LS-TTL input currents of 0.4 mA for a low input and 40 µA for a high input. ALS-TTL input currents are 0.2 mA and 20 µA and S-TTL input currents are 3.2 mA and 100 µA. *Figure 7* tabulates these values. The near zero input current of CMOS eases designing, since a typical input can be viewed as an open circuit. This eliminates the need for fanout restrictions which are necessary in TTL logic designs.

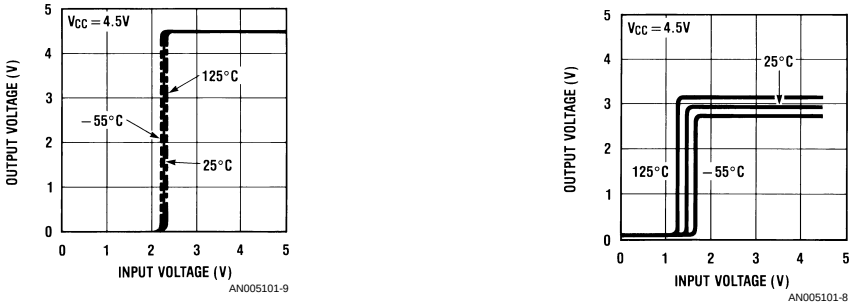


FIGURE 6. Input-Output Transfer Characteristics for 74XX08 AND Gate Implemented in (a) HC-CMOS (b) ALS-TTL

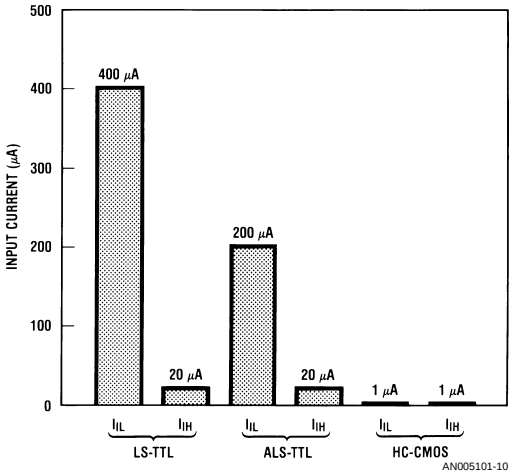


FIGURE 7. Comparison of Input Current Specifications for Various Logic Families

POWER SUPPLY RANGE

Figure 4 also compares the supply range of MM54HC/MM74HC logic and LS-TTL. The high speed CMOS family is specified to operate at voltages from 2V to 6V. 54LS, 54S and 54ALS logic is specified to operate from 4.5V to 5.5V, and 74LS and 74S will operate from 4.75V to 5.25V. 74ALS is specified over a 4.5V to 5.5V supply range. This wider operating range for the HC family eases power supply design by eliminating costly regulators and enhances battery operation capabilities.

OUTPUT DRIVE

Since there was no speed, noise immunity, or power trade-off, standard HC-CMOS was designed to have similar high current output drive that is characteristic of LS-TTL and ALS-TTL. Schottky TTL has about 5 times the output drive of MM54HC/MM74HC. Thus HC-CMOS has an output low current specification of 4 mA at an output voltage of 0.4V. In keeping with CD4000B series and 54C/74C series logic, the source and sink currents are symmetrical. Thus HC logic can source 4 mA as well. This large increase in output current for high speed CMOS over CD4000B also has the added advantage of reducing signal line crosstalk which can be of greater concern in high speed systems. *Figure 8* compares HC, LS, and ALS specified output currents.

Since TTL logic families do have significant input currents they have a limited fanout capability. *Table 4* illustrates the limitations of these families, based on their input and output currents. High speed CMOS is also included. MM54HC/MM74HC has the same CMOS-to-CMOS fanout characteristics as CD4000B, virtually infinite.

TABLE 4. Fanout of HC-CMOS, LS-TTL, ALS-TTL, S-TTL

From, To	74HC	74LS	74ALS	74S
74HC	4000	10	20	2
74LS	*	20	40	4
74ALS	*	20	40	4
74S	*	50	100	10

As another indication of the similarity of HC-CMOS to LS-TTL, *Figure 9* plots typical output currents versus output voltage for LS and HC. The output sink current curves are very similar, but LS source current is somewhat different, due to its emitter-follower output circuitry.

MM54HC/MM74HC bus driving circuits, namely the 3-STATE buffers and latches, have half again as much output current drive as standard outputs. These components have a 6 mA output drive. The 6 mA was chosen based on a trade-off of die size and speed-load variations. This current is less than the 12 mA or more specified for LS and ALS bus driver circuits, because the bus fanout limitations of these families do not apply in CMOS systems. S-TTL bus output sink current is 48 mA.

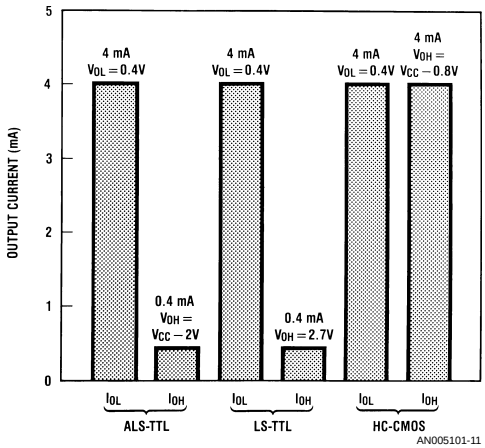


FIGURE 8. Output Current Specifications for ALS-TTL, S-TTL and HC-CMOS

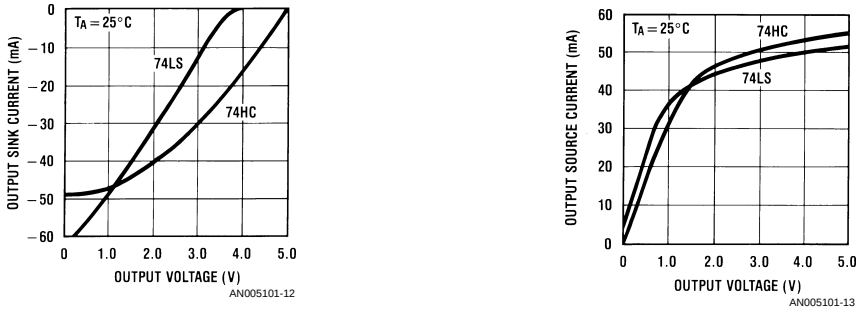


FIGURE 9. Comparison of Standard LS-TTL and HC-CMOS Output (a) Source (b) Sink Currents

OPERATING TEMPERATURE RANGE

The operating temperature range and temperature effects on various HC-CMOS operating parameters differ from bipolar logic. The recommended temperature range for 74LS, 74S, and 74ALS is 0˚C to 70˚C, compared to −40˚C to 85˚C for the 74HC family. 54 series logic is specified from −55˚C to 125˚C for all four families.

Temperature variation of operating parameters for the MM54HC/MM74HC family behaves very predictably and is due to the gain decreasing of MOSFET transistors as temperature is increased. Thus the output currents decrease and propagation delays increase at about 0.3% per degree centigrade.

Figure 10 shows typical propagation delays for the 74XX00 over the −55˚C to +125˚C temperature range. The 'HC00's speed increases almost linearly with temperature, whereas the LS and ALS behave differently.

A WORD ABOUT PLUG-IN REPLACEMENT OF TTL

MM54HC/MM74HC logic implements TTL equivalent functions with the same pin outs as TTL. HC is not designed to be directly plug-in replaceable, but, with some care, some TTL systems can be converted to MM54HC/MM74HC with little or no modification. The replaceability of HC is determined by several factors.

One factor is the difference in input levels. In systems where all TTL is not being replaced and TTL outputs feed CMOS inputs, the input high voltages, as specified, are not totally compatible. Although TTL outputs will typically drive HC inputs correctly, an external pull-up resistor should be added to the TTL outputs, or an MM54HCT/MM74HCT TTL compatible circuit should be used. This incompatibility tends to limit the designer's ability to intermingle TTL and HC-CMOS. Note, though, that HC outputs are completely compatible with the various TTL family's input specifications; therefore, there is no problem when HC is driving TTL.

Another source of possible problems can occur when the LS design floats device inputs. This practice is not recommended when using LS-TTL, but it is sometimes done. Usually, TTL inputs float high; however, CMOS inputs may float either high or low depending on the static charge on the input. It is therefore important to always tie unused CMOS inputs to either V_{CC} or ground to avoid incorrect logic functioning.

A third factor to consider when replacing any TTL logic is AC performance. The logic functions provided by 54HC/74HC are equivalent to LS-TTL, and the propagation delay, set-up and hold times are similar to LS. However, there are some differences in the way CMOS circuits are implemented which will cause differences in speed. For the most part, these differences are minor, but it is important to verify that they do not affect the design.

CONCLUSION

The MM54HC/MM74HC family represents a major step forward in CMOS performance. It is a full line family capable of being designed into virtually any application which now uses LS-TTL with substantial improvement in power consumption. ALS and S-TTL primarily offer faster speeds than HC-CMOS, but still do not have the input and output advantages or the lower power consumption of CMOS. Because of its high input impedance and large output drive, HC logic is actually easier to use. This, coupled with continued expansion of the 54HC/74HC, will make it an increasingly popular logic family.

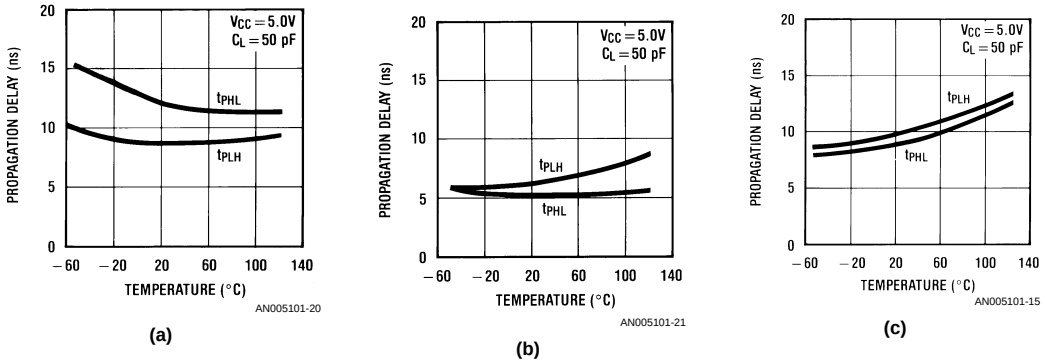
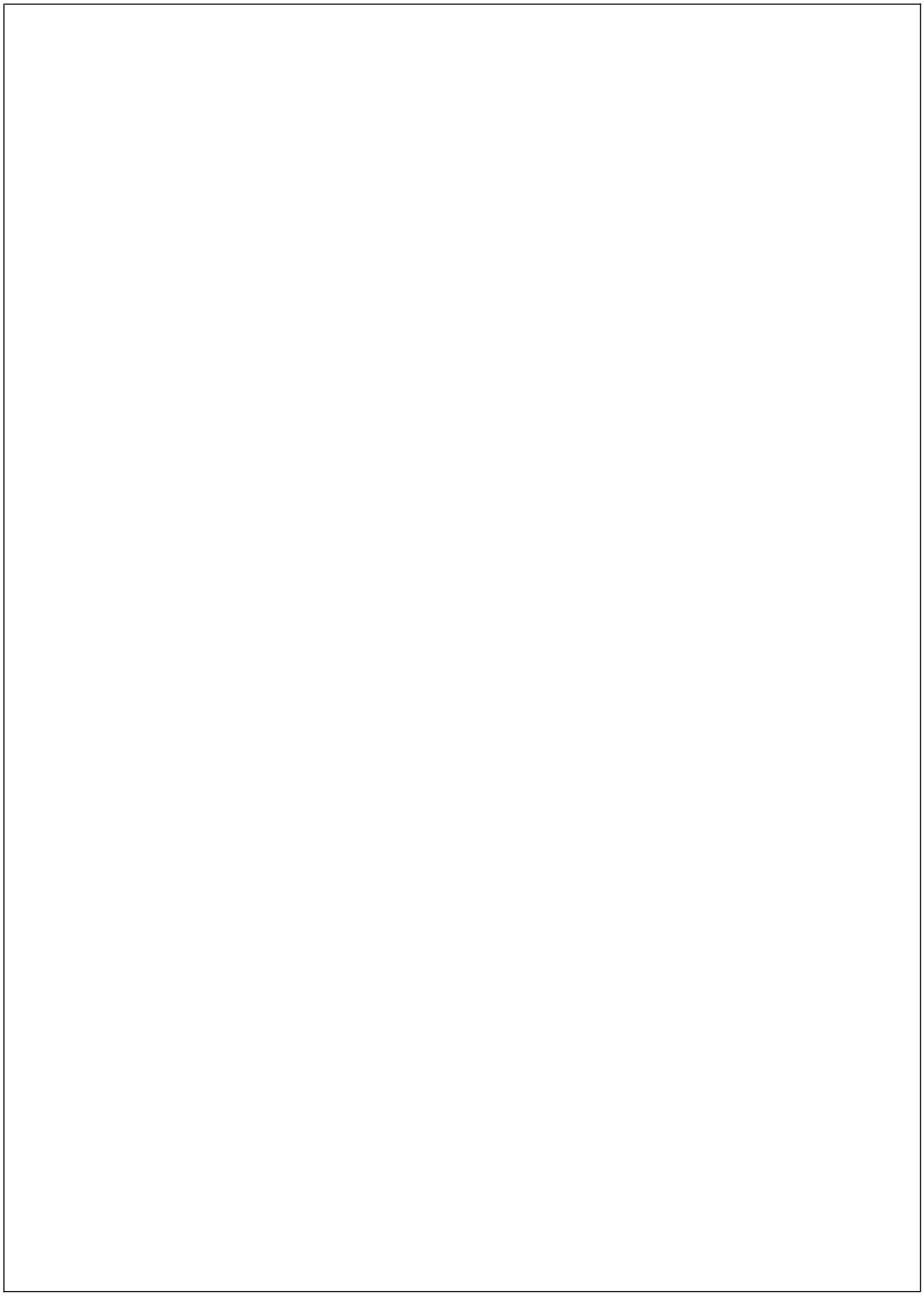


FIGURE 10. Propagation Delay Variation Across Temperature for (a) 74LS00 (b) 74ALS00 and (c) 74HC00



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