安森美半导体
ON Semiconductor®

功率低于75 W、待机能耗极低的固定频率适配器设计及应用

Design and implementation of a fixed-frequency adapter < 75 W with very low power consumption

议程 Agenda

- 新的“能源之星”要求 New ENERGY STAR® requirements
- 符合新规范所需要的特性 Needed features to meet the new specification
- 新的控制器系列NCP1237/38/87/88 New controller family NCP1237/38/87/88
- 设计步骤1：电源段 Design step 1: Power stage
- 设计步骤2：设定补偿 Design step 2: Set the compensations
- 设计步骤3：空载输入能耗 Design step 3: No Load Input Power
- 设计步骤4：磁学 Design step 4: Magnetics
- 设计步骤5：电磁干扰 Design step 5: EMI
- 初步演示板示例 Preliminary demoboard example
- 总结 Summary

EPA 2.0 (外部电源 External Power Supplies)

EPA ENERGY STAR Version 2.0 EPS Voluntary Specification
(Effective November 1, 2008)

Energy-Efficiency Criteria for Ac-Ac and Ac-Dc External Power Supplies in Active Mode: Standard Models

Nameplate Output Power (P_{no})	Minimum Average Efficiency in Active Mode (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.480 * P_{no} + 0.140
> 1 to ≤ 49 watts	≥ [0.0626 * Ln (P_{no})] + 0.622
> 49 watts	≥ 0.870

(此前的1.1版中为>0.84)
(was > 0.84 in previous version 1.1)

Energy Consumption Criteria for No-Load

Nameplate Output Power (P_{no})	Maximum Power in No-Load	
	AC-AC EPS	AC-DC EPS
0 to < 50 watts	≤ 0.5 watts	≤ 0.3 watts
≥ 50 to ≤ 250 watts	≤ 0.5 watts	≤ 0.5 watts

1.1版为<0.5 W
(< 0.5 W in 1.1)
1.1版为<0.75 W
(< 0.75 W in 1.1)

EPS 5.0 (“能源之星”计算机项目要求)

EPS 5.0 (ENERGY STAR® Program Requirements for Computers)

- 定义E_{TEC}为不同类型产品的总能耗 Defines E_{TEC} for different types of products as a Typical Energy Consumption
- 对于台式机和笔记本产品类别而言，TEC由下列公式确定： For the desktop and notebook product categories TEC will be determined by the following formula:

$$E_{TEC} = (8760/1000) * (P_{off} * T_{off} + P_{sleep} * T_{sleep} + P_{idle} * T_{idle})$$

- 其中，所有Px参数均是功率值，单位为瓦(W)；所有Tx参数均是时间值，表示占1年时间的百分比；TEC E_{TEC}以千瓦时(kWh)为单位，表示不同工作模式加权值的每年能耗 where all Px are power values in watts, all Tx are Time values in % of year, and the TEC E_{TEC} is in units of kWh and represents annual energy consumption based on mode weightings
- **轻载能效及空载能耗更为重要 The light load efficiency and no load consumption is more important**

EPS 5.0 (“能源之星”计算机项目要求)(续)
EPS 5.0 (ENERGY STAR® Program Requirements for Computers)

E_{TEC}台式机及笔记本要求
E_{TEC} requirement desktops and notebooks

	台式计算机及 一体式计算机(kWh) Desktops and Integrated Computers (kWh)	笔记本计算机(kWh) Notebook Computers (kWh)
总能耗 TEC (kWh)	A类 Category A: ≤ 148.0 B类 Category B: ≤ 175.0 C类 Category C: ≤ 209.0 D类 Category D: ≤ 234.0	A类 Category A: ≤ 40.0 B类 Category B: ≤ 53.0 C类 Category C: ≤ 88.5

- 生效时间：2009年7月1日(例外：游戏机相关要求自2010年7月1日生效)
  Effective from July 1, 2009 (except: game consoles from July 1, 2010)

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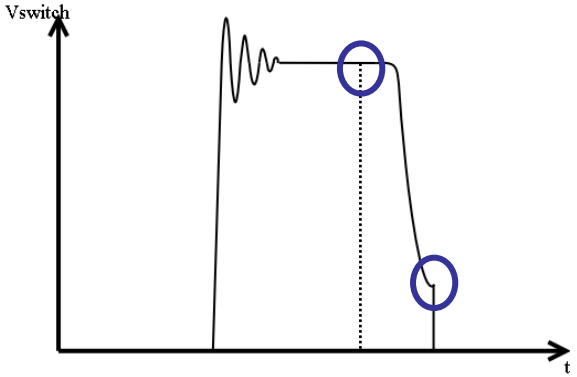
提升效率 Improving Efficiency

- 损耗来源 Sources of loss:
  - 开关损耗 Switching losses:

$$P_{loss(switching)} = \frac{1}{2} \cdot C_{DRAIN} \cdot V_{DRAIN(turn-off)}^{2} \cdot F_{SW}$$

  - 由泄漏电感导致的损耗 Losses caused by leakage inductance:

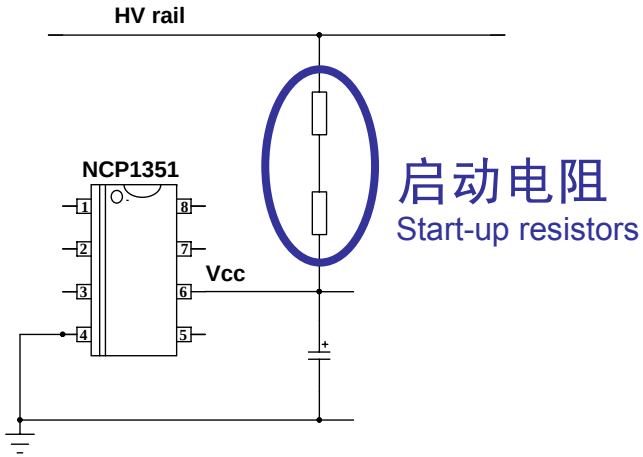
$$P_{loss(leak)} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^{2} \cdot F_{SW}$$



- 提升能效的途径 Ways to improve efficiency:
  - 降低开关频率F_{SW} Lower the switching frequency F_{SW} ➔ 轻载时频率反走 frequency foldback at light loads
  - 降低关闭时的漏极电压 Lower the Drain voltage at turn-off ➔ 谷底开关 valley switching

降低空载能耗 Reducing No-load Input Power

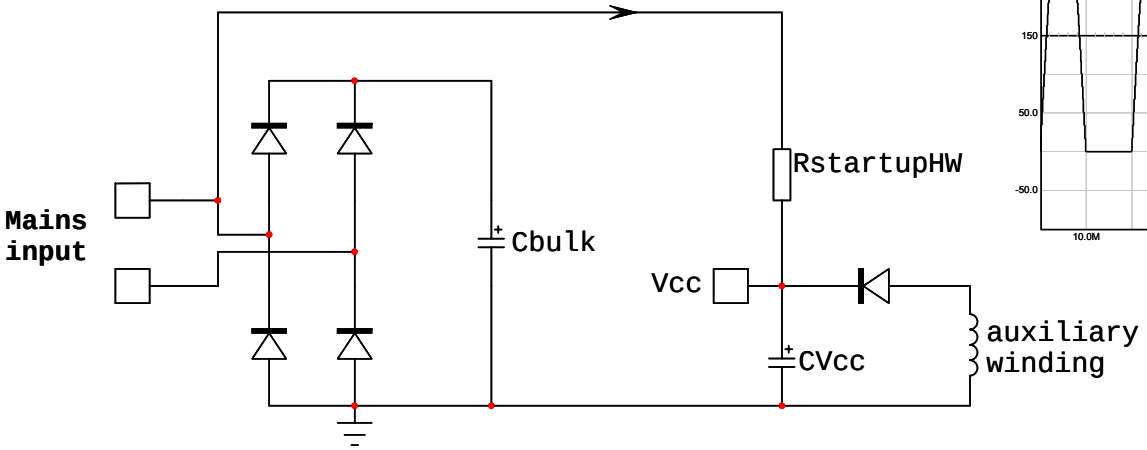
- 启动电路静态损耗 Static losses in the start-up circuit:
  - 启动电阻持续从大电容消耗电流 Start-up resistor permanently drawing current from the bulk capacitor
- 降低启动电路损耗的途径 Ways to lower the start-up circuit losses
  - 采用外部启动电阻 With external start-up resistor ➔ 启动电流极低 Extremely low start-up current
  - 集成启动电流源 Integrated start-up current source ➔ 关闭时泄漏极低 Extremely low leakage when off
  - 连接启动电路至半波整流交流输入 Connect the start-up circuit to the half-wave rectified ac input

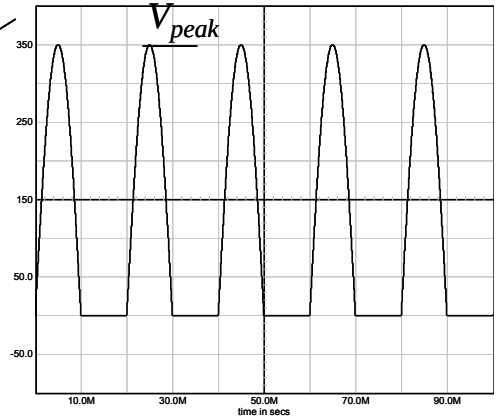


降低空载输入能耗 Reducing No-load Input Power

选自大电容连接
Selected from bulk connection

$$R_{startupHW} = \frac{R_{startup}}{\pi}$$





$$P_{R_{startupHW}} = \frac{P_{R_{startup}}\,\pi}{4}$$

→ 降低21%的能耗 Brings a 21% reduction in power

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NCP1237/38/87/88

2010年Q1上市
Avail. in Q1 2010

价值主张 Value Proposition

The NCP1237/38/87/88 series represents the next generation of fixed frequency PWM controllers. It targets applications where cost-effectiveness, reliability, design flexibility and low standby power are compulsory.

独特特性 Unique Features

- High-voltage current source with built-in Brown-out and mains OVP
- Freq. reduction in light load conditions and skip mode
- Adjustable Over Power Protection

优势 Benefits

- Fewer components and rugged design
- Extremely low no-load standby power
- Simple option to alter the max. peak current set point at high line

其它特性 Others Features

- Latch-off input for severe fault conditions, allowing direct connection of NTC
- Timer-based protection: auto-recovery or latched
- Dual OCP option available
- Built-in ramp compensation
- Frequency jittering for a softened EMI signature
- Vcc operation up to 30 V

市场及应用 Market & Applications

- AC-DC adapters for notebooks, LCD monitor, game console, printers
- CE applications (DVD, STB)

应用数据 Application Data



	DSS	Dual OCP	Latch	Auto Recovery
NCP1237A	Yes	Yes	Yes	
NCP1237B	Yes	Yes		Yes
NCP1238A	Yes	No	Yes	
NCP1238B	Yes	No		Yes
NCP1287A	HV only	Yes	Yes	
NCP1287B	HV only	Yes		Yes
NCP1288A	HV only	No	Yes	
NCP1288B	HV only	No		Yes

根据终端应用需求提供不同选择 Various options available depending upon end applications needs

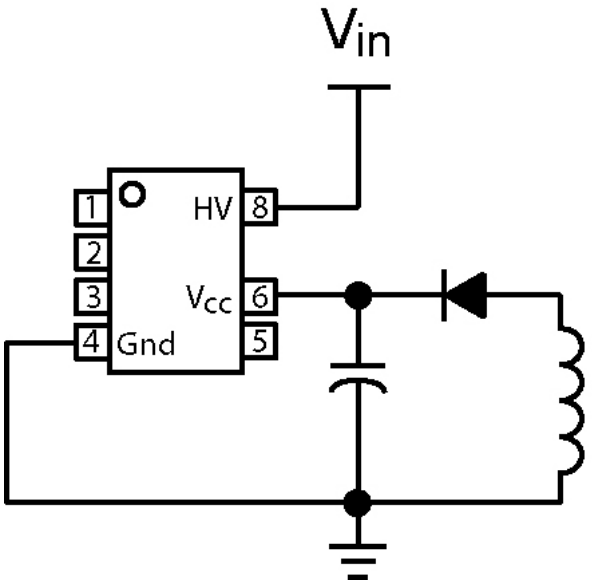
订购及封装信息 Ordering & Package Information

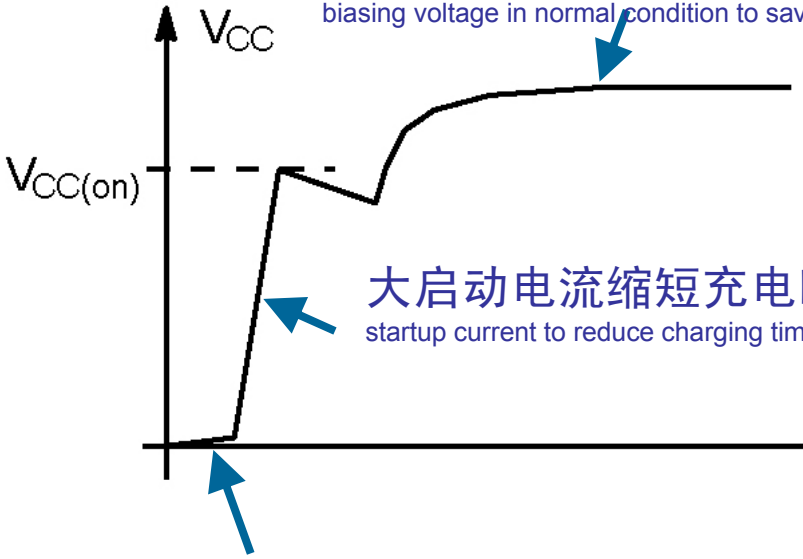
- NCP1237/38xDR2G - NCP1287/88xDR2G
- SOIC-7 2500p per reel

Pb O, DW

NCP1237/38/87/88-内置启动场效应管

NCP1237/38/87/88 – Built-in Startup FET





在正常工作条件下反激辅助绕组提供偏置电压以省电 A flyback auxiliary winding supplies biasing voltage in normal condition to save power

大启动电流缩短充电时间 High startup current to reduce charging time

若Vcc引脚对地短路，低初始启动电流防止电路受到损耗 Low initial startup current to prevent damage if Vcc pin is shorted to ground.

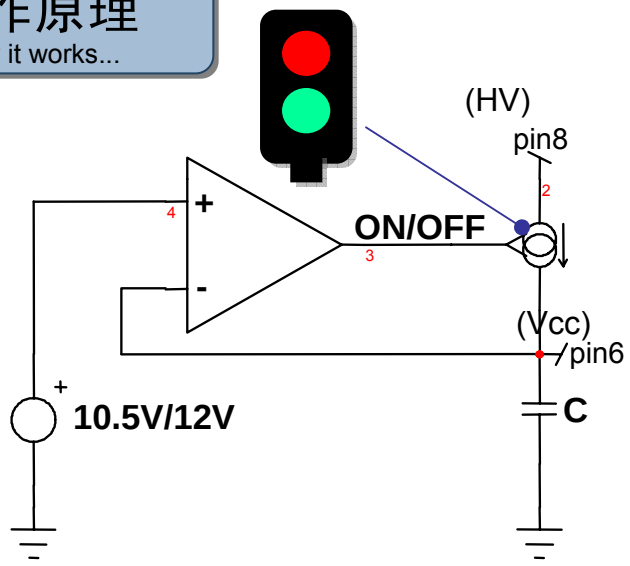
无启动电阻！
No startup resistor!

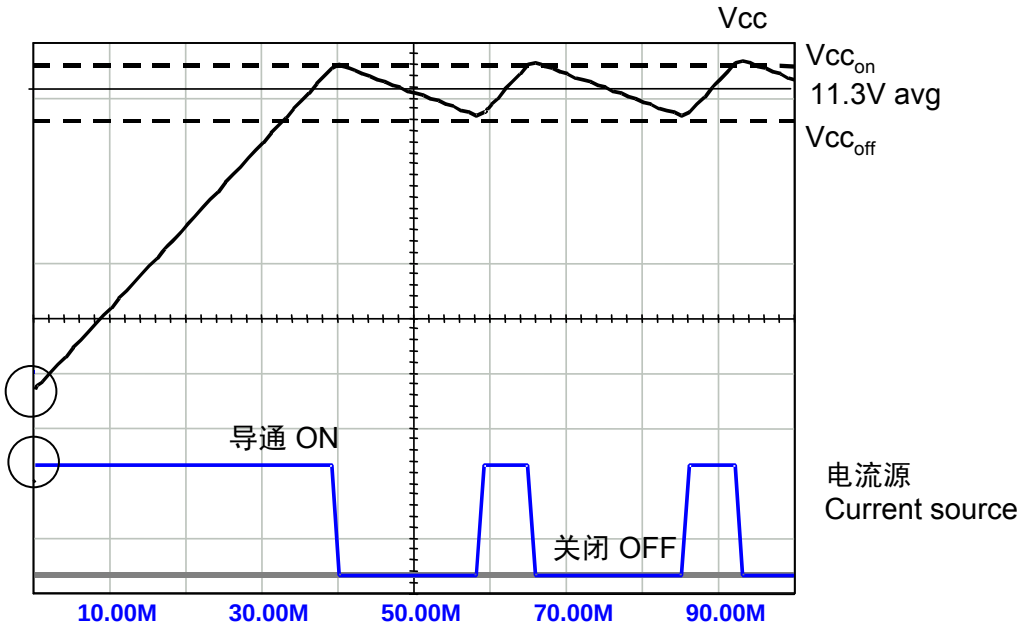
节省电路板空间并省电
Saves PCB area & saves power

NCP1237/38/87/88-动态自供电(可选功能)

NCP1237/38/87/88 – Dynamic Self Supply (optional)

工作原理
How it works...





电源导通 Power ON → 电流源导通 Current Source turns ON → V_{CC}上升； 无输出脉冲 V_{cc} is rising; no output pulses

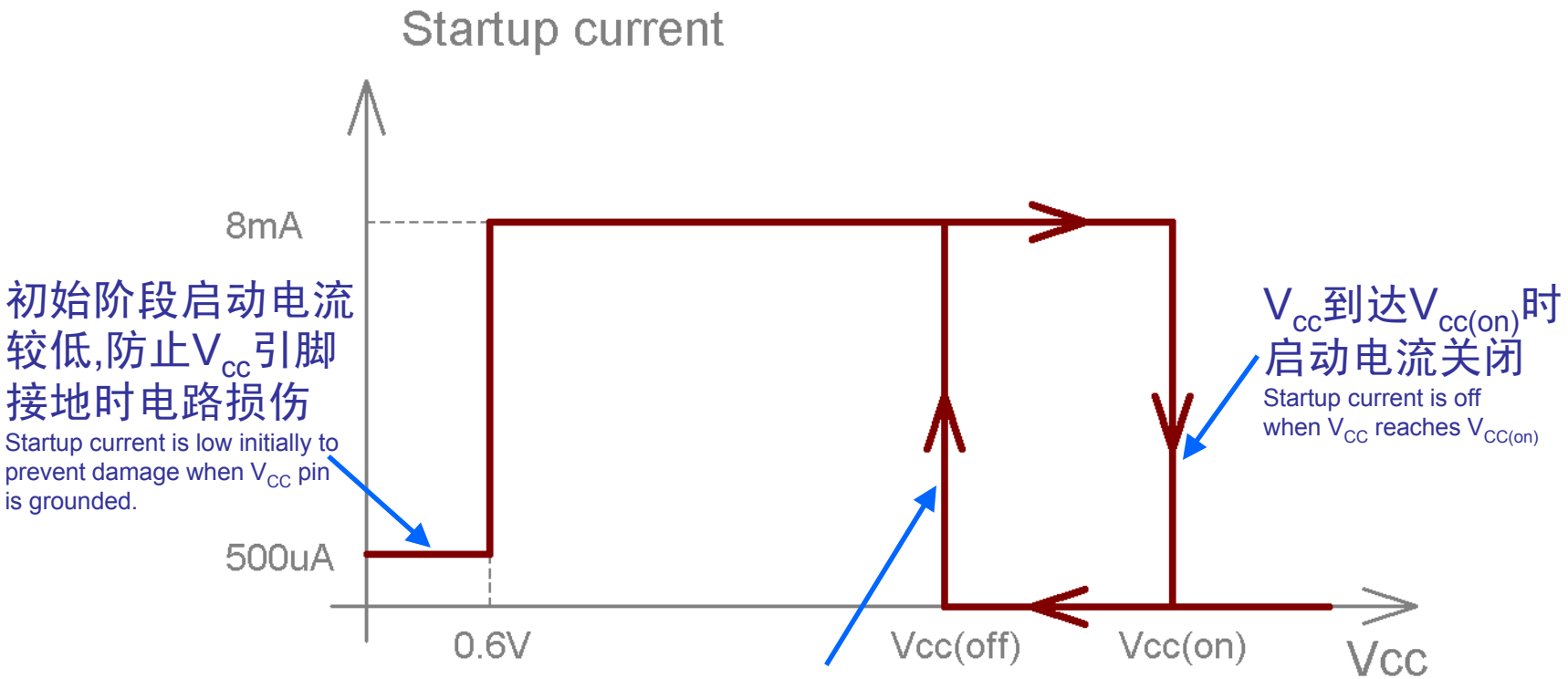
V_{CC}到达$V_{CC(on)}$ V_{cc} reaches $Vcc_{(on)}$ → 电流源关闭 Current Source turns OFF → V_{cc}下降;输出脉冲 V_{cc} is falling; output is pulsing

V_{cc}下降至$V_{cc(off)}$ V_{cc} falls to $Vcc_{(off)}$ → 电流源导通 Current Source turns ON → V_{cc}上升;输出脉冲 V_{cc} is rising; output is pulsing

动态自供电 Dynamic Self-Supply ⇒ 无需辅助绕组! No need of auxiliary winding!

NCP1237/38/87/88-双启动电流电平

NCP1237/38/87/88 – Dual startup current level



初始阶段启动电流较低,防止V_{cc}引脚接地时电路损伤

Startup current is low initially to prevent damage when V_{CC} pin is grounded.

V_{cc}到达$V_{cc(on)}$时启动电流关闭

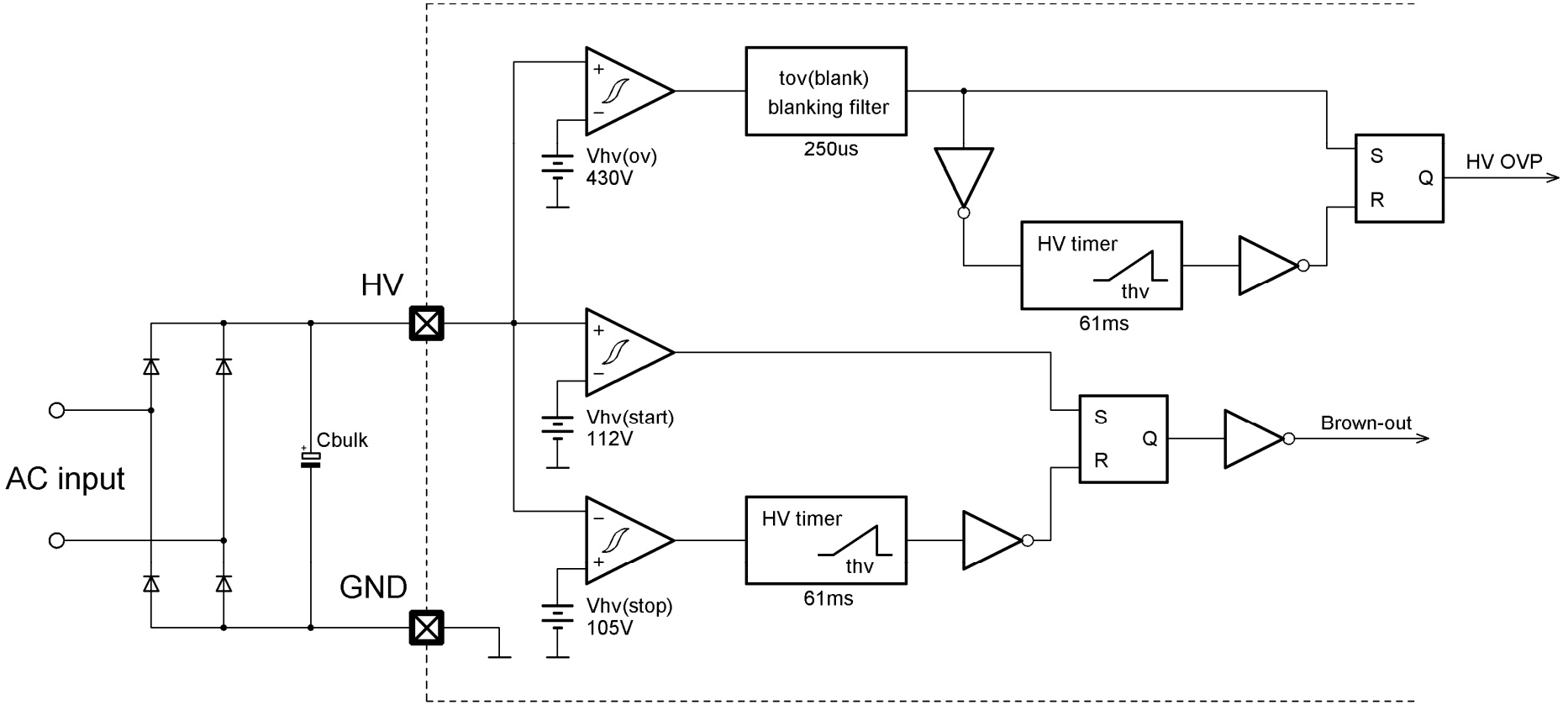
Startup current is off when V_{CC} reaches $V_{CC(on)}$

V_{cc}降至$V_{cc(off)}$时启动电流激发至较高电平。因此，启动后电压始终不会降低低于$V_{cc(off)}$。

Startup current is activated when V_{CC} drops to $V_{CC(off)}$. Hence, the voltage never drops below $V_{CC(off)}$ after startup.

NCP1237/38/87/88-输入欠压及主电源过压保护

NCP1237/38/87/88 – Brown-out and Mains OVP



检测不受HV引脚纹波影响

Detection independent of Ripple on HV pin

能连接至半波整流交流电路

Can be connected to the half-wave rectified ac line

NCP1237/38/87/88-输入欠压及主电源过压保护

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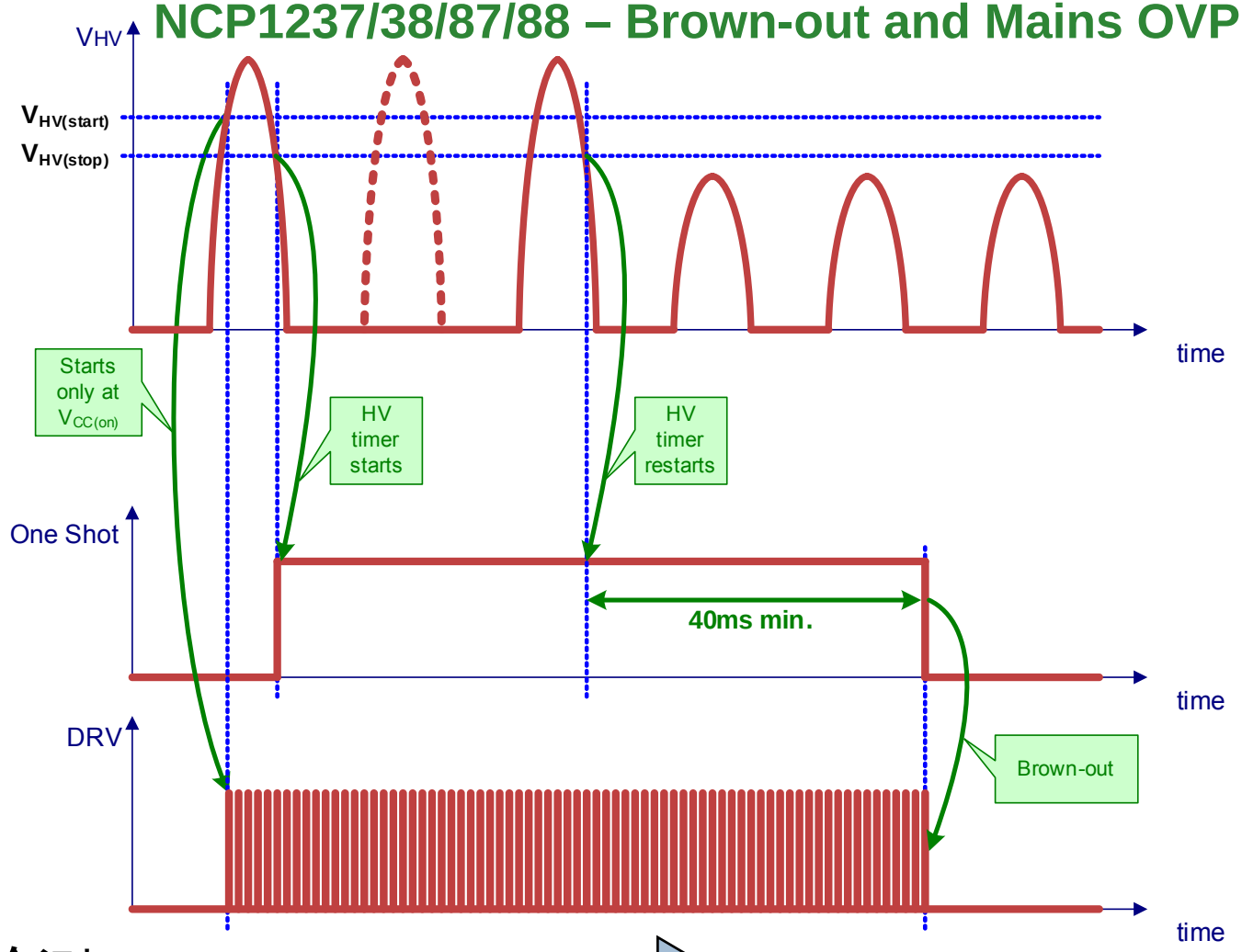


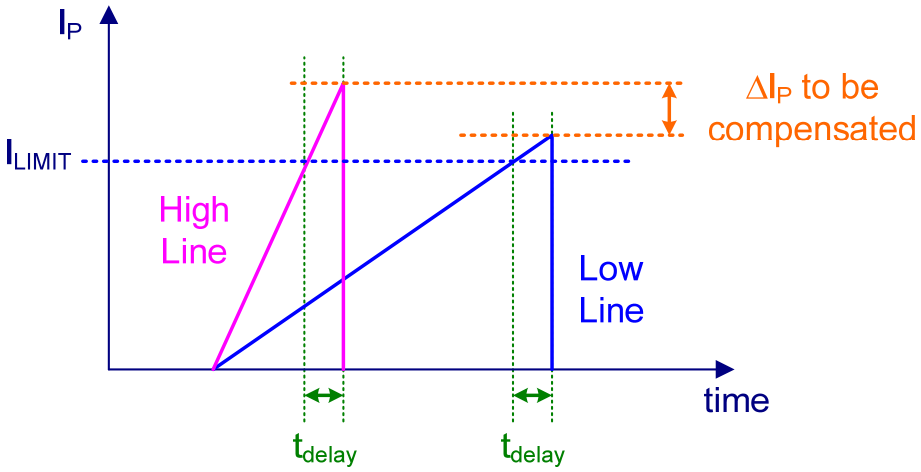
定时检测 Timer-based detection

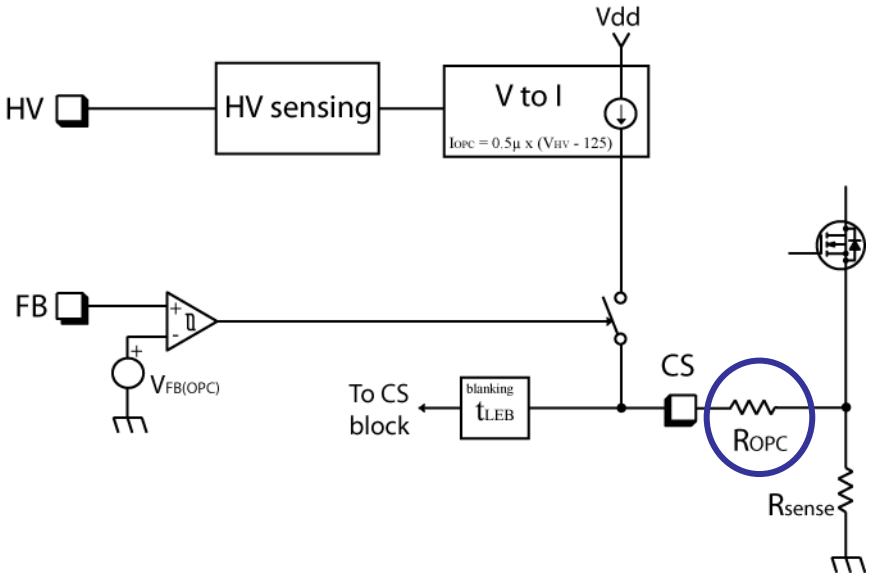
略过完整线路周期内的压降

Passes full line cycle drop-out

NCP1237/38/87/88-过载保护

NCP1237/38/87/88 – Over Power Protection





需要补偿传播延迟效应

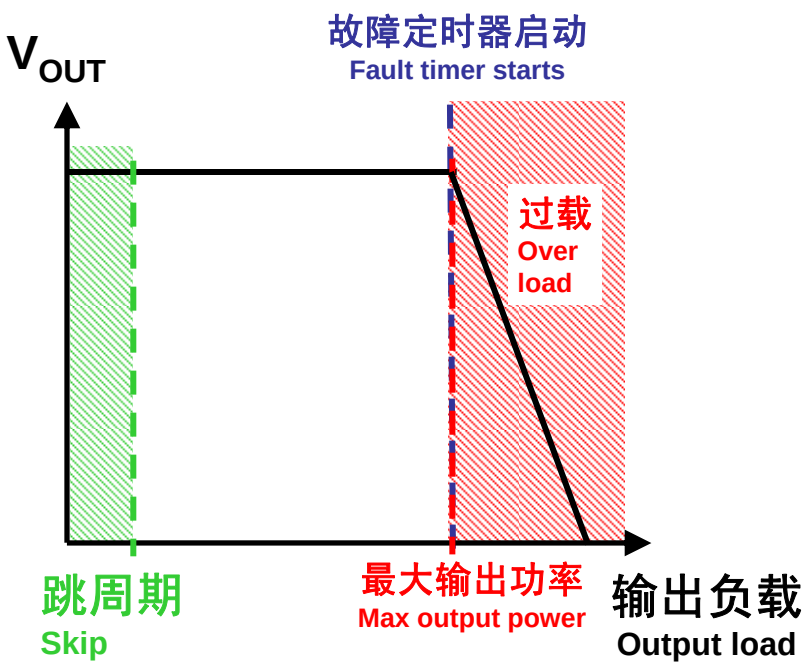
Need to compensate for the effect of the propagation delay

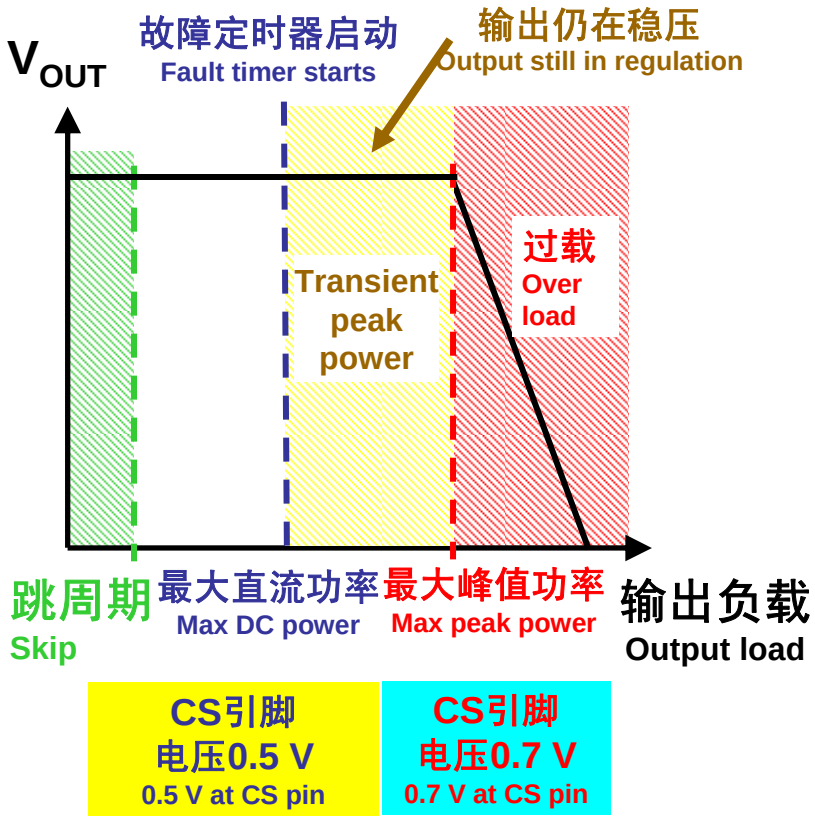
补偿电流电流感测(CS)信号上产生偏置 The compensation Current creates an offset on the Current Sense signal

过载保护 Over Power Protection ⇒ 最大输出功率钳位 Maximum output power clamped

NCP1237/38/87/88-双过流保护阈值

NCP1237/38/87/88 – Dual OCP threshold





适应大输出功率瞬态条件

Accommodates large output power transients

适合打印机应用

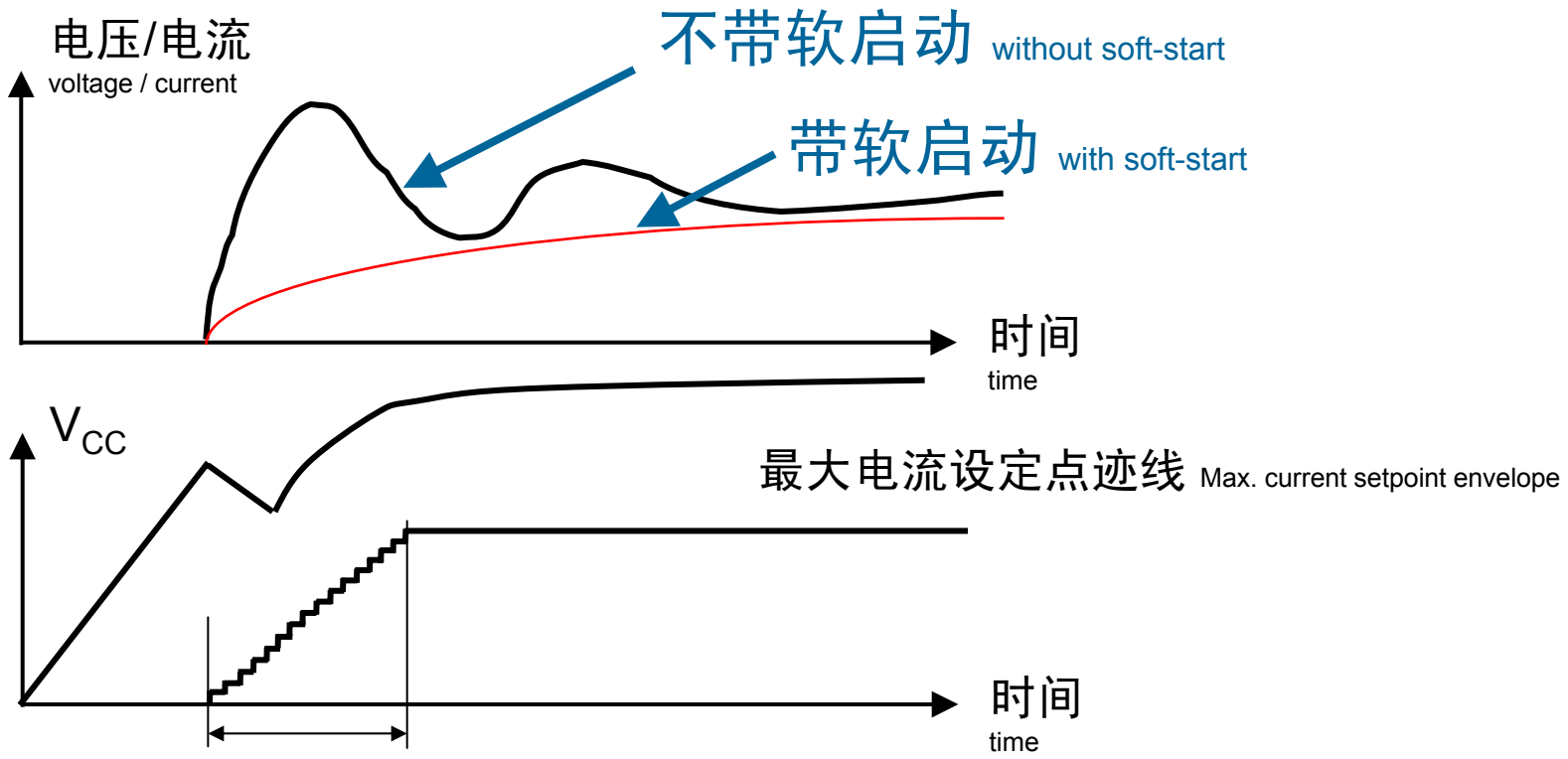
Suitable for printers

这些保护功能使用递增/递减计数器,类似于经典的模拟集成功能

These protections use the Up/Down counters, like classical analog integration.

NCP1237/38/87/88-4 ms软启动

NCP1237/38/87/88 – 4 ms Soft Start

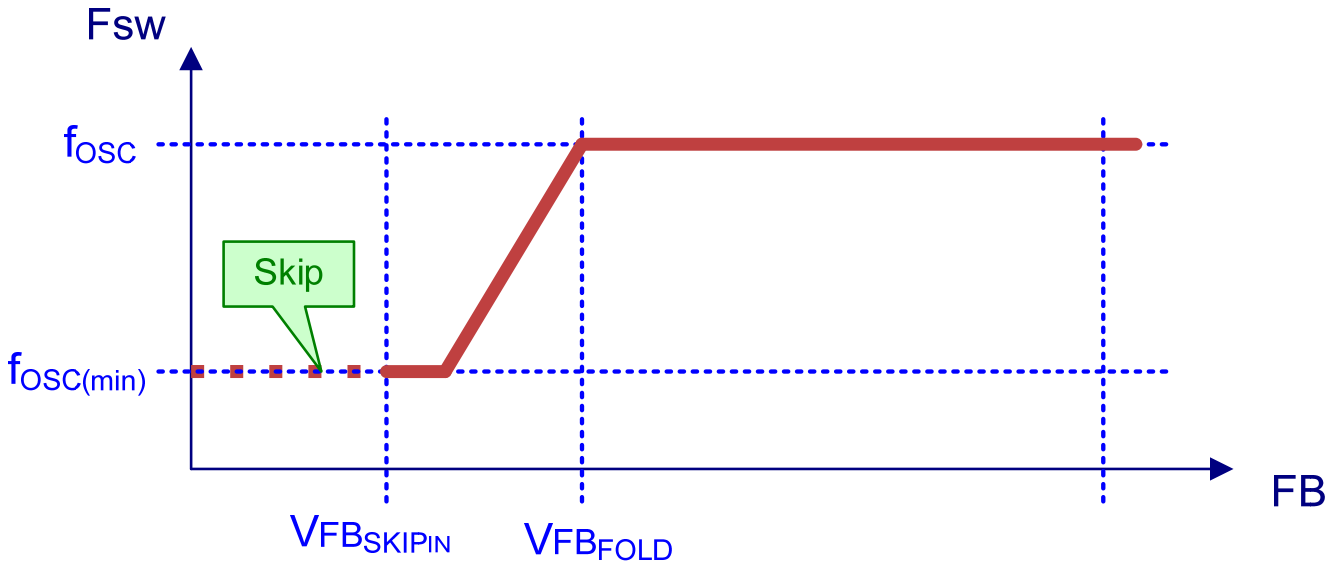


4 ms时间的“数字”软启动工作 4 ms “digital” soft-start operation

4 ms软启动 4 ms Soft Start ⇒ 无应力启动相位 Stressless start-up phase

NCP1237/38/87/88-频率反走

NCP1237/38/87/88 – Frequency Foldback



轻载时开关频率降低
Switching frequency lowered at light load

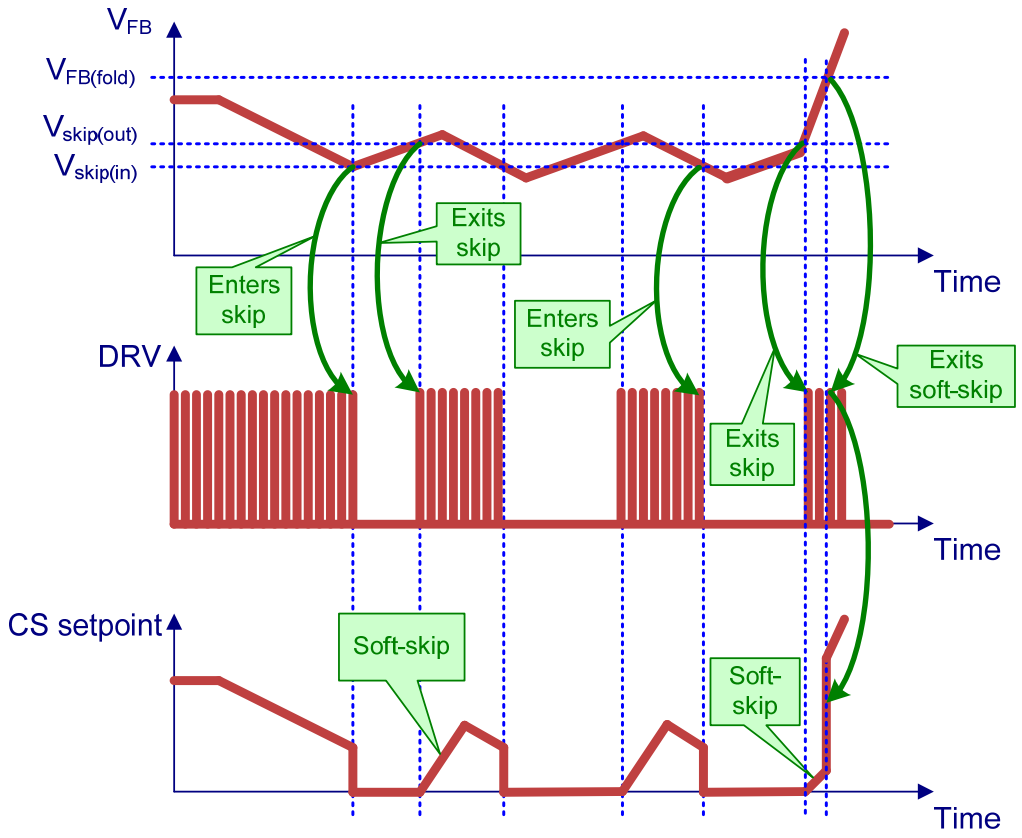
提升能效
Increased efficiency

开关频率在25 kHz钳位
Switching frequency clamped at 25 kHz

没有可听噪声
No audible noise

NCP1237/38/87/88 –从待机模式恢复

NCP1237/38/87/88 – Recover from Standby



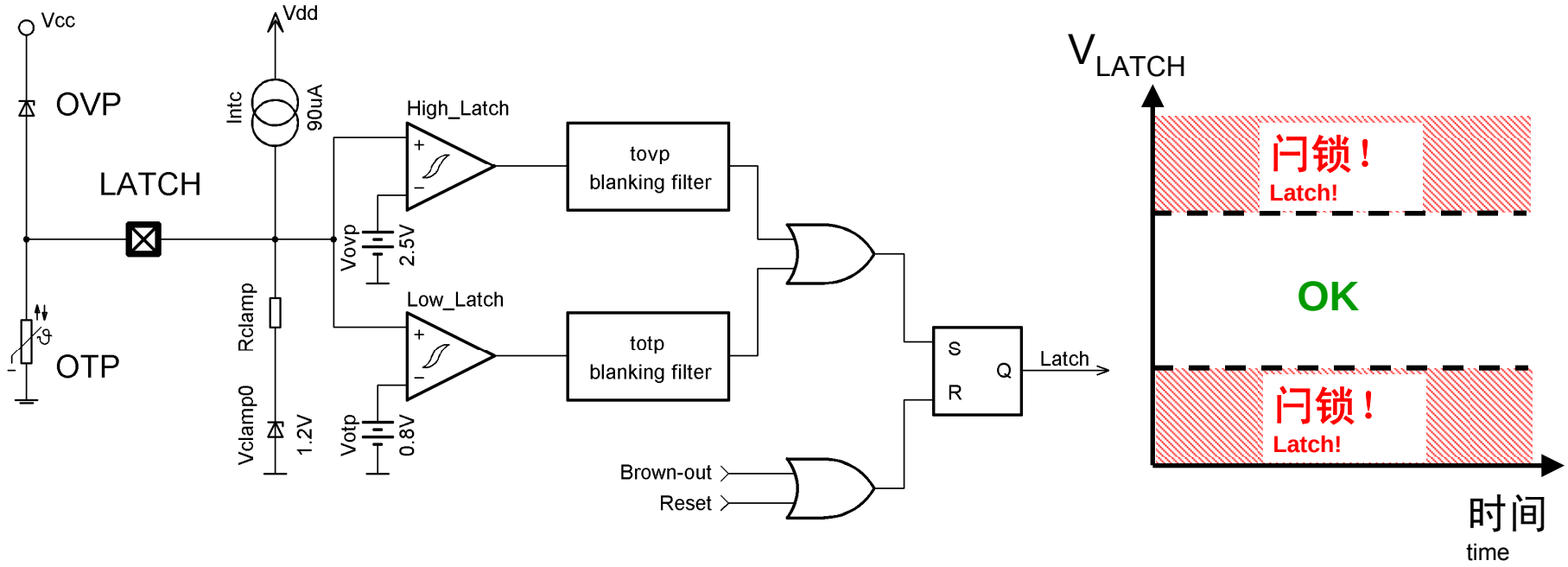
反馈引脚上的电压一达到TLD阈值，就离开软跳周期模式 Soft-Skip mode is left as soon as the voltage on the feedback pin reaches the TLD threshold

瞬态负载检测(TLD)功能
Transient Load Detect Function (TLD)

改善负载瞬态响应时间
Improved Load Transient response time

NCP1237/38/87/88-闩锁保护

NCP1237/38/87/88 – Latch-off Protection



负温度系数(NTC)热敏电阻能直接连接至IC

An NTC thermistor can be directly connected to the IC

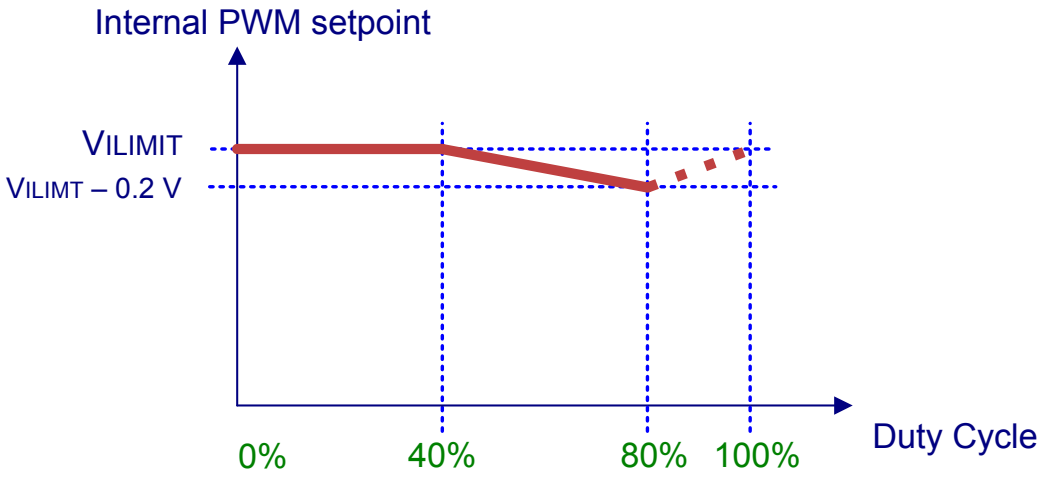
需要的外部元件较少

Less external components needed

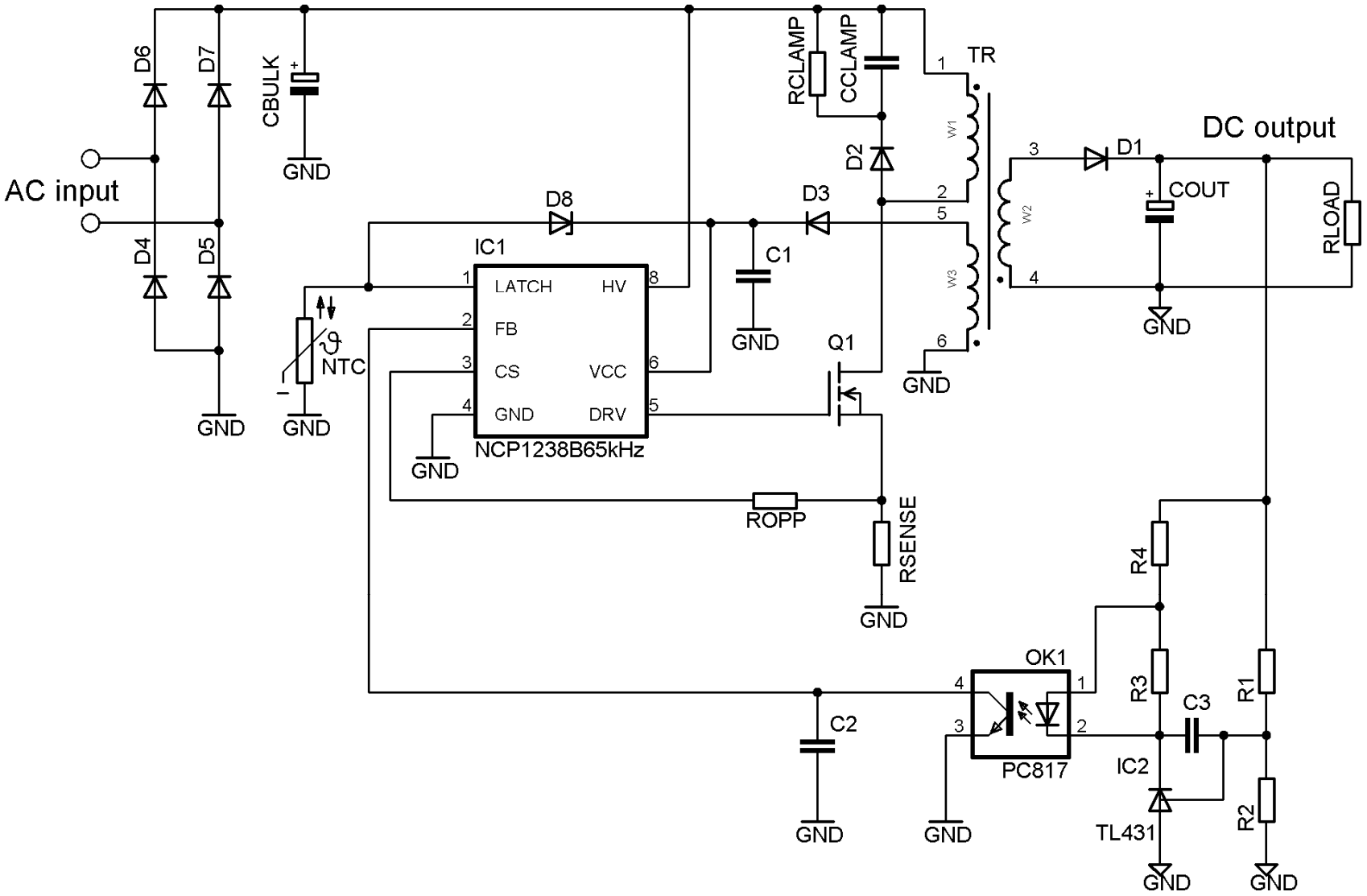
NCP1237/38/87/88-斜坡补偿

NCP1237/38/87/88 – Slope compensation

- 内置斜坡补偿，不需外部设定 There is a built in slope compensation with no external setting
- 若占空比高于40%则激发内置斜坡补偿 The internal slope compensation is activated if the duty cycle is higher than 40%
- CS引脚观测到的斜坡补偿额度是5 mV/% The amount of slope compensation is 5mV/% observed at CS pin



应用电路图 Application schematic



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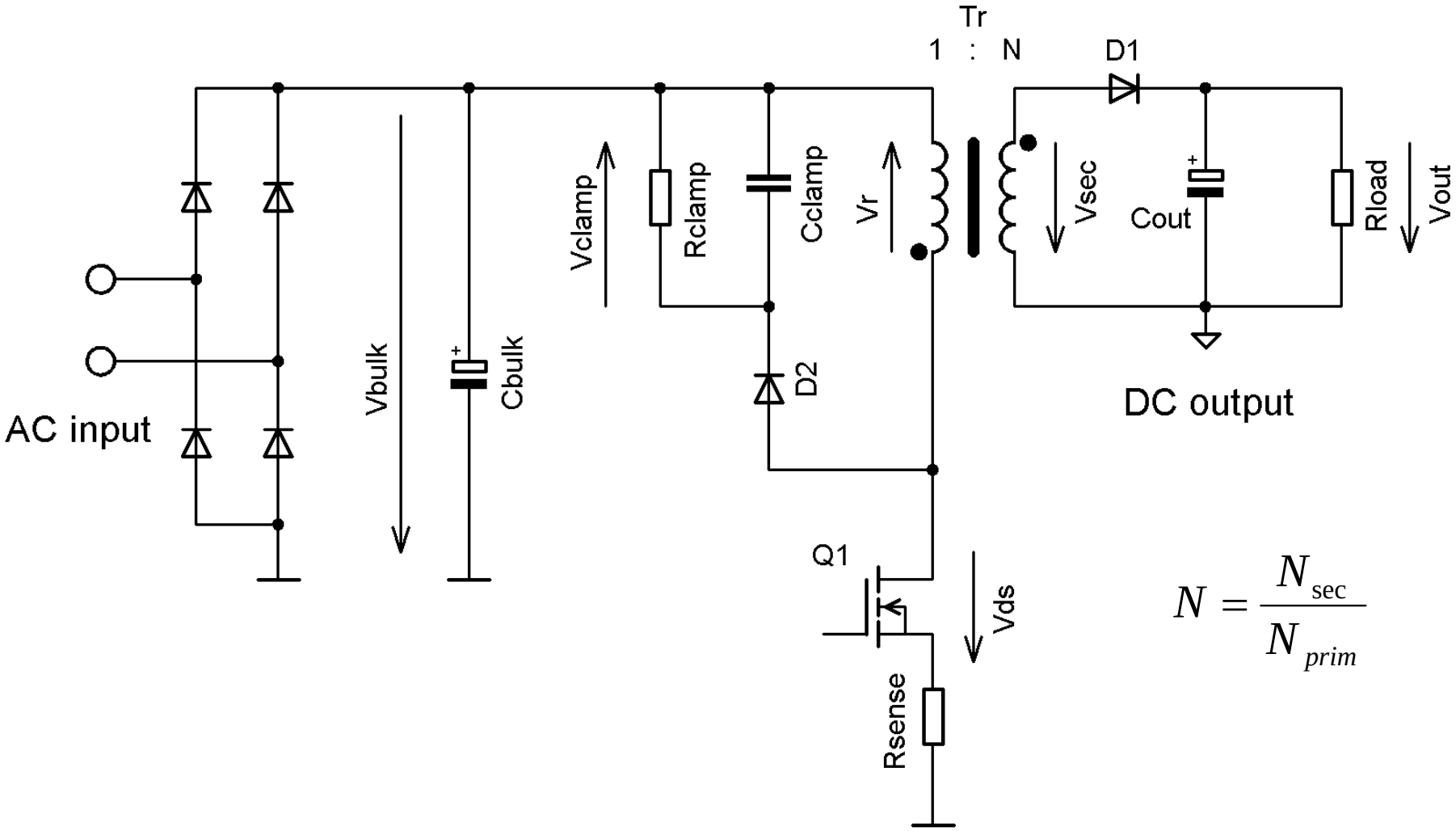
电源段：反激转换器电路图

Power stage: Schematic of flyback converter



$$N = \frac{N_{sec}}{N_{prim}}$$

电源段设计：大电容
Power stage design: Bulk capacitor

- 输出功率 Output power P_{out}

$$P_{out} = V_{out} \cdot I_{out}$$

- 平均输入电流 Average input current $I_{in,avg}$

$$I_{in,avg} = \frac{P_{in}}{V_{bulk,\min}}$$

- 预估输入功率 Estimation of input power P_{in}

$$P_{in} = \frac{P_{out}}{\eta}$$

根据EPA相关标准来预估能效

η Estimate the η based on the EPA standard

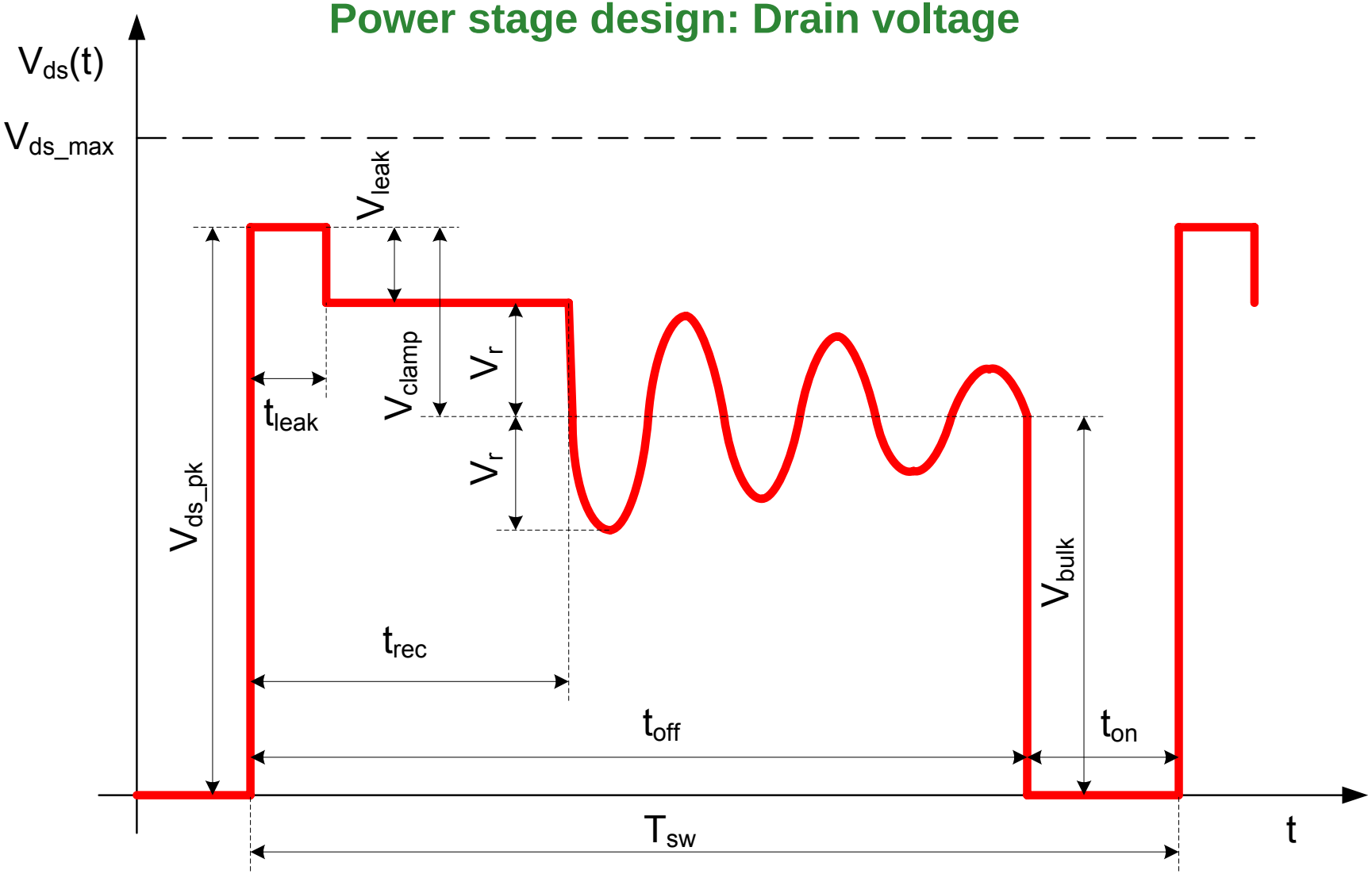
- 计算大电容值 Bulk capacitor value C_{bulk}

$$C_{bulk} = \frac{I_{in,avg} \cdot t_{dis}}{\Delta V_{bulk}}$$

使用 Use t_{dis}=8.5 ms

电源段设计：V_{ds}电压

Power stage design: Drain voltage



电源段设计：变压器匝数比
Power stage design: Transformer ratio

变压器匝数比-考虑所使用Q1的V_{DSS} Transformer ratio – consideration of the V_{DSS} of used Q1

$$N = \frac{k_C \cdot \left(V_{out} + V_{f,diode}\right)}{0.85 \cdot V_{DS,\max} - 20V - V_{bulk,\max}} \qquad k_C = \frac{V_{clamp}}{V_r}$$

20 V表示为钳位二极管启动过冲提供裕量 The 20V means margin for clamping diode turning-on overshoot.

次级到初级的反射电压V_r Reflected voltage V_r at primary from secondary

$$V_r = \frac{V_{out} + V_{f,diode}}{N} \qquad N = \frac{N_{\sec}}{N_{prim}}$$

最大占空比DC_{max} Maximum duty cycle DC_{max}

连续导电模式(CCM)工作
In CCM operation:

$$DC_{\max} = \frac{V_r}{V_r + V_{bulk,\min}}$$

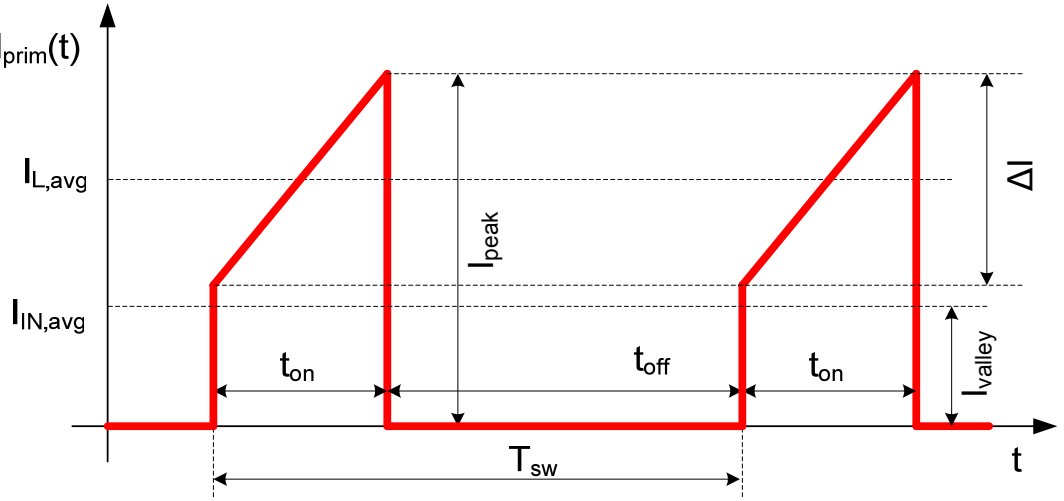
不连续导电模式(DCM)工作与N无关
In DCM operation doesn't depend on N:

$$DC_{\max} = \frac{V_{out}}{V_{bulk,\min}} \cdot \sqrt{\frac{2 \cdot L_{prim} \cdot F_{sw}}{R_{load,\min}}}$$

电源段设计：电流纹波
Power stage design: Current ripple

反射到初级绕组的平均共用电流$I_{L,avg}$ The average shared transformer current reflected to primary winding $I_{L,avg}$

$$I_{L,avg} = \frac{I_{in,avg}}{DC_{\max}}$$



选择相关的纹波 δ I_r：它影响CCM或DCM工作 Choose the relative ripple δ I_r: it affects the operation in the CCM or DCM

- 通用交流输入设计使用的 δ I_r范围为0.5至1.0 For universal AC input design use the δ Ir in range 0.5 to 1.0
- 欧洲交流输入设计使用的 δ I_r范围为0.8至1.6 For European AC input use the δ Ir in range 0.8 to 1.6

$$\delta I_r = \frac{\Delta I}{I_{L,avg}}$$

$$\Delta I = \delta I_r \cdot I_{L,avg}$$

$$\Delta I = I_{peak} - I_{valley}$$

$$I_{peak} = I_{L,avg} \cdot \left(1 + \frac{\delta I_r}{2}\right)$$

$$I_{valley} = I_{L,avg} \cdot \left(1 - \frac{\delta I_r}{2}\right)$$

电源段设计：初级电感
Power stage design: Primary inductance

变压器初级绕组电感 Transformer primary winding inductance L_{prim}

$$L_{prim} = \frac{V_{bulk,\min} \cdot DC_{\max}}{F_{sw} \cdot \Delta I}$$

流过初级绕组的电流的最大均方根值 Maximum RMS value of the current flowing through primary winding $I_{prim,RMS}$

$$I_{primRMS} = \sqrt{DC_{\max} \cdot \left(I_{peak}^{\ 2} - I_{peak} \cdot \Delta I + \frac{\Delta I^2}{3} \right)}$$

流过次级绕组的电流的最大均方根值 Maximum RMS value of the current flowing through secondary winding $I_{sec,RMS}$

$$I_{\sec,peak} = \frac{I_{peak}}{N} \qquad \Delta I_{\sec} = \frac{\Delta I}{N}$$

$$I_{\sec RMS} = \sqrt{(1 - DC_{\max}) \cdot \left(I_{\sec,peak}^{\ 2} - I_{\sec,peak} \cdot \Delta I_{\sec} + \frac{\Delta I_{\sec}^{\ 2}}{3} \right)}$$

电源段设计：Q1选择
Power stage design: Q1 selection

Q1导电损耗应该是接近输出功率(Pout)的1% Conduction loss at Q1 should be approx. 1% of the Pout

$$R_{DSon} \le \frac{P_{out}}{100 \cdot I_{prim,RMS}^{2}}$$

然后根据这些参数来选择恰当的器件： Then the right device is chosen by parameters

V_{DSmax}, I_{peak}, t_{on}, t_{off}

电流感测电阻R_{sense}的选择 Current sensing resistor R_{sense} selection

$$R_{sense} = \frac{V_{ILIM}}{1.1 \cdot I_{peak}} \qquad P_{sense} = I_{primRMS}^{2} \cdot R_{sense}$$

因数1.1表示为L_{prim}提供10%的裕量，也是另一项参数扩展，能够提供最大的功率 *The 1.1 factor means 10% margin for L_{prim} and another parameters spread, to be able deliver maximum power.*

电源段设计：次级整流
Power stage design: Secondary rectification

二极管D1选择 D1 selection:

D1反射电压 Reflected voltage across D1

$$PIV = V_{bulk,\max} \cdot N + V_{out}$$

D1选择的其它重要参数是$I_{sec,peak}$、I_{out}及快速和软恢复 The next important parameters for D1 selection are $I_{sec,peak}$, I_{out} and the fast and soft recovery

输出电容Cout选择 Cout selection:

最小输出电容C_{out}值 Minimum C_{out} value

$$C_{out} \geq \frac{I_{out} \cdot DC_{\max}}{V_{out,ripple} \cdot F_{sw}}$$

C_{out}允许的最大等效串联电阻(ESR)
The maximum allowed ESR of C_{out}

$$ESR \leq \frac{V_{out,ripple}}{I_{\sec,peak}}$$

主要部分
Dominant part

$$I_{Cout,rms} = \sqrt{I_{\sec,rms}^{\ 2} - I_{out}^{\ 2}}$$

建议使用更大的并联C_{out}，降低输出电压纹波 it is recommended to use more parallel C_{out} for lowering the output voltage ripple.

电源段设计：钳位网络
Power stage design: Clamping network

瞬态电压抑制器(TVS)-抑制器中损耗的功率 TVS – loses in the suppressor:

空载条件下更佳 better at no load conditions

$$P_{clamp} = E_{clamp} \cdot F_{sw} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^{2} \cdot F_{sw} \cdot \frac{V_{clamp}}{V_{clamp} - V_r}$$

RCD钳位-一阶迭代

RCD clamp – 1st iteration:

电磁干扰(EMI)响应更佳 better EMI response

$$R_{clamp} = \frac{2 \cdot V_{leak} \cdot V_{clamp}}{L_{leak} \cdot I_{peak}^{2} \cdot F_{sw}}$$

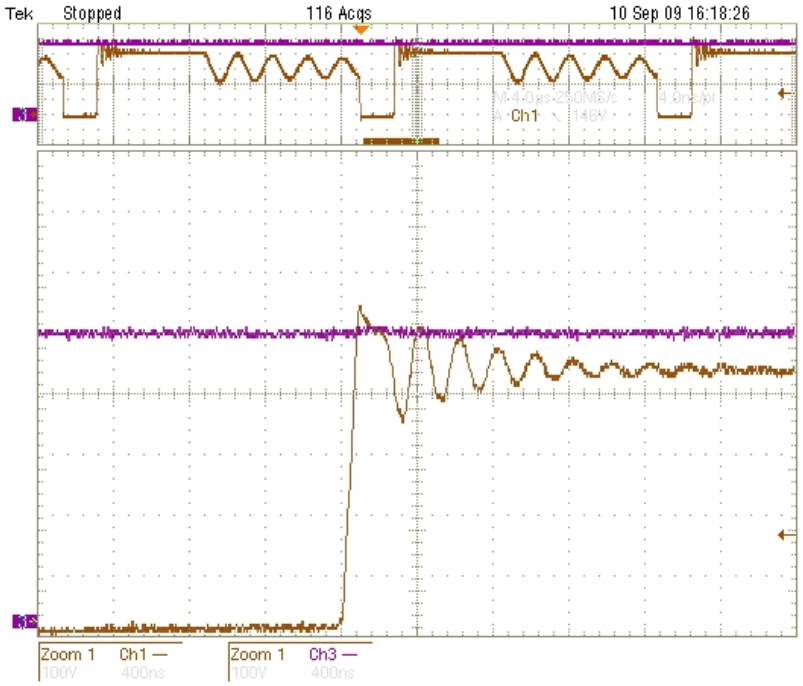
$$P_{clamp} = \frac{V_{clamp}^{2}}{R_{clamp}}$$

$$C_{clamp} > \frac{V_{clamp}}{V_{ripple} \cdot R_{clamp} \cdot F_{sw}}$$

需要针对空载能耗及慢钳位二极管D2损耗来优化这些值 **These values need to be optimized for the no load consumption and losses in slow clamping diode D2**

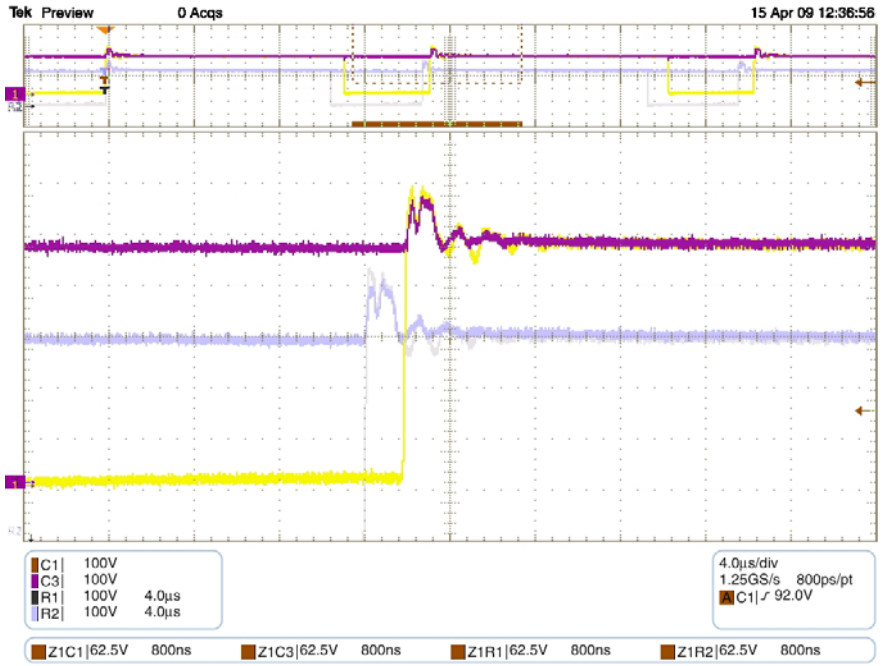
TVS钳位与RCD钳位比较

TVS vs RCD clamp comparison



钳位时TVS漏电压振铃

Drain voltage ringing with TVS as clamp



钳位时RCD漏电压振铃

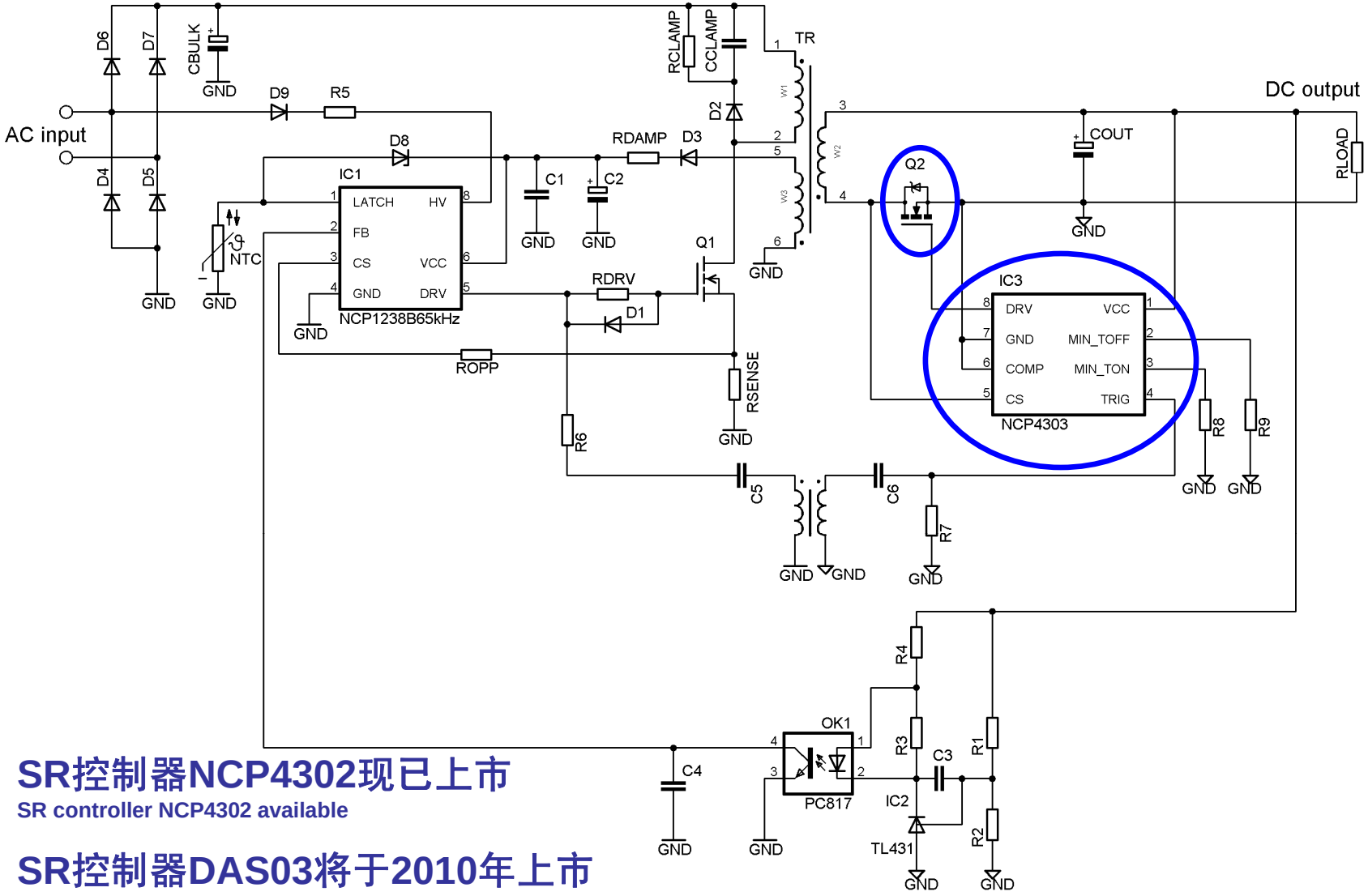
Drain voltage ringing with RCD as clamp

所用钳位中的不同R_{damp}

Different R_{damp} in clamp used

Ch1 – 漏电压 Drain, Ch3 – 钳位节点 Clamp node

同步整流(SR) Synchronous rectification



- **SR控制器NCP4302现已上市**
  SR controller NCP4302 available
- **SR控制器DAS03将于2010年上市**
  SR controller DAS03 coming in 2010

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过载补偿(OPC)
Over power compensation

过载补偿影响初级峰值电流，这电流由下述公式确定 The overpower compensation affects the primary peak current, by the following formula:

$$I_{PEAK} = \frac{V_{CS\,\mathrm{int}}}{R_{sense}} + V_{bulk} \cdot \left(\frac{t_{PROP}}{L_P} - g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \right) + V_{off} \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}}$$

然后能以下述公式计算过载补偿电阻值 Then the overpower compensation resistor can be calculated:

$$R_{OPP} = \frac{t_{PROP} \cdot R_{sense}}{L_P \cdot g_{OPP}}$$

过载补偿电阻仅影响I_{peak}值，但在连续导电模式(CCM)，输出功率由下述公式确定，其中包含I_{valley}因数 Over power compensating resistor affects only the I_{peak} value, but in CCM is the output power given by following formula, where I_{valley} plays a role:

$$P_{out} = \frac{1}{2} \cdot \eta \cdot L_{prim} \cdot F_{sw} \cdot \left(I_{peak}^{\ 2} - I_{valley}^{\ 2} \right)$$

二级过载保护
2nd level over power protection

过载补偿影响二级过载保护，增加了大电压反馈前馈

The overpower compensation affects the 2nd level over power protection by the addition of bulk voltage feed forward.

$$I_{TRAN} = \frac{V_{CStran}}{R_{sense}} - \left(V_{bulk} - V_{off}\right) \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}}$$

过载补偿能用于减小变压器尺寸一半，同时维持峰值功率能力

The overpower compensation can be used for reducing the transformer size to ½ and keeping the peak power capability.

过载补偿(OPC)电子表格设计

Spread sheet design of OPC

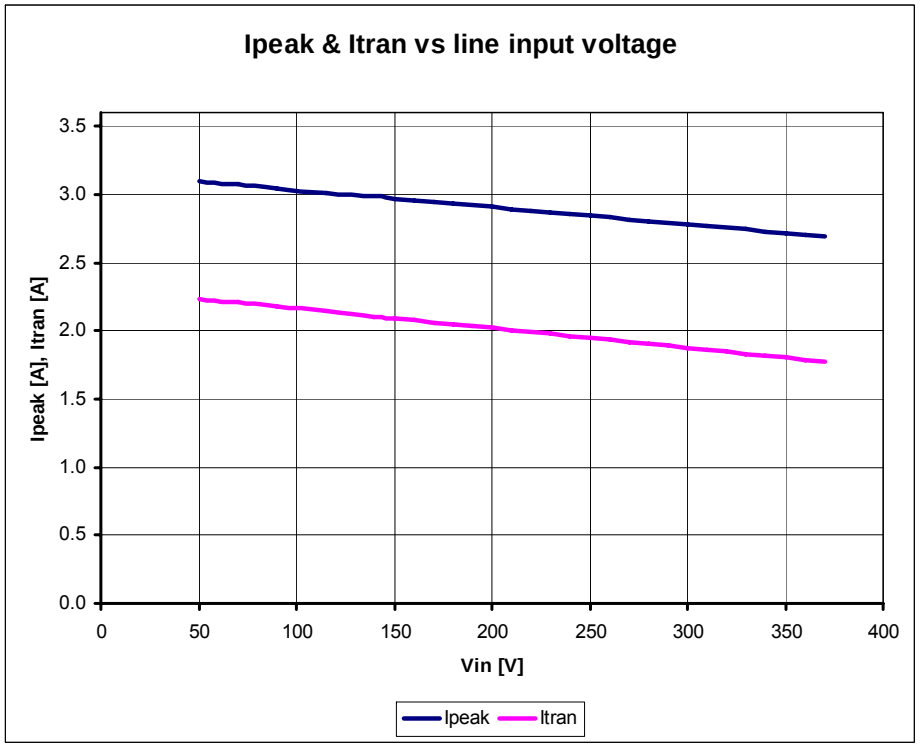
已创建OPC设计电子表格，用户能够选择恰当的R_{OPP}及其对I_{peak}、I_{tran}、P_{out}及P_{tran}的影响 OPC design spread sheet was created and the user can choose the right R_{OPP} and it's effect to I_{peak}, I_{tran}, P_{out} and P_{tran}

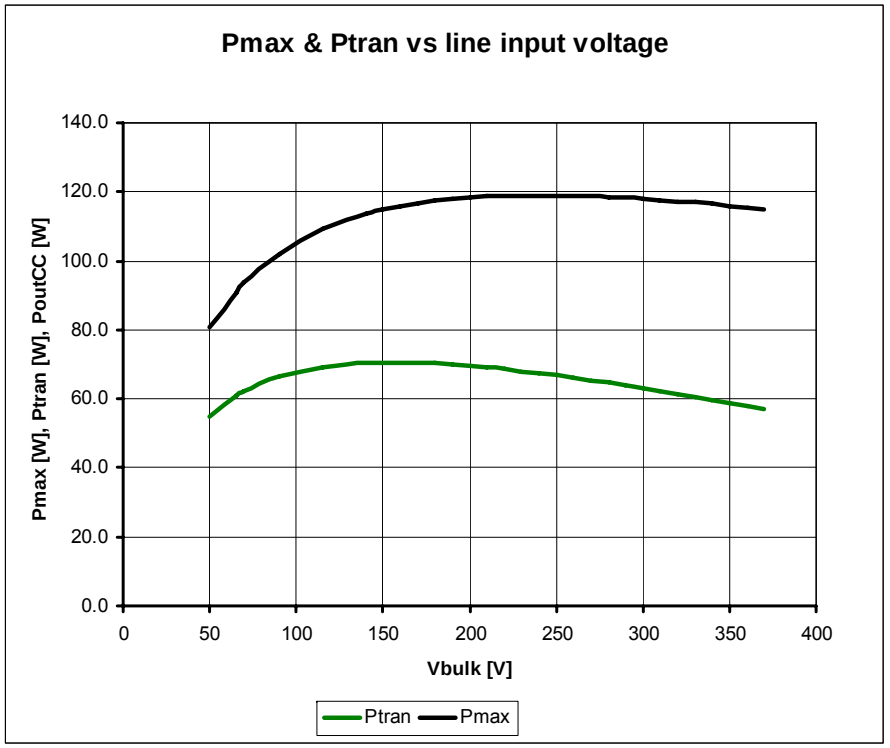
输入
Inputs:

Output voltage	Vout [V]	19
Primary turns	N1 [-]	100
Secondary turns	N2 [-]	25
Ramp Comp at CS	RaCo [mV/%]	5
Maximum int set point	Vilimit [V]	0.7
Sensing resistor	Rsense [Ohm]	0.235
Propagation delay	tprop [ns]	100
Primary inductance	Lp [uH]	560
Vin to Iopp ratio	gopp [uS]	0.5
Over power comp resistor	Ropp [Ohm]	680
Switching frequency	Fsw [kHz]	65
2nd level overcurrent prot	Vcstran [V]	0.5

即将提供，NCP1237/38/87/88也将发布 Will be available soon, while NCP1237/38/87/88 will be released

过载补偿(OPC)电子表格设计
Spread sheet design of OPC





在连续导电模式(CCM)保持恒定的峰值电流(I_{peak})，会使I_{valley}下降而V_{in}上升。这就是可提供的最大输出功率P_{out}随着V_{in}的上升而上升的原因。

注意选择恰当的补偿！ Keeping constant I_{peak} in CCM mode tends to I_{valley} decreasing with increasing the Vin. That's why the maximum output deliverable power P_{out} increases with increasing Vin. **Choose the right compensation.**

环路补偿
Loop compensation

在下述网址下载电子表格 Download the work sheet at:

www.onsemi.cn/pub/Collateral/FLYBACK DWS.XLS.ZIP

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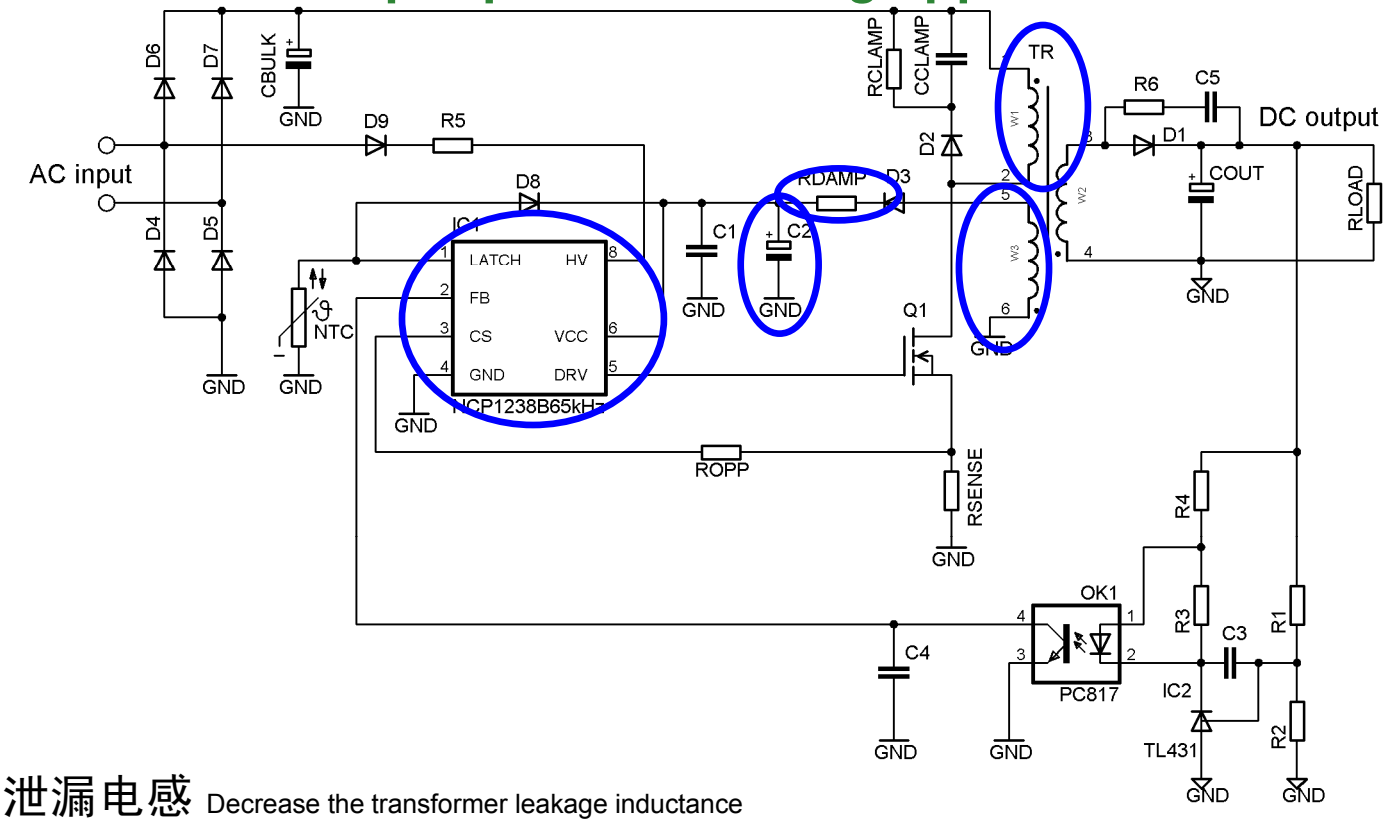
降低空载输入能耗的途径

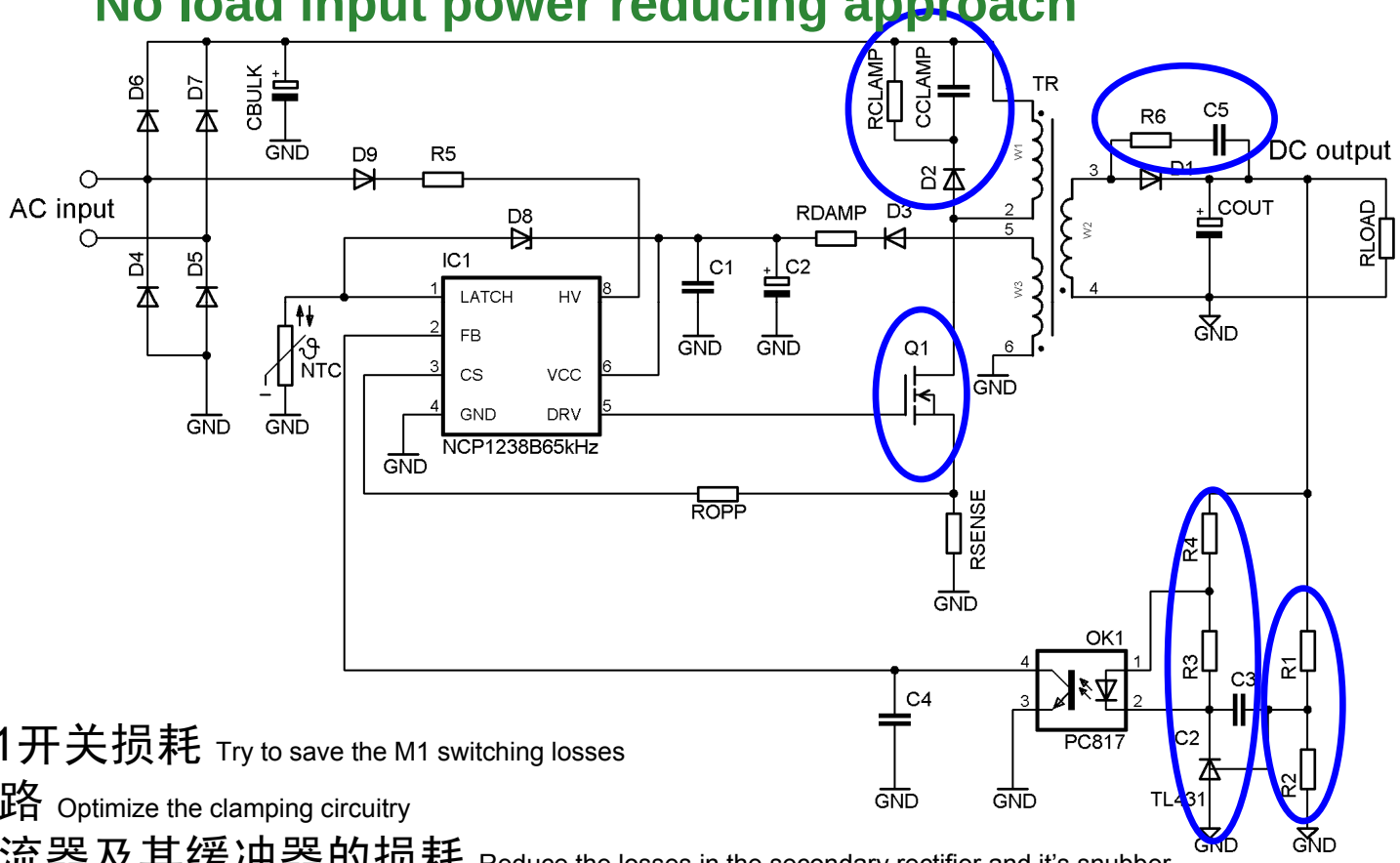
No load input power reducing approach



- 降低变压器泄漏电感 Decrease the transformer leakage inductance
- 使用带有频率反走及跳周期模式的控制器IC Use the controller IC with the frequency foldback and skip mode features
- 不允许动态自供电(DSS)工作(V_{cc}电容增加) Do not allow the DSS operation (V_{cc} cap increase)
- 出现低Vcc及高辅助绕组泄漏情况下，增加辅助绕组匝数，关闭DSS In case of low Vcc and high aux winding leakage increase the aux number of turns to disable the DSS
- 减小Vcc钳位电阻值(可能影响EMI) Decrease the value of the Vcc damping resistor (may affect the EMI)

降低空载输入能耗的途径

No load input power reducing approach



- 尝试节省M1开关损耗 Try to save the M1 switching losses
- 优化钳位电路 Optimize the clamping circuitry
- 降低次级整流器及其缓冲器的损耗 Reduce the losses in the secondary rectifier and it's snubber
- 降低TL431偏置 Decrease the TL431 biasing
- 藉反馈电阻分流器减小涡流 Decrease the cross current through the feedback resistor divider
- 为所有负载电流设定稳定的工作 Set the stable operation for the all loading currents
- 不要使用输出电压显示LED Do not use the output voltage indication LED

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面积乘积A_P
Area product A_P

- 涉及到面积乘积A_P的定义(单位m^4) There is defined the area product A_P [m^4]
- A_P为有效窗口面积W_a[m^2]与铁芯截面积A_C[m^2]的乘积 Product of effective window area W_a [m^2] and iron cross section area A_c [m^2]

$$A_P = W_a \cdot A_c$$

- 支持快速、高效及优化的磁设计 Allows fast, effective and optimal magnetic design
- 应当公布在磁芯数据表中 Should be published in core datasheet

窗口利用率Ku Window utilization factor Ku

Ku衡量的是铜出现在变压器窗口面积上的量。这窗口利用率受下列因素影响 Ku is a measure of the amount of copper that appears in the window area of transformer. This window utilization factor is affected by:

1) 线绝缘 Wire insulation
2) 线布置(占空因数) Wire lay (fill factor)
3) 线轴面积 Bobbin area
4) 多层绕线或绕线之间要求隔离 Insulation required for multilayer windings or between windings

典型窗口利用率数量在0.35至0.48范围
Typical values lay in range 0.35 to 0.48

负载系数K_{load} The load coefficient K_{load}

- 磁性元件磁通密度应该以I_{peak}设计，并带有一些裕量(5%)来防止饱和 Flux density in magnetic should be designed at I_{peak} with some margin (5%) to avoid saturation
- 你是否始终需要100%的I_{out}？ Do you really need 100% Iout for 100% time??

若不是，就减小磁芯尺寸！ If not, decrease core size!!

$$K_{load} = \frac{I_{out,RMS}}{I_{out,RMS,\max}}$$

示例 Example:

- 最大直流输出电流是3.5 A，但只在瞬态条件下需要这大电流
  Maximum DC output current is 3.5A, but it's only needed for transients
- 长期均方根值仅1.75 A(最少10分钟) The long term RMS value is only 1.75A (at least 10 min.)
- 负载系数仅为0.5(而非1) Loading coefficient is only 0.5 (not 1) → 磁芯尺寸更小 core size is smaller → 磁芯及铜损耗更少 loses in core and in copper are smaller

反激变压器磁芯尺寸确定
Flyback transformer core sizing

在下述输入条件下，磁芯尺寸能根据A_P因数来计算 The core size can be calculated by the A_P factor in case of these inputs:

1. 转换器参数 Converter parameters: L_{prim}, I_{peak}, K_{load}, δ I_r, DC_{max}
2. 考虑磁芯最大磁通密度B_{max}及开关频率F_{sw}时的磁滞和涡电流 Core maximum flux density B_{max} considered with the hysteresis and eddy current loses at switching frequency F_{sw}
3. 绕组参数(初级及次级绕组利用率Ku_{prim}及Ku_{sec})、(初级及次级绕组密度J_{prim}、J_{sec}) Winding parameters (utilization factors for primary and secondary windings Ku_{prim}, Ku_{sec}), (current densities in primary and secondary windings J_{prim}, J_{sec}

$$A_P = \frac{L_{prim} \cdot I_{peak}^{\,2}}{B_{max}} \cdot K_{load} \cdot \left(\frac{\sqrt{DC_{max}}}{J_{prim} \cdot Ku_{prim}} + \frac{\sqrt{1 - DC_{max}}}{J_{sec} \cdot Ku_{sec}} \right) \cdot \sqrt{\frac{\delta I_r^{\,2} + 12}{3 \cdot (\delta I_r + 2)^2}}$$

现在就就可以根据A_P因数从供应商产品中选择恰当的磁芯

Now the appropriate core can be selected from the vendor products list by the A_P factor .

绕组设计 Windings design

- 初级绕组匝数 Number of turns of primary winding

$$NT_{prim} = \frac{L_{prim} \cdot I_{peak}}{B_{\max} \cdot A_c}$$

- 次级绕组匝数 Number of turns of secondary winding

$$NT_{\sec} = N \cdot NT_{prim}$$

- 辅助绕组匝数 Number of turns of auxiliary winding

$$NT_{aux} = \frac{V_{CC} + V_{f,Vcc}}{V_{out} + V_{f,diode}} \cdot NT_{\sec}$$

气隙长度l_g Air gap length l_g

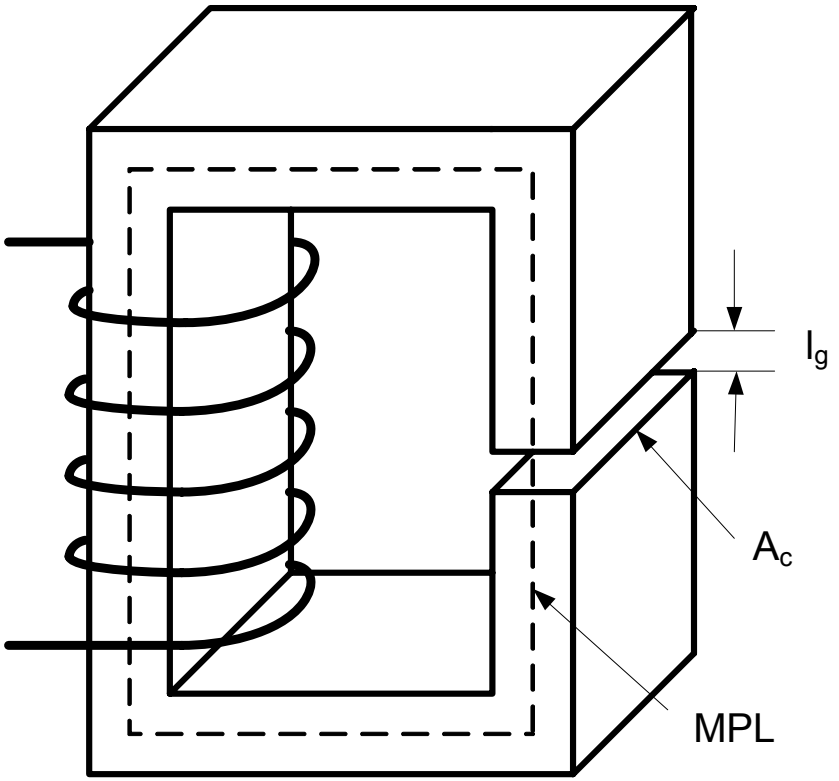
$$l_g = \frac{N \cdot \mu_0 \cdot I_{peak}}{B_{\max}} - \frac{MPL}{\mu_r}$$

条件是 in case of $l_g << MPL$

MPL – 磁通路长度 core magnetic path length

μ_0 - 真空磁导率 permeability of vacuum

μ_r - 磁芯磁导率 permeability of core



在使用EE、RM的情况下，罐型磁芯以因数2来除所计算出的l_g，因为磁芯磁通路中含有2个气隙 In case of use the EE, RM, pot core divide the calculated l_g by factor 2, because your core has 2 air gaps in magnetic path

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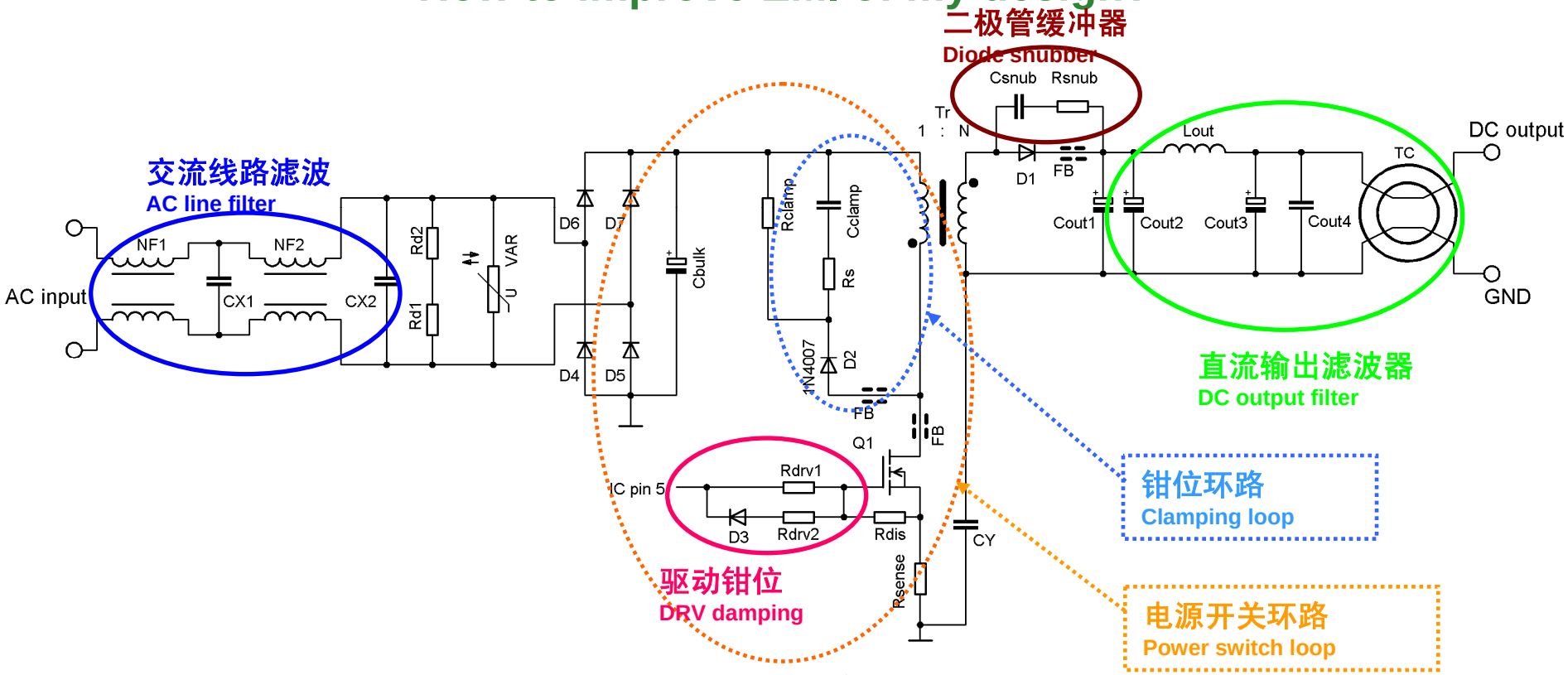
如何改善设计中的电磁干扰？
How to improve EMI of my design?



- 所有带有射频电流的开关环路的面积均应较小 All switching loops with RF currents should have small area
- 以两个扼流圈来分隔输入交流滤波器，减小寄生电容耦合影响 Divide input AC filter at two chokes to decrease the parasitic capacitance coupling
- CY-关闭通过变压器注入射频电流的电流环路 CY – closes the current loop for the RF currents injected via transformer

二极管缓冲器设计
Diode snubber design

- 缓冲器电阻应当接近振铃电路的特征阻抗 Snubber resistance should be close to characteristic impedance of ringing circuitry

$$R_{snubber} = \sqrt{\frac{L_{leak,SEC}}{C_d}}$$

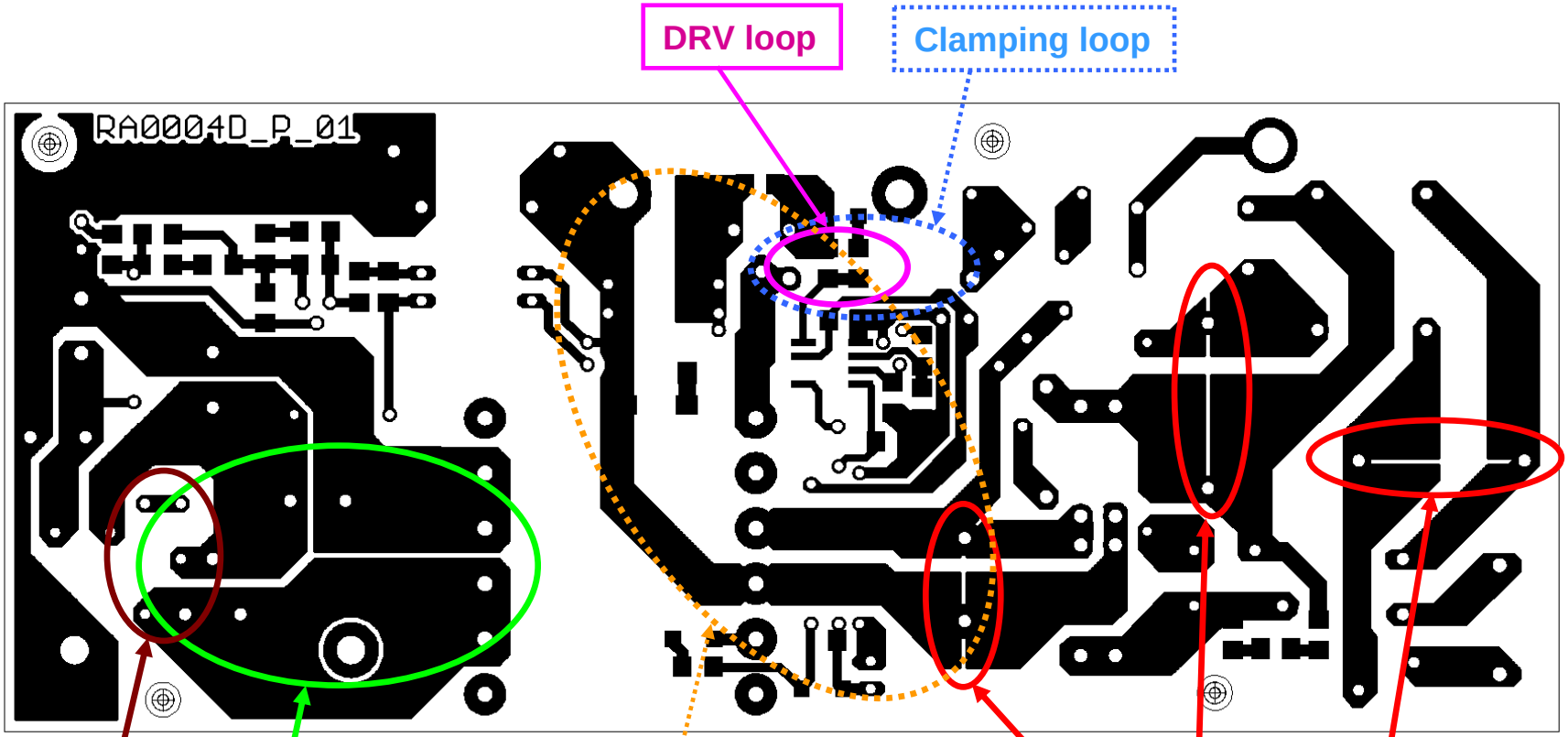
$L_{leak,SEC}$ –次级侧观测到的变压器泄漏电感
the transformer leakage inductance observed from secondary side

C_d – 反向二极管电容 reverse direction diode capacitance

- 缓冲器的RC时间常数应当相对于开关周期较小，但与电压上升时间比应当较长 RC time constant of the snubber should be small compared to the switching period but long compared to the voltage rise time

$$C_{snubber} \approx 3 \div 4 \cdot C_d$$

电路板布线窍门
PCB Layout tips



议程 Agenda

- 新的“能源之星”要求 New ENERGY STAR® requirements
- 符合新规范所需要的特性 Needed features to meet the new specification
- 新的控制器系列NCP1237/38/87/88 New controller family NCP1237/38/87/88
- 设计步骤1：电源段 Design step 1: Power stage
- 设计步骤2：设定补偿 Design step 2: Set the compensations
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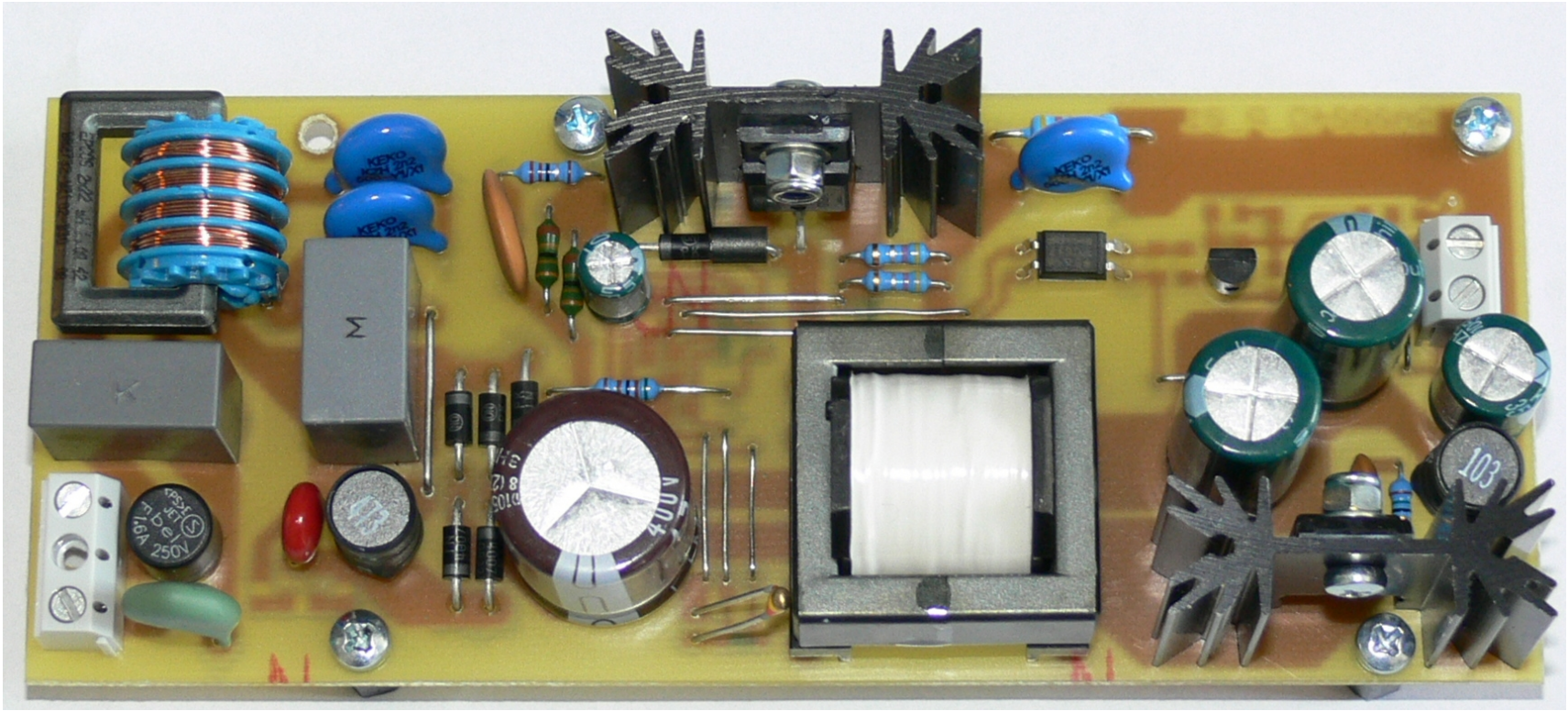
- 初步演示板示例 Preliminary demoboard example
- 总结 Summary

初步演示板
Preliminary demoboard

典型的65 W笔记本适配器(19 V输出)
A typical 65 W notebook adapter (19 V output)



(针对EPS 2.0规范优化 optimized for EPS 2.0)

初步演示板电路图
Schematic of preliminary demoboard

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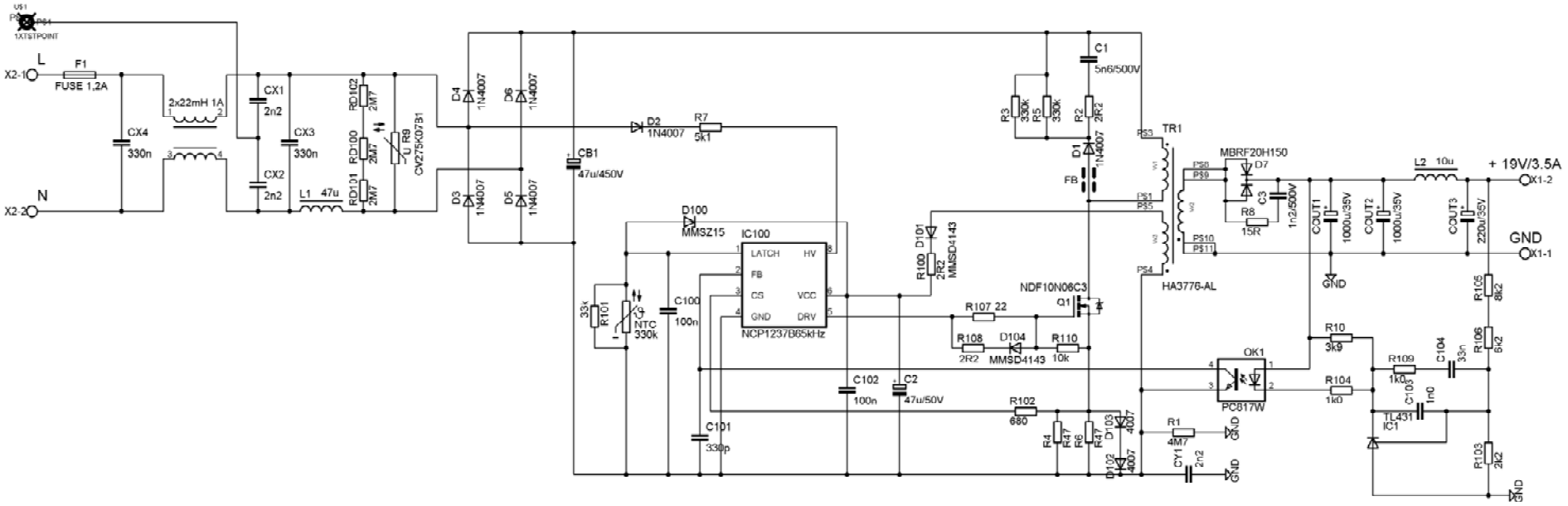
A typical 65 W notebook adapter (19 V output)



(针对EPS 2.0规范优化 optimized for EPS 2.0)

直流线缆上测得的演示板能效

Demoboard Efficiency measured with the DC cord

直流线缆长度为1.05米，铜截面积为0.75平方毫米

The DC cord length is 1.05m and copper cross sec. is 0.75mm^2

V_{IN} % of P_{OUTnom}	115 Vac/60Hz	230 Vac/60Hz
100 % (65 W)	87.10 %	87.37 %
75 % (49 W)	87.52 %	87.63 %
50 % (32 W)	87.54 %	87.88 %
25 % (16 W)	87.79 %	85.96 %

115 Vac时平均能效87.32%；230 Vac时平均能效87.21%

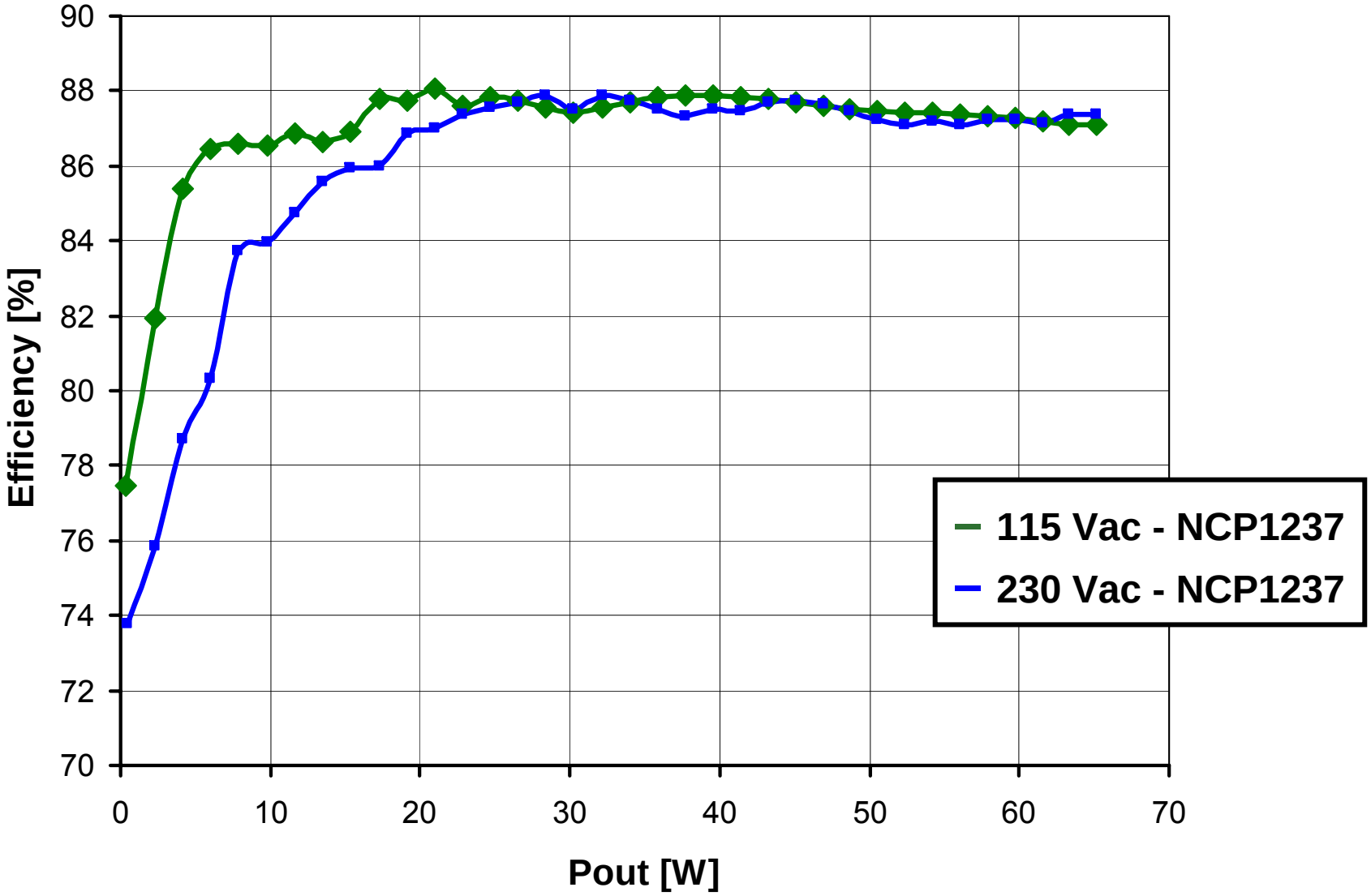
Average at 115 Vac is 87.32% and at 230 Vac is 87.21 %

演示板待机能耗 Demoboard Standby Power

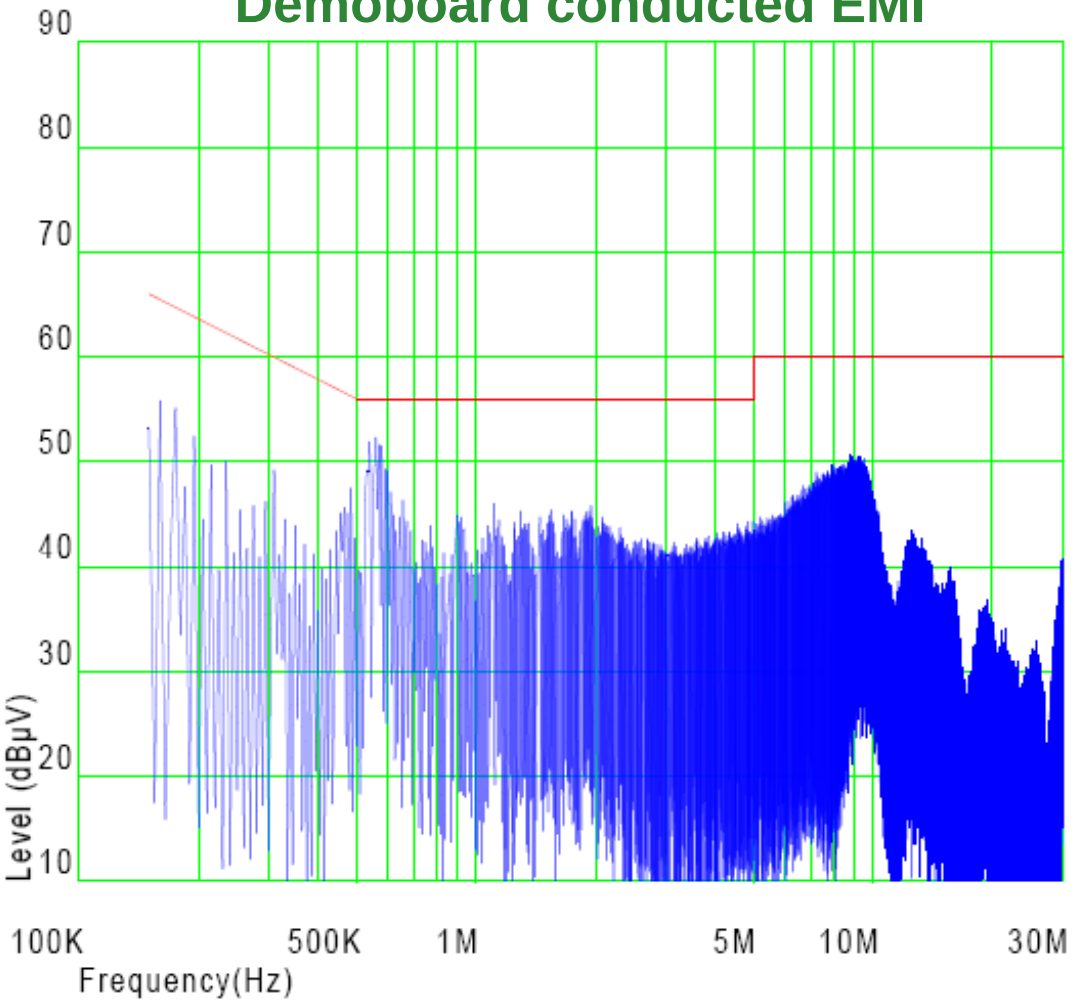
采用NCP1237的演示板轻载及空载输入能耗 Light load and no load input power with the NCP1237

P_{OUT} \ V_{IN}	115 Vac/60Hz	230 Vac/50Hz
10 % (6.5 W)	86.55 %	83.74 %
5 % (3.3 W)	85.40 %	78.72 %
1 % (0.65 W)	77.49 %	73.77 %
空载 No load	51.1 mW	73.5 mW

演示板能效 Demoboard Efficiency



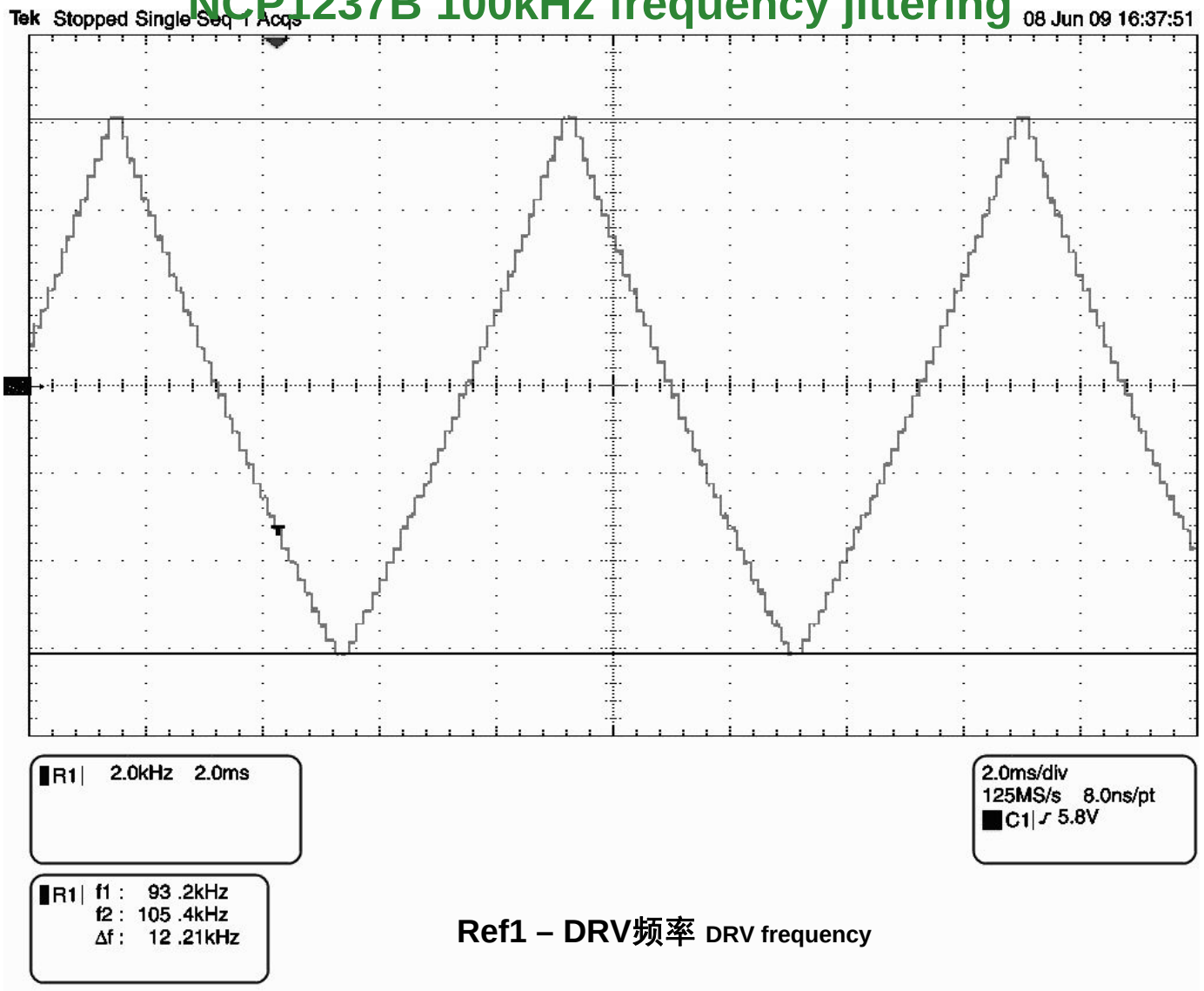
演示板导电电磁干扰
Demoboard conducted EMI



采用频率为65 kHz的NCP1237B的演示板在230 V/50 Hz条件下满载(2.72 A)的80%时的EMI 80% of full load (2.72A) at 230V/50Hz NCP1237B 65 kHz

NCP1237B100kHz频率抖动

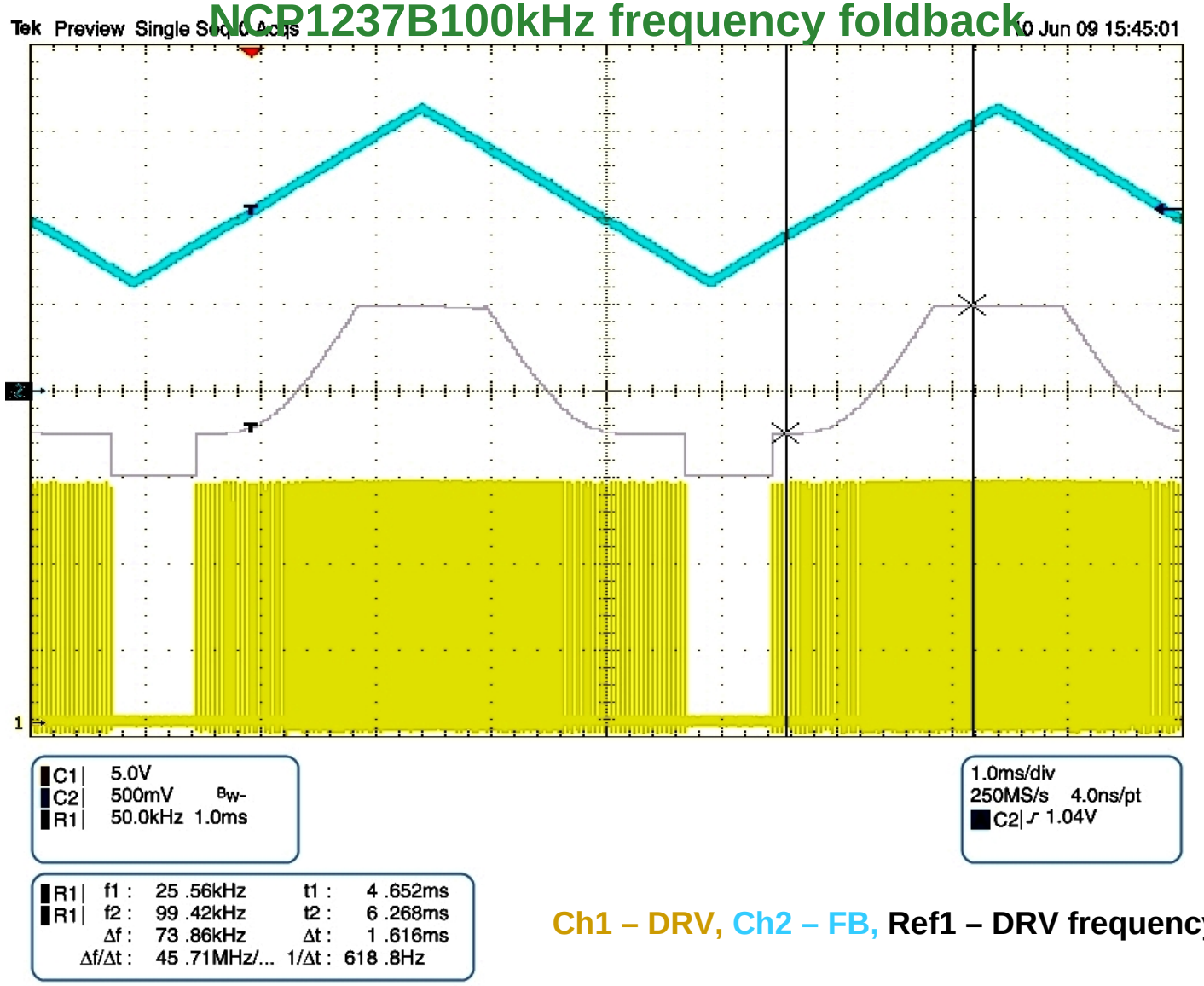
NCP1237B 100kHz frequency jittering



Ref1 – DRV频率 DRV frequency

NCP1237100kHz频率反走

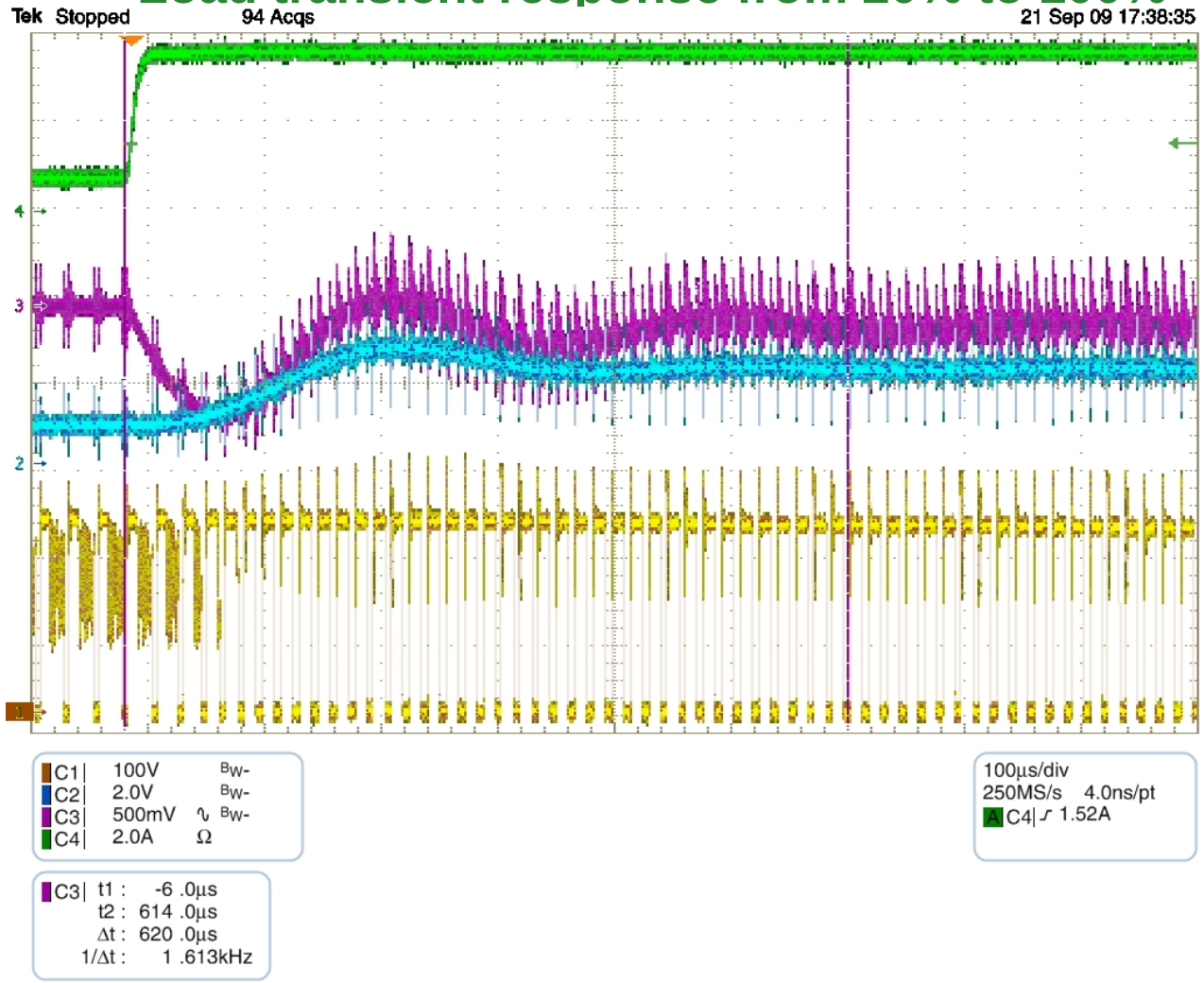
NCP1237B100kHz frequency foldback



Ch1 – DRV, Ch2 – FB, Ref1 – DRV frequency

20%负载到满载时的负载瞬态响应

Load transient response from 20% to 100%



Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout

满载到20%负载时的负载瞬态响应

Load transient response from 100% to 20%

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总结 Summary

- 有可能采用经典的反激转换器满足最新的“能源之星”或IEC规范要求 Meeting the most recent requirements from ENERGY STAR® or IEC is possible with the classical **Flyback** converter
- 带轻载时频率反走及跳周期功能的新控制器NCP1237/ 38/ 87/ 88提供这种可能性 The new controller NCP1237/38/87/88 with the frequency foldback and skip-mode at light load make it possible
- 有可能提供高于**87%**的平均能效 Average efficiencies above **87%** are possible
- 有可能提供低于**300 mW**的空载输入能耗 No-load input power below **300 mW** is possible
- 可以实现低于**100 mW**的空载输入能耗，但单凭控制IC本身无法做到。整个电源设计必须减少功率浪费 No-load input power below **100 mW** is achievable, although the controller alone cannot ensure this. The whole power supply must be designed to reduce power waste.

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies