

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

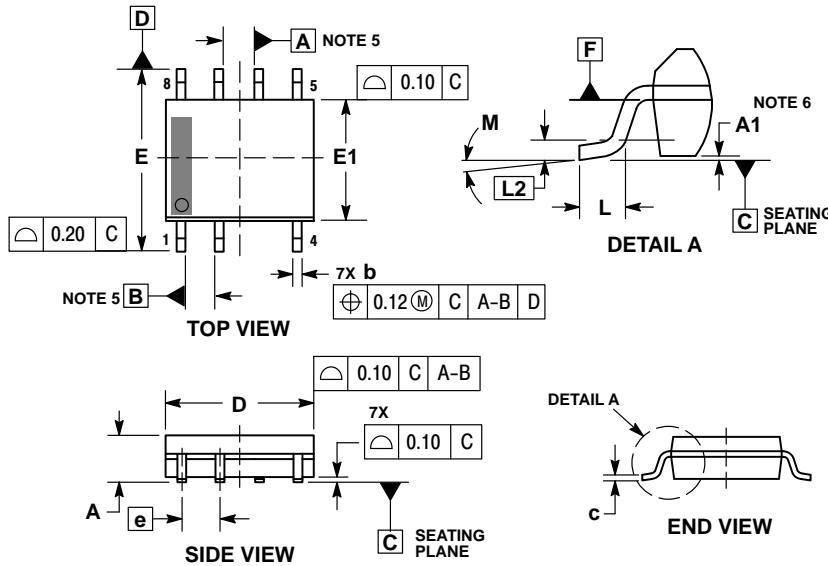
ON Semiconductor®



SCALE 1:1

SOIC8 MISSING PIN 3 CASE 751EV ISSUE O

DATE 19 SEP 2017

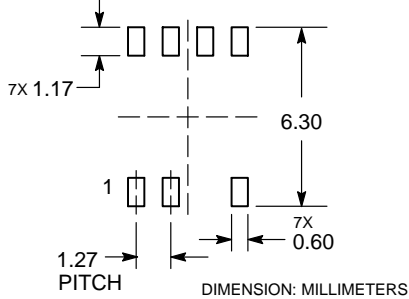


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* & *E1* DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS *D* AND *E1* ARE DETERMINED AT DATUM F.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM F.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

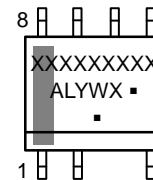
MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.19	0.25
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
M	0° - 8°	

**RECOMMENDED
SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	SOIC8 MISSING PIN 3	PAGE 1 OF 2

