PDIP−16
CASE 648−08
ISSUE V
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NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
    AGE SEATED IN JEDC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
    OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
    NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
    PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
    TO DATUM C.
6. DIMENSION eb IS MEASURED AT THE LEAD TIPS WITH THE
    LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
    LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
    CORNERS).

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. GATE
11. GATE
12. GATE
13. SOURCE
14. SOURCE
15. SOURCE
16. SOURCE

XX  XXXXXXXX XXXX XXXXXXXX
AWL YY WW G

XX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, “G" or microdot “*", may or may not be present.

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