NOTES:
2. CONTROLLING DIMENSION MILLIMETERS.
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT
   DOES NOT INCLUDE HEAT SINKS OR OTHER ATTACHED FEATURES.
4. DIMENSIONS D AND E DO NOT INCLUDE PROTRUSIONS. SUCH
   PROTRUSIONS SHALL NOT EXTEND MORE THAN 0.08 ON ANY SIDE.
   CORNERS AND EDGES OF THE PACKAGE MAY HAVE CHAMFERS.
5. PIN A1 IDENTIFICATION WILL BE IN THIS AREA. ID TYPE
   MAY CONSIST OF NOTCHES, METALLIZED MARKINGS, OR OTHER
   FEATURES.
6. THIS DIMENSION DEFINES THE MAXIMUM SIZE FOR THE PIN
   BRAZE PADS.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN.</th>
<th>MAX</th>
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<tr>
<td>A</td>
<td>3.37</td>
<td>4.13</td>
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<tr>
<td>B</td>
<td>0.25</td>
<td>0.35</td>
</tr>
<tr>
<td>D</td>
<td>35.14</td>
<td>35.86</td>
</tr>
<tr>
<td>E</td>
<td>30.19</td>
<td>30.86</td>
</tr>
<tr>
<td>eD</td>
<td>27.40</td>
<td></td>
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<tr>
<td>eE</td>
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<td></td>
</tr>
<tr>
<td>L</td>
<td>1.83</td>
<td>2.23</td>
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor® ON

DATE 30 JUN 2011

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DOCUMENT NUMBER: 98AON56484E
STATUS: ON SEMICONDUCTOR STANDARD
REFERENCE:
DESCRIPTION: CPGA168, 35.50 X 30.50

PAGE 1 OF 3
TOP OF PACKAGE

MARK THIS EDGE - ON SIDE

SIDE VIEW

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number
<table>
<thead>
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<th>ISSUE</th>
<th>REVISION</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
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<td>RELEASED FOR PRODUCTION FROM CYPRESS DRAWING #001-45332 TO ON SEMICONDUCTOR. REQ. BY K. BERKMAN.</td>
<td>30 JUN 2011</td>
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