

Product Overview

MC100EP52: ECL Differential Clock/Data D Flip-Flop

For complete documentation, see the data sheet.

The MC10EP/100EP52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the EL52 device. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP52 allow the device to also be used as a negative edge triggered device. The EP52 employs input clamping circuitry so that under open input conditions (pulled down to VEE) the outputs of the device will remain stable.

Features

- 330ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode: VCC = 3.0 V to 5.5 V with VEE = 0 V
- NECL Mode: VCC = 0 V with VEE = -3.0 V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output will default LOW with inputs open or at VEE
- Pb-Free Packages are Available

Applications

- Negative edge-triggering

Part Electrical Specifications																
Product	Pricing (\$/Unit)	Compliance	Status	Type	Bits	Input Level	Output Level	V _{CC} Typ (V)	t _{jitter} Typ (ps)	t _{pd} Typ (ns)	t _{SU} Min (ns)	t _h Min (ns)	t _{rec} Typ (ns)	t _R & t _F Max (ps)	f _{Toggle} Typ (MHz)	Package Type
MC100EP52DG		Pb-free Halide free non AEC-Q and PPAP	Active	D-Type	1	CM L ECL	ECL	3.3 5	0.2	0.33	0.05	0		170	4000	SOIC-8
MC100EP52DR2G		Pb-free Halide free non AEC-Q and PPAP	Active	D-Type	1	CM L ECL	ECL	3.3 5	0.2	0.33	0.05	0		170	4000	SOIC-8
MC100EP52DTG		Pb-free Halide free non AEC-Q and PPAP	Active	D-Type	1	CM L ECL	ECL	3.3 5	0.2	0.33	0.05	0		170	4000	TSSOP-8
MC100EP52DTR2G		Pb-free Halide free non AEC-Q and PPAP	Active	D-Type	1	CM L ECL	ECL	3.3 5	0.2	0.33	0.05	0		170	4000	TSSOP-8
MC100EP52MNR4G		Pb-free Halide free non AEC-Q and PPAP	Active	D-Type	1	CM L ECL	ECL	3.3 5	0.2	0.33	0.05	0	-	170	4000	DFN-8

For more information please contact your local sales support at www.onsemi.com.

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