Product Overview

NB6L14M: Clock / Data Fanout Buffer, 1:4 Differential, with CML Outputs

For complete documentation, see the data sheet.

The NB6L14M is a 3.0GHz differential 1:4 CML clock or data fanout buffer. The differential inputs incorporate internal 50-ohm termination resistors that are accessed through the VT pin. This feature allows the NB6L14M to accept various logic standards, such as CML, LVCMOS, LVTTL, CML, or LVDS logic levels. The 16mA differential CML outputs provide matching internal 50-ohm terminations and produce 400mV output swings when externally terminated with a 50-ohm resistor to VCC. The VREFAC reference output can be used to rebias capacitor-coupled differential or single-ended input signals. The 1:4 fanout design was optimized for low output skew applications. The NB6L14M is a member of the ECLinPS MAX family of high performance clock and data management products.

Features

- Input Clock Frequency > 3.0 GHz
- < 20 ps Within Device Output Skew
- Internal Input and Output Termination Resistors, 50-ohm
- VREFAC Reference Output

Benefits

- High performance applications
- Low Output-to-output skew
- No external components needed
- Rebias Capacitor-coupled Input Signals

Applications

- Cloack / Data Distribution

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	$t_{JitterRMS}$ Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NB6L14MMNG		Pb-free Halide free non AEC-Q and PPAP	Active	Buffer	1	1:4	CML LVDS LVPECL	CML	2.5 3.3	0.2	20	0.35	150	3000	2500	QFN-16
NB6L14MMNR2G		Pb-free Halide free non AEC-Q and PPAP	Active	Buffer	1	1:4	CML LVDS LVPECL	CML	2.5 3.3	0.2	20	0.35	150	3000	2500	QFN-16

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