Product Overview

PCA9655E: I/O Port Expander, I²C, 16-bit, Remote Low Voltage w/Interrupt

For complete documentation, see the data sheet.

The PCA9655E provides 16 bits of General Purpose parallel Input and Output (GPIO) expansion through the I2C-bus and SMBus. The PCA9655E consists of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity Inversion (active-HIGH) or active-LOW operation) registers. At power on, all IOs default to inputs. Each IO may be configured as either input or output by writing to its corresponding IO configuration bit. The data for each Input or Output is kept in its corresponding Input or Output register. The Polarity Inversion register may be used to invert the Polarity if the read register. All registers can be read by the system master.
The PCA9655E provides an open-drain interrupt output which is activated when any input state differs from its corresponding input port register state. The interrupt output is used to indicate to the system master that an input state has changed. The power-on reste sets the registers to their default values and initializes the device state machine.
Three hardware pins (AD0, AD1, AD2) are used to configure the I2C-bus slave address of the device. Up to 64 devices are allowed to share the same I2C-bus and SMBus.

Features

- VCC Operating Range: 1.65 V to 5.5 V
- SDA Sink Capability: 30 mA
- 5.5 V Tolerant I/Os
- Polarity Inversion Register
- Active LOW Interrupt Output
- Low Standby Current
- Noise Filter on SCL/SDA Inputs
- No Glitch on Powerup
- Internal Poweron Reset
- 64 Programmable Slave Addresses Using Three Address Pins

  For more features, see the data sheet

Applications

- Input/output Port Expansion for Extended Addressing Capability

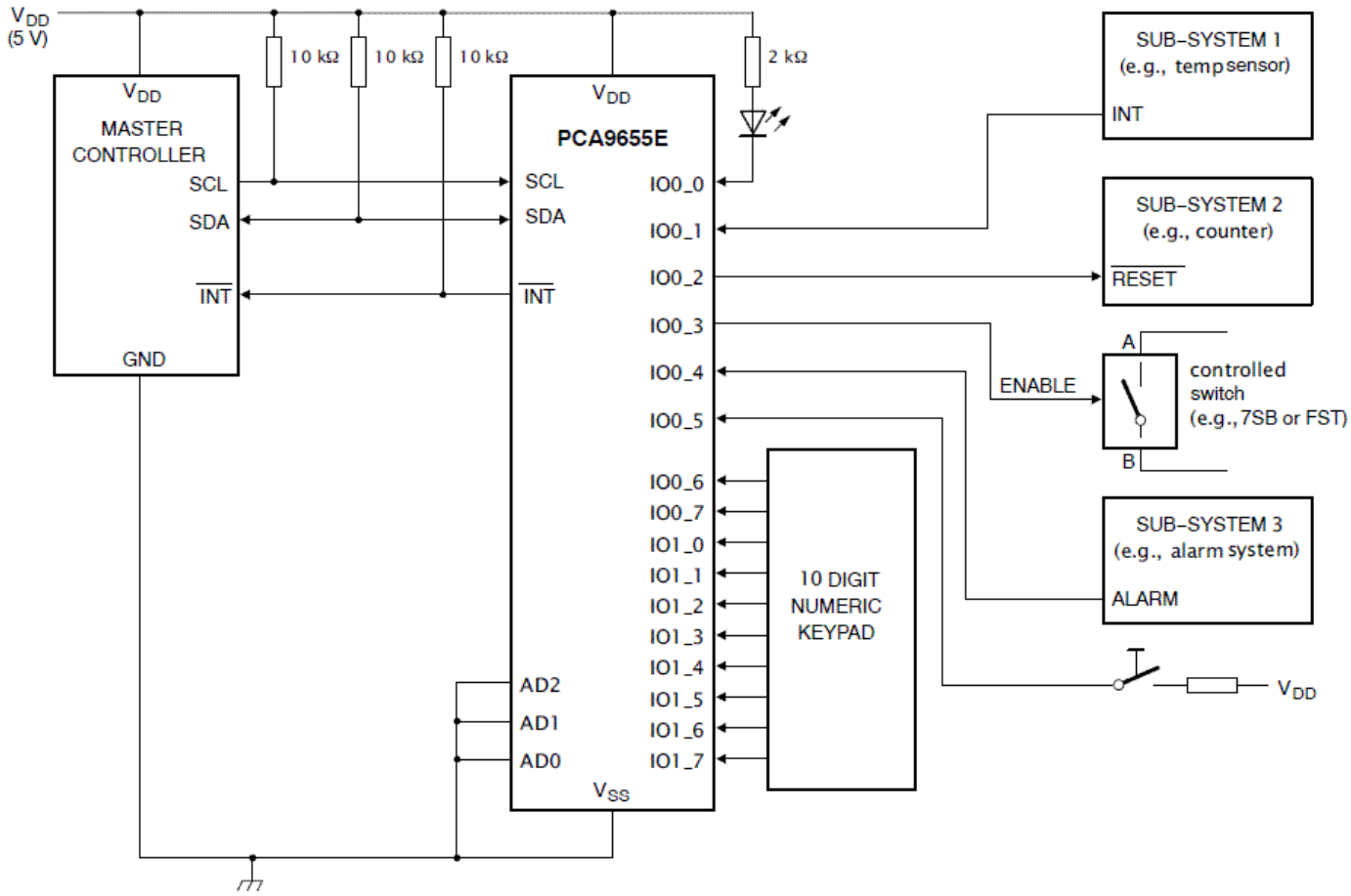
End Products

- Keyboards

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	I/O	Cascadable	V_{CC} Min (V)	V_{CC} Max (V)	Interrupt Output	I/O Pullups	LED Blink/PWM	I_O Min (mA)	Package Type
PCA9655EDTR2G	0.773	Pb-free Halide free non AEC-Q and PPAP	Active	16	8 Slave ID Addresses	1.65	5.5	Yes	Yes	No	25	TSSOP-24
PCA9655EDWR2G	0.773	Pb-free Halide free non AEC-Q and PPAP	Active	16	8 Slave ID Addresses	1.65	5.5	Yes	Yes	No	25	SOIC−24 WB
PCA9655EMTTXG	0.986	Pb-free Halide free non AEC-Q and PPAP	Active	16	8 Slave ID Addresses	1.65	5.5	Yes	Yes	No	25	QFN-24

Application Diagram



Device address configured as 0100 000xb for this example.

IO0_0, IO0_2, IO0_3 configured as outputs.

IO0_1, IO0_4, IO0_5 configured as inputs.

IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

For more information please contact your local sales support at www.onsemi.com.

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