MC74HC73A

Dual JK Flip Flop with Reset

Product Overview

For complete documentation, see the data sheet.

High Performance Silicon Gate CMOS. The MC74HC73A is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs. Each flip flop is negative edge clocked and has an active low asynchronous reset. The MC74HC73A is identical in function to the HC107, but has a different pinout.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 92 FETs or 23 Equivalent Gates
- These are PbFree Devices

Applications

- Desktop

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
MC74HC73ADG	0.188	Pb H	Active	JK-Type	2	2	6	21	5.2	SOIC-14
MC74HC73ADR2G	0.142	Pb H	Active	JK-Type	2	2	6	21	5.2	SOIC-14
MC74HC73ADTR2G	0.1567	Pb H	Active	JK-Type	2	2	6	21	5.2	TSSOP-14
NLV74HC73ADR2G	0.198	A P Pb H	Active	JK-Type	2	2	6	21	5.2	SOIC-14