# MC74HC112A

# Dual JK Flip-Flop with Set and Reset

## Product Overview

For complete documentation, see the data sheet.

High Performance Silicon Gate CMOS The MC74HC112A is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs. Each flip flop is negative edge clocked and has active low asynchronous Set and Reset inputs. The HC112A is identical in function to the HC76, but has a different pinout.

### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- PbFree Packages are Available

### Applications

- Desktop, White Goods, etc.

## Part Electrical Specifications

| Product | Pricing ($/Unit) | Compliance | Status | Type | Channels | $V_{CC}$ Min (V) | $V_{CC}$ Max (V) | $t_{pd}$ Max (ns) | $I_O$ Max (mA) | Package Type |
|---|---|---|---|---|---|---|---|---|---|---|
| MC74HC112ADR2G | 0.1557 | Pb H | Active | JK-Type | 2 | 2 | 6 | 21 | 5.2 | SOIC-16 |
| MC74HC112ADTG | 0.222 | Pb H | Active | JK-Type | 2 | 2 | 6 | 21 | 5.2 | TSSOP-16 |
| MC74HC112ADTR2G | 0.168 | Pb H | Active | JK-Type | 2 | 2 | 6 | 21 | 5.2 | TSSOP-16 |