74LVX273

Low Voltage Octal D-Type Flip-Flop

Product Overview

For complete documentation, see the data sheet.

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR#) input load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR# input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Applications

- This product is general usage and suitable for many different applications.

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
74LVX273MTCX	0.2644	Pb	Active	Octal D-type	8	2	3.6	14.5	4	TSSOP-20