74LCX112

Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

Product Overview

For complete documentation, see the data sheet.

The LCX112 is a dual J-K flip-flop. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs with Q, Q# outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V or 2.5) operation with the added capability of interfacing to a 5V signal environment. The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 2.3V-3.6V VCC specifications provided
- 7.5 ns tPD max (VCC = 3.3V), 10 µA ICC max
- Power down high impedance inputs and outputs
- ±24 mA output drive (VCC = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance: Human body model > 2000V Machine model > 2000V

Applications

- This product is general usage and suitable for many different applications.

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
74LCX112MTCX	0.2187	Pb H	Active	Dual J-K negative edge-triggered	2	2	3.6	7.5	24	TSSOP-16
74LCX112MX	0.5307	Pb	Active	Dual J-K negative edge-triggered	2	2	3.6	7.5	24	SOIC-16