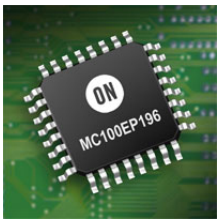
MC100EP196

3.3 V ECL Programmable Delay Chip



Product Overview

For complete documentation, see the data sheet.

The MC100EP196 is a programmable delay chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides programmably variable delay of a differential ECL input signal. It has similar architecture to the EP195 with the added feature of further tuneability in delay using the FTUNE pin. The FTUNE input takes an analog voltage from VCC to VEE to fine tune the output delay from 0 to 60 ps.

Features

- Maximum Frequency > 1.2 GHz Typical
- PECL Mode Operating Range: VCC = 3.0 V to 3.6 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -3.6 V
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the ENbar Pin Will Force Q to Logic Low
- D[0:10] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- VBB Output Reference Voltage
- Pb-Free Packages are Available

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	$t_{d(prog)}$ Min (ns)	$t_{d(prog)}$ Max (ns)	$t_{d(step)}$ Typ (ps)	t_{Jitter} Typ (ps)	t_R & t_F Max (ps)	Package Type
MC100EP196FAG	7	Pb H	Active		ECL	3.3	1200	8.6	12	11	3	200	LQFP-32
MC100EP196FAR2G	7	Pb H	Active		ECL	3.3	1200	8.6	12	11	3	200	LQFP-32